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Lab 1: Introduction to Cadence Schematic Capture and Simulation

ECEN 454 - 503

September 19, 2022

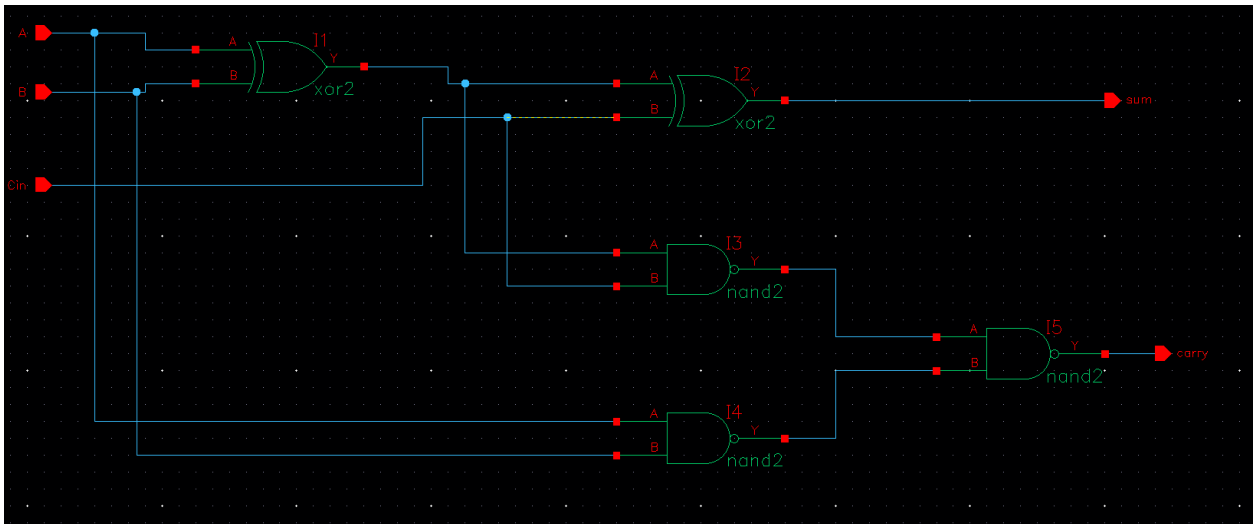
Introduction

The objective of this first lab was to learn how to utilize cadence and design a full adder, 4-bit adder, and 8-bit adder. All the designs, symbols, and results are below.

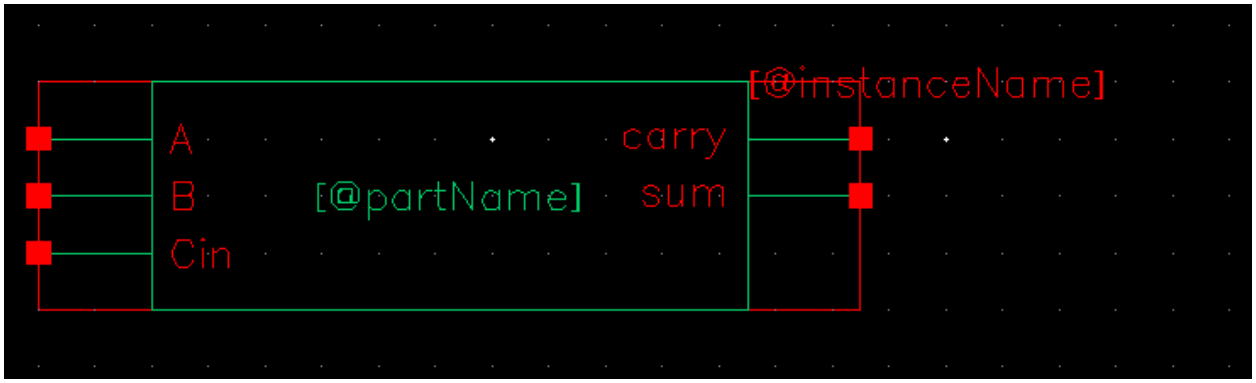
Result

Full Adder

Design



Symbol



Code

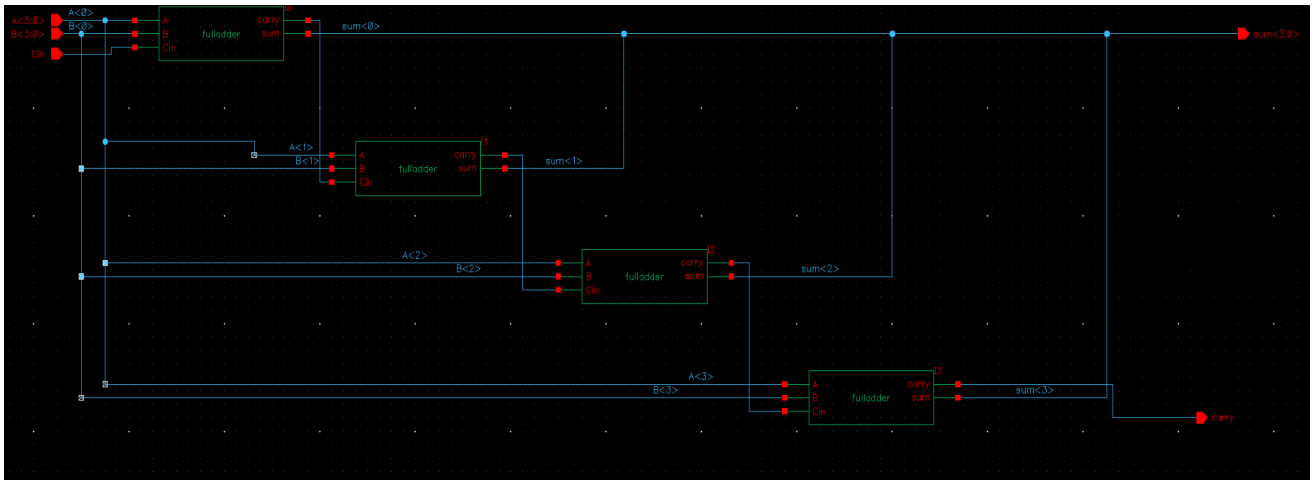
```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
$monitor ($time," A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);


initial
begin

   A = 1'b0;
   B = 1'b0;
   Cin = 1'b0;

#50 A=1'b0; B=1'b0; Cin=1'b1;           //ABC=001
#50 A=1'b0; B=1'b1; Cin=1'b0;           //ABC=010
#50 A=1'b0; B=1'b1; Cin=1'b1;           //ABC=011
#50 A=1'b1; B=1'b0; Cin=1'b0;           //ABC=100
#50 A=1'b1; B=1'b0; Cin=1'b1;           //ABC=101
#50 A=1'b1; B=1'b1; Cin=1'b0;           //ABC=110
#50 A=1'b1; B=1'b1; Cin=1'b1;           //ABC=111
end
```

Simulation

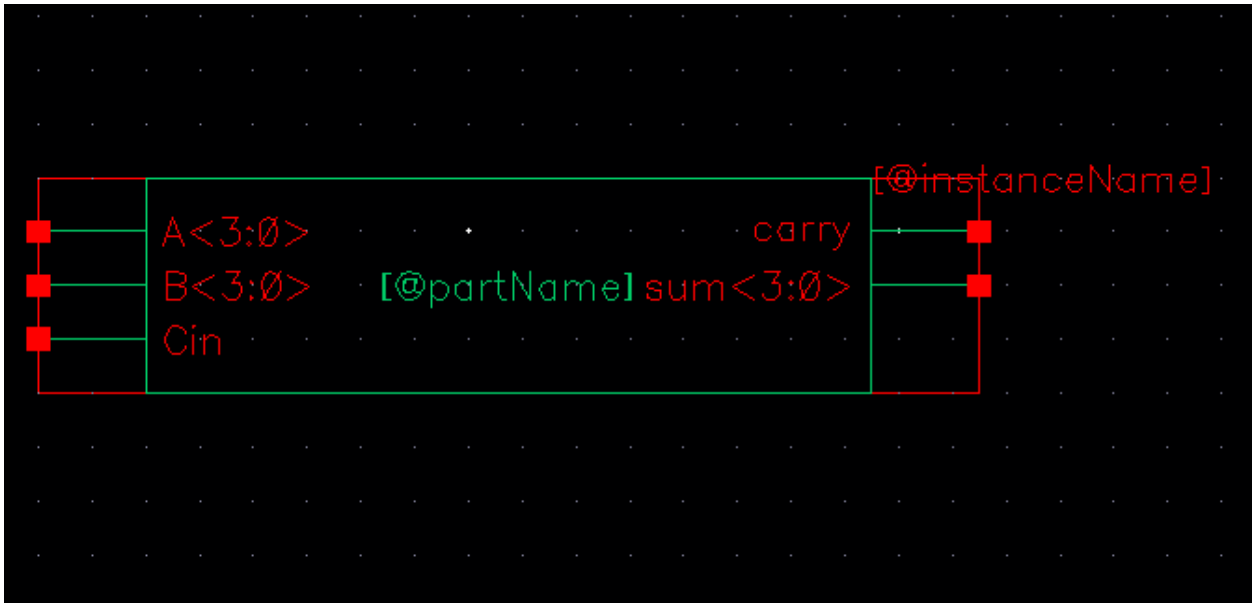
```
TOOL:   ncxlmode        15.20-s086: Started on Sep 16, 2022 at 17:31:20 CDT
ncxlmode
        +delay_mode_path
        +typdelays
        -l
        simout.tmp
        /home/ugrads/e/esha.adhawade/ecen454_503/fulladder_run1/testfixture.template
        -f /home/ugrads/e/esha.adhawade/ecen454_503/fulladder_run1/verilog.inpfiles
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nand2/functional/verilog.v
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xor2/functional/verilog.v
                ihnl/cds0/netlist
        +nostdout
        +nocopyright
        +ncvlogargs+" -neverwarn -nostdout -nocopyright "
        +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -timescale 1ns/1ns -nostdout -
nocopyright"
        +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/ugrads/e/esha.adhawade/ecen454_503/fulladder_run1/.simTmpNCCmd "
        +mpssession+virtuoso20730
        +mpshost+zach-127-09.engr.tamu.edu

-----------------------------------
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
               0 A=0, B=0, Cin=0, sum=0, carry=0
              50 A=0, B=0, Cin=1, sum=1, carry=0
             100 A=0, B=1, Cin=0, sum=1, carry=0
             150 A=0, B=1, Cin=1, sum=0, carry=1
             200 A=1, B=0, Cin=0, sum=1, carry=0
             250 A=1, B=0, Cin=1, sum=0, carry=1
             300 A=1, B=1, Cin=0, sum=0, carry=1
             350 A=1, B=1, Cin=1, sum=1, carry=1
ncsim>
```

4-Bit Adder

Design



Symbol



Code

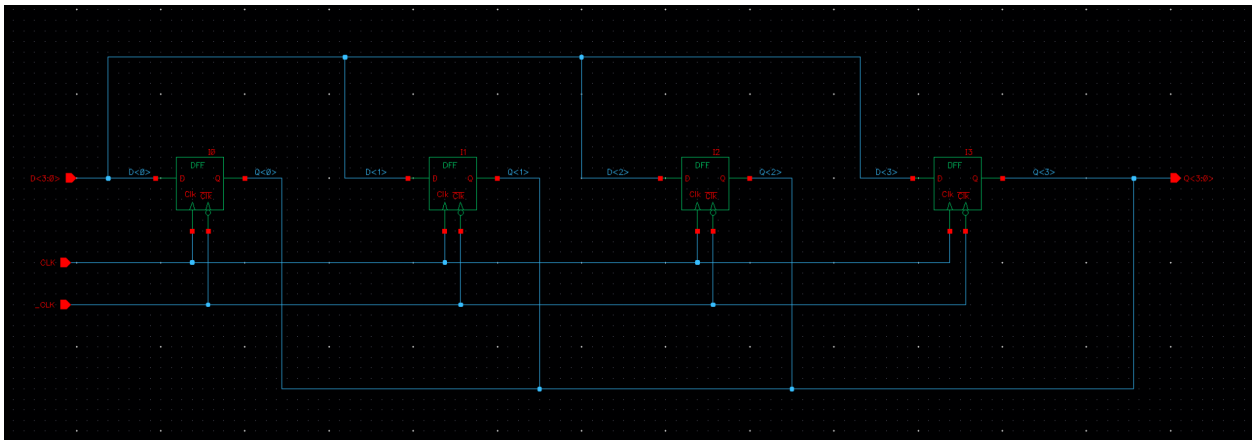
```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.

initial
$monitor ($time," A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);


initial
begin

    A[3:0] = 4'b0000;

    B[3:0] = 4'b0000;

    Cin = 1'b0;

#50 A[3:0]=4'b1111; B[3:0]=4'b1111; Cin=1'b0;           //ABC=1111 1111 0
#50 A[3:0]=4'b1010; B[3:0]=4'b1010; Cin=1'b1;           //ABC=1010 1010 1
#50 A[3:0]=4'b0101; B[3:0]=4'b0101; Cin=1'b1;           //ABC=0101 0101 1

end

```

Simulation

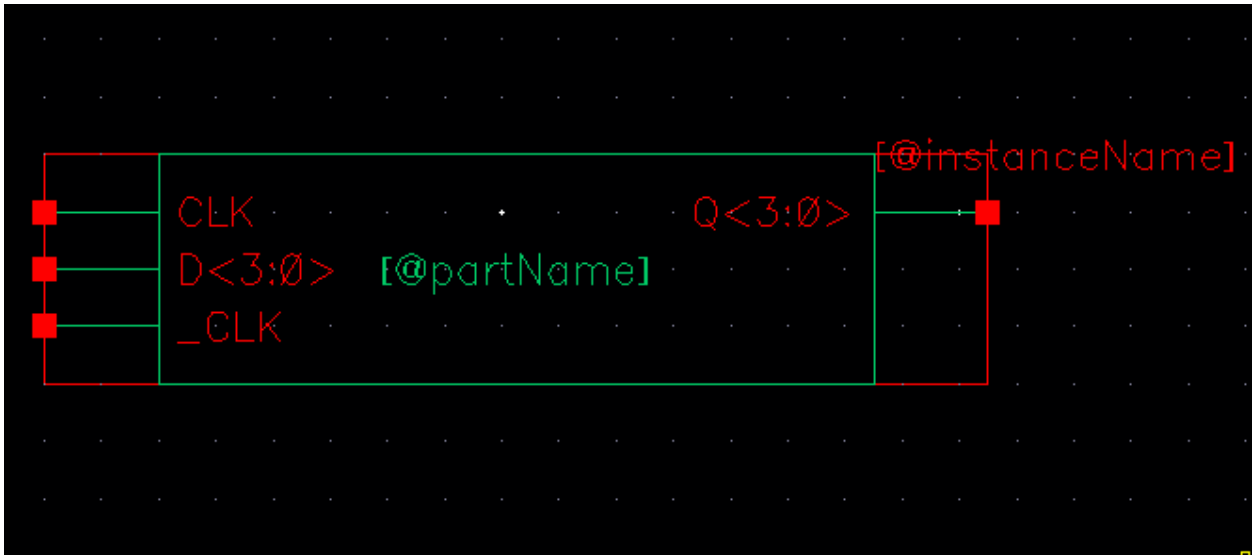
```
TOOL:   ncxlmode        15.20-s086: Started on Sep 16, 2022 at 19:19:19 CDT
ncxlmode
        +delay_mode_path
        +typdelays
        -l
        simout.tmp
        /home/ugrads/e/esha.adhawade/ecen454_503/4-bitadder_run1/testfixture.template
        -f /home/ugrads/e/esha.adhawade/ecen454_503/4-bitadder_run1/verilog.inpfiles
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/nand2/functional/verilog.v
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xor2/functional/verilog.v
                ihnl/cds0/netlist
                ihnl/cds1/netlist
        +nostdout
        +nocopyright
        +ncvlogargs+" -neverwarn -nostdout -nocopyright "
        +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -timescale 1ns/1ns -nostdout -
nocopyright"
        +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/ugrads/e/esha.adhawade/ecen454_503/4-bitadder_run1/.simTmpNCCmd "
        +mpssession+virtuoso20730
        +mpshost+zach-127-09.engr.tamu.edu

-----------------------------------
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                  0 A=0000, B=0000, Cin=0, sum=0000, carry=0
                 50 A=1111, B=1111, Cin=0, sum=1110, carry=1
                100 A=1010, B=1010, Cin=1, sum=0101, carry=1
                150 A=0101, B=0101, Cin=1, sum=1011, carry=0
ncsim> run
ncsim>
```

4-Bit Register

Design

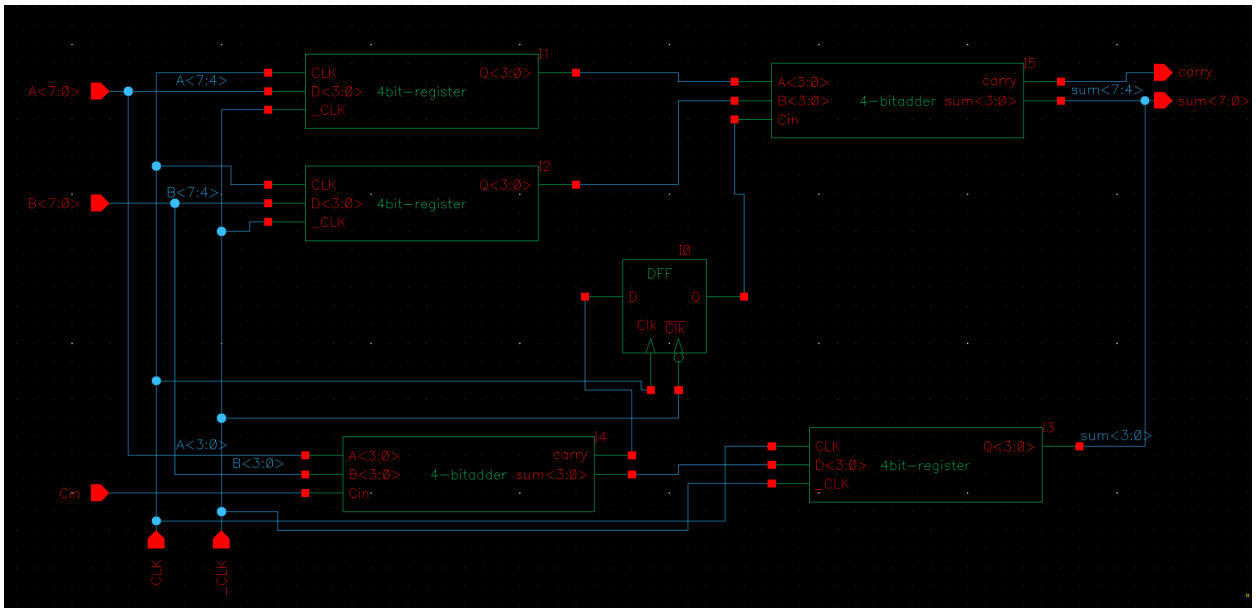


Symbol

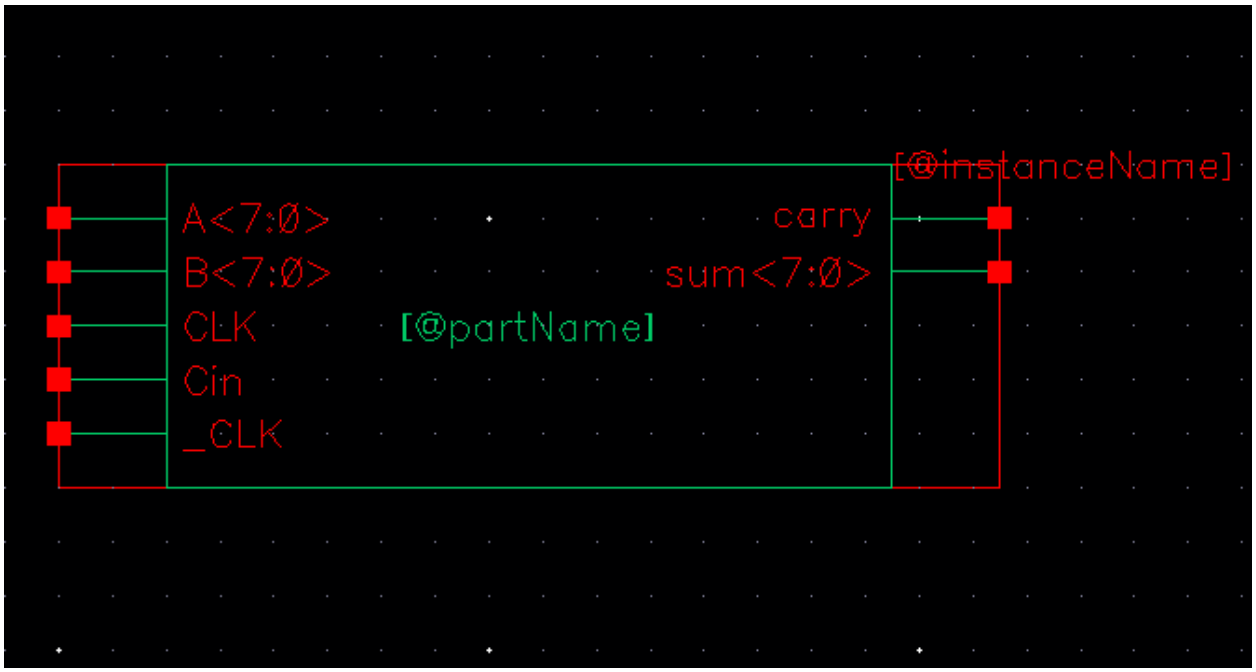


8-Bit Adder

Design



Symbol



Code

```
// Verilog stimulus file.
// Please do not create a module in this file.


// Default verilog stimulus.



always
#1 CLK= !CLK;
always
#1 _CLK= !CLK;

initial
begin

   A[7:0] = 8'b00000000;

   B[7:0] = 8'b00000000;

   CLK = 1'b0;
   Cin = 1'b0;
   _CLK = 1'b0;
   $monitor ($time, " A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);


        #50 A=8'b01111110; B=8'b11100111; Cin=1'b0;           //ABC=01111110 11100111 0
        $monitor ($time, " A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);

        #50 A=8'b11111111; B=8'b00000000; Cin=1'b1;           //ABC=11111111 00000000 1
        $monitor ($time, " A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);

        #50 A=8'b10101010; B=8'b01010101; Cin=1'b0;           //ABC=10101010 01010101 0
        $monitor ($time, " A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);

        #50 A=8'b10101010; B=8'b01010101; Cin=1'b1;           //ABC=10101010 00000000 1
        $monitor ($time, " A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);

        #50 A=8'b11001100; B=8'b00110011; Cin=1'b0;           //ABC=11001100 00110011 0
        $monitor ($time, " A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);

        #50 A=8'b11001100; B=8'b00110011; Cin=1'b1;           //ABC=11001100 00110011 1
        $monitor ($time, " A=%b, B=%b, Cin=%b, sum=%b, carry=%b", A, B, Cin, sum, carry);
#50 $finish;
end
```

Simulation

```
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/xor2/functional/verilog.v
                /opt/coe/ncsu/ncsu-cdk-1.6.0.beta/lib/NCSU_Digital_Parts/Dlatch/behavioral/verilog.v
                ihnl/cds0/netlist
                ihnl/cds1/netlist
                ihnl/cds2/netlist
                ihnl/cds3/netlist
                ihnl/cds4/netlist
        +nostdout
        +nocopyright
        +ncvlogargs+" -neverwarn -nostdout -nocopyright "
        +ncelabargs+" -neg_tchk  -nonotifier  -sdf_NOCheck_celltype  -access +r  -pulse_e 100  -pulse_r 100  -neverwarn  -timescale 1ns/1ns -nostdout -
nocopyright"
        +ncsimargs+" -neverwarn  -nocopyright -gui -input /home/ugrads/e/esha.adhawade/ecen454_503/8-bitadder_run1/.simTmpNCCmd "
        +mpssession+virtuoso20730
        +mpshost+zach-127-09.engr.tamu.edu

-------------------------------------
Relinquished control to SimVision...
ncsim>
ncsim> source /opt/coe/cadence/INCISIVE152/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test  -all   -depth 1
Created probe 1
ncsim> run
                  0 A=00000000, B=00000000, Cin=0, sum=xxxxxxxx, carry=x
                  3 A=00000000, B=00000000, Cin=0, sum=00000000, carry=0
                 50 A=01111110, B=11100111, Cin=0, sum=00000000, carry=0
                 51 A=01111110, B=11100111, Cin=0, sum=01100101, carry=1
                100 A=11111111, B=00000000, Cin=1, sum=01100101, carry=1
                101 A=11111111, B=00000000, Cin=1, sum=00000000, carry=1
                150 A=10101010, B=01010101, Cin=0, sum=00000000, carry=1
                151 A=10101010, B=01010101, Cin=0, sum=11111111, carry=0
                200 A=10101010, B=01010101, Cin=1, sum=11111111, carry=0
                201 A=10101010, B=01010101, Cin=1, sum=00000000, carry=1
                250 A=11001100, B=00110011, Cin=0, sum=00000000, carry=1
                251 A=11001100, B=00110011, Cin=0, sum=11111111, carry=0
                300 A=11001100, B=00110011, Cin=1, sum=11111111, carry=0
                301 A=11001100, B=00110011, Cin=1, sum=00000000, carry=1
Simulation complete via $finish(1) at time 350 NS + 0
./testfixture.verilog:45 #50 $finish;
ncsim>
```