Lab 9: Introduction to High-Speed Addition

ECEN 248 - 505

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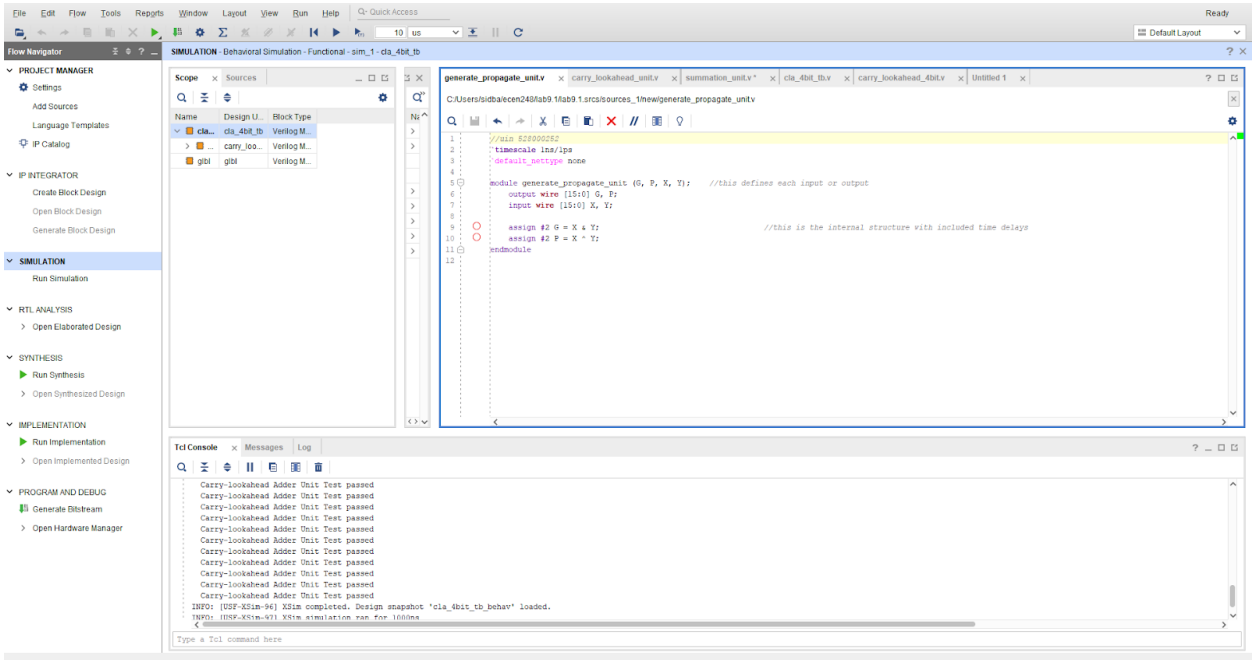
Objectives

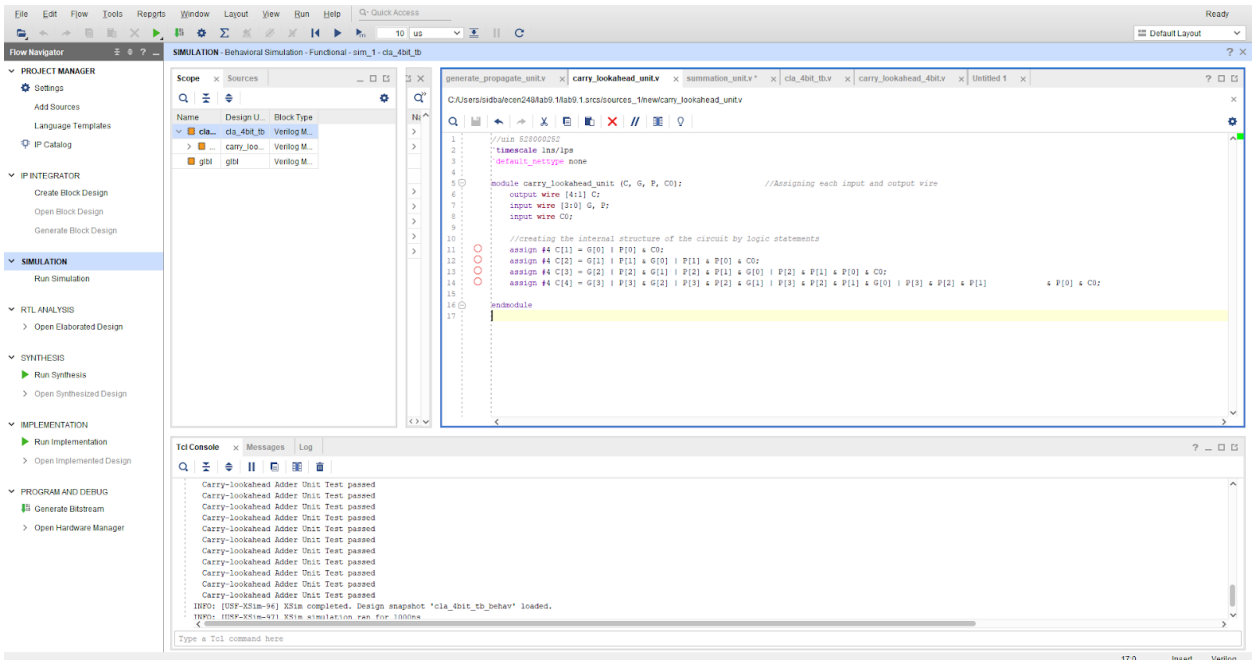
The purpose of this lab is to help students learn the purpose of how certain circuits are made for specific tasks. For example, carry-lookahead addition is used for fast addition in high-speed arithmetic units. This involves the usage of the dataflow of structural Verilog.

Design

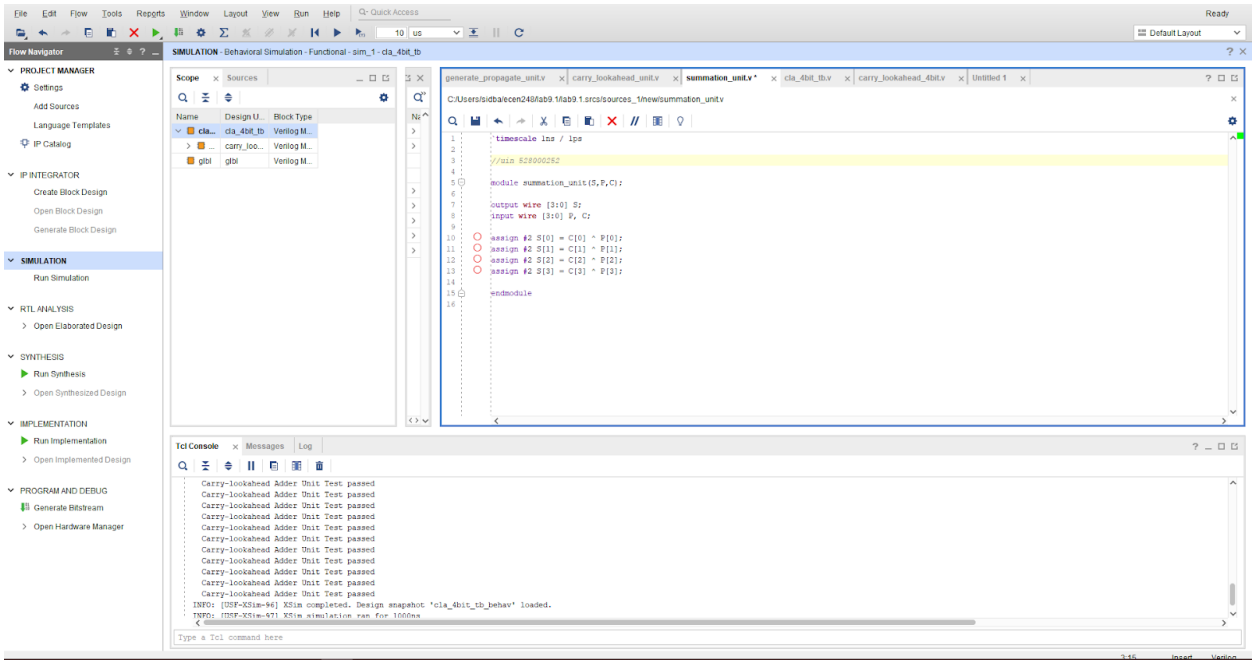
GPU



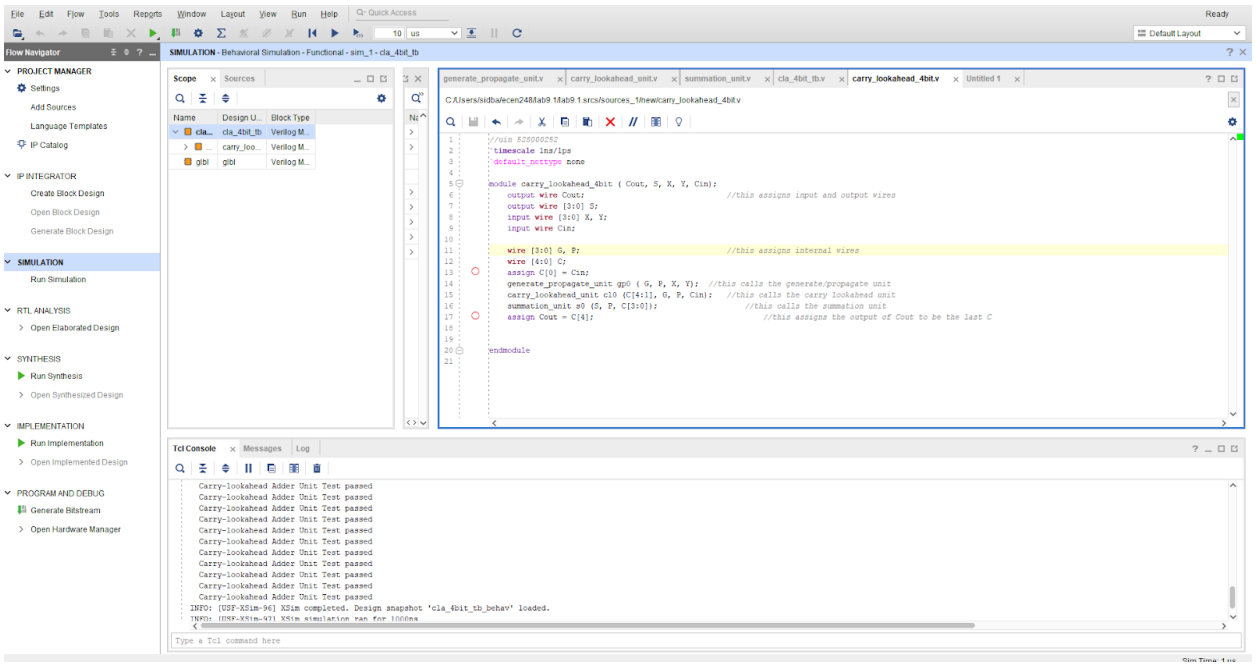
CLU



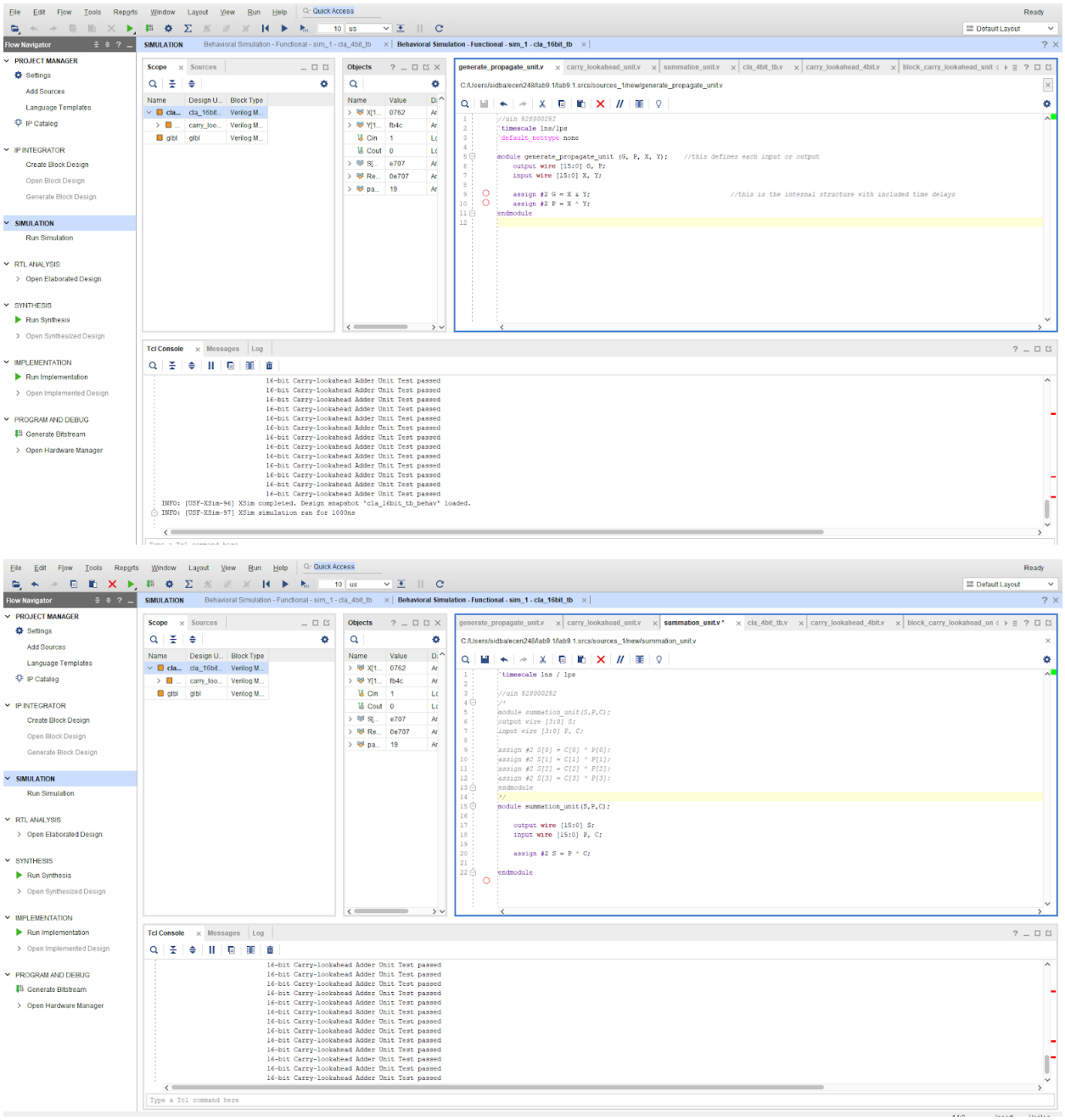
SU



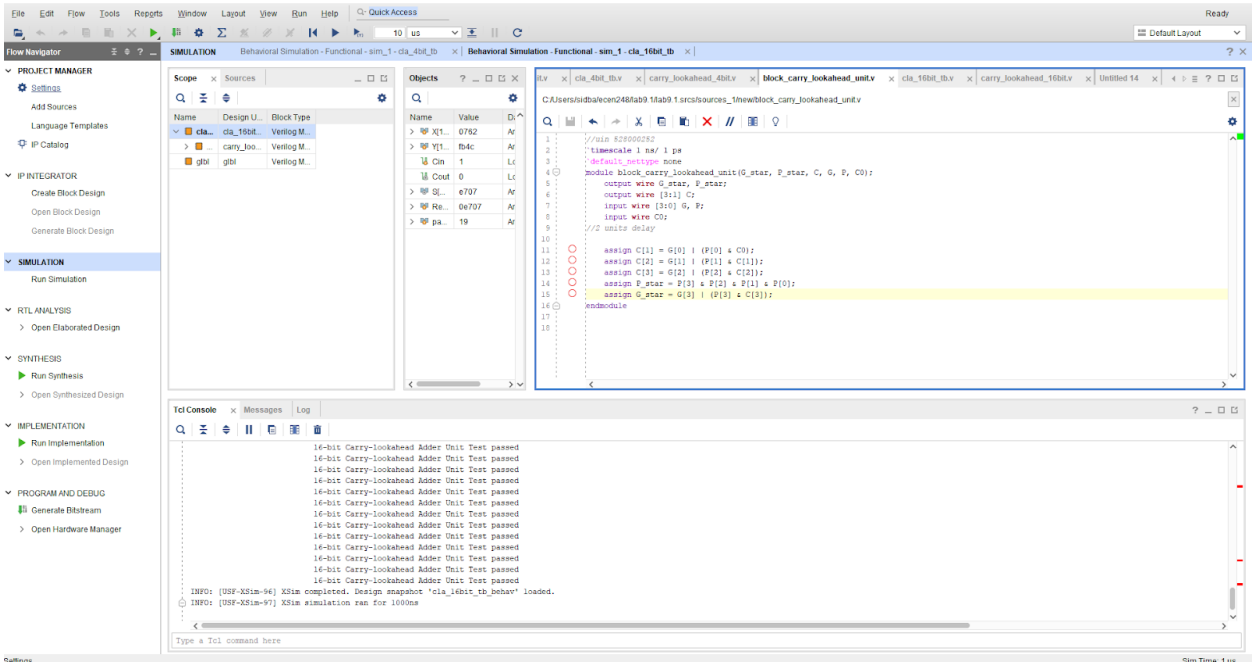
Cla_4bit



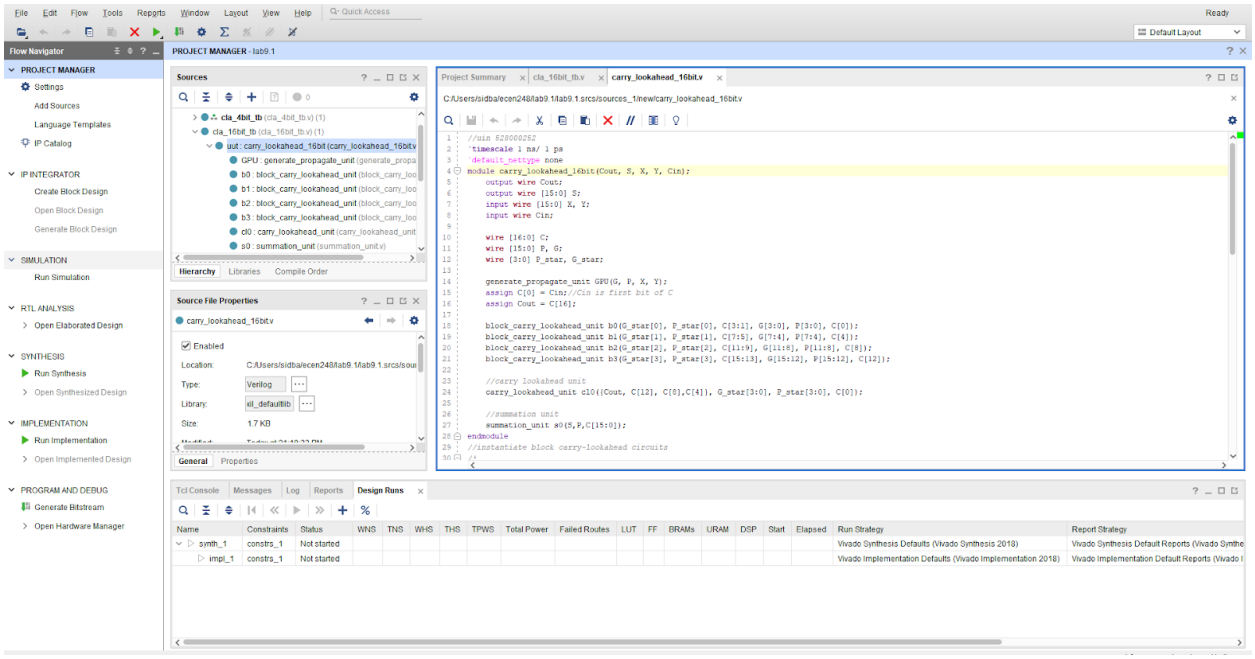
GPU/SU - 16bit



Block carry-lookahead

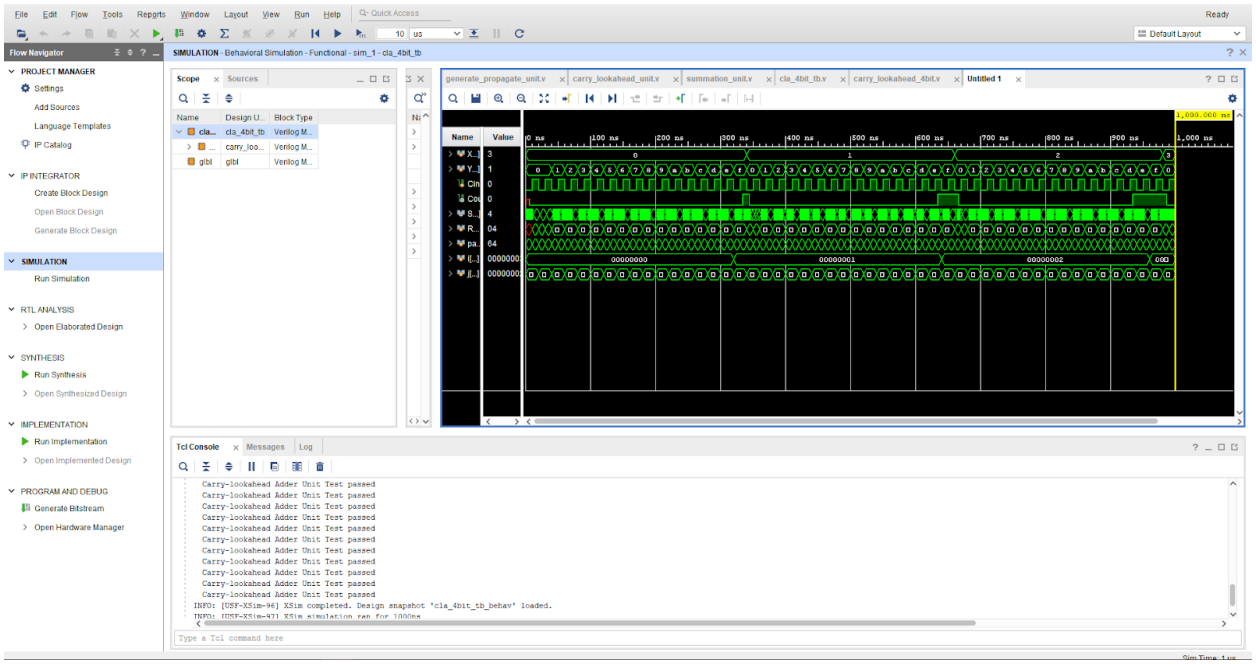


Cla_16bit

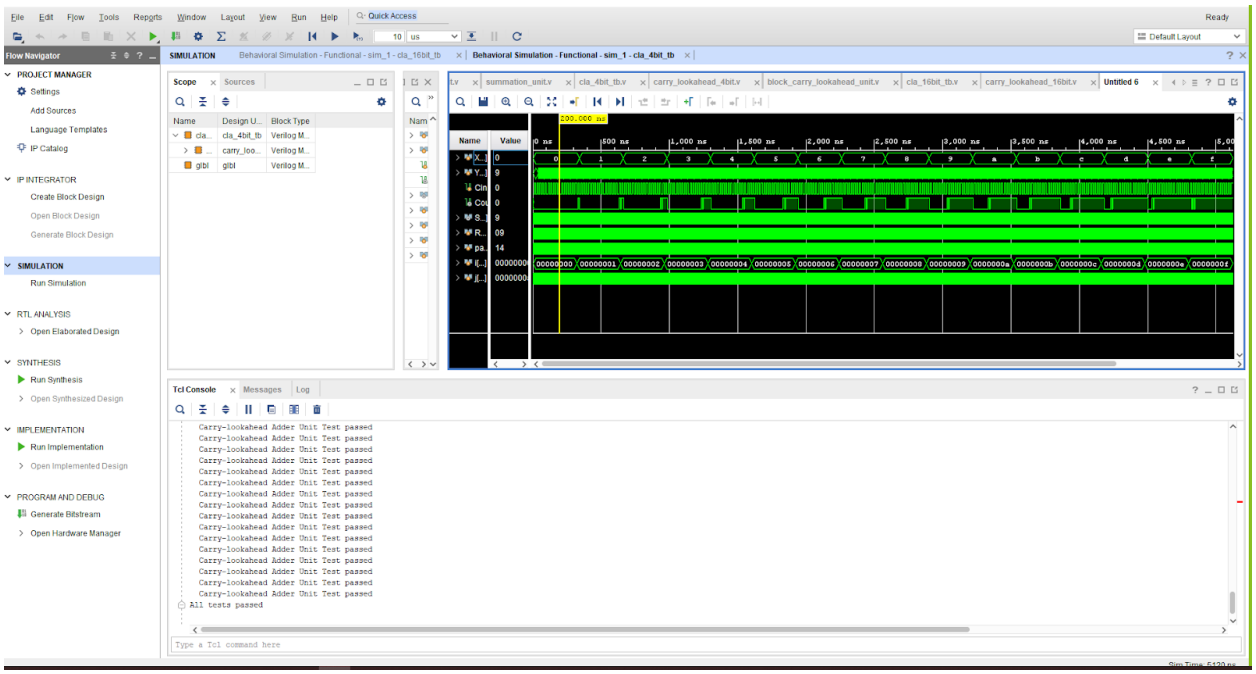


Results

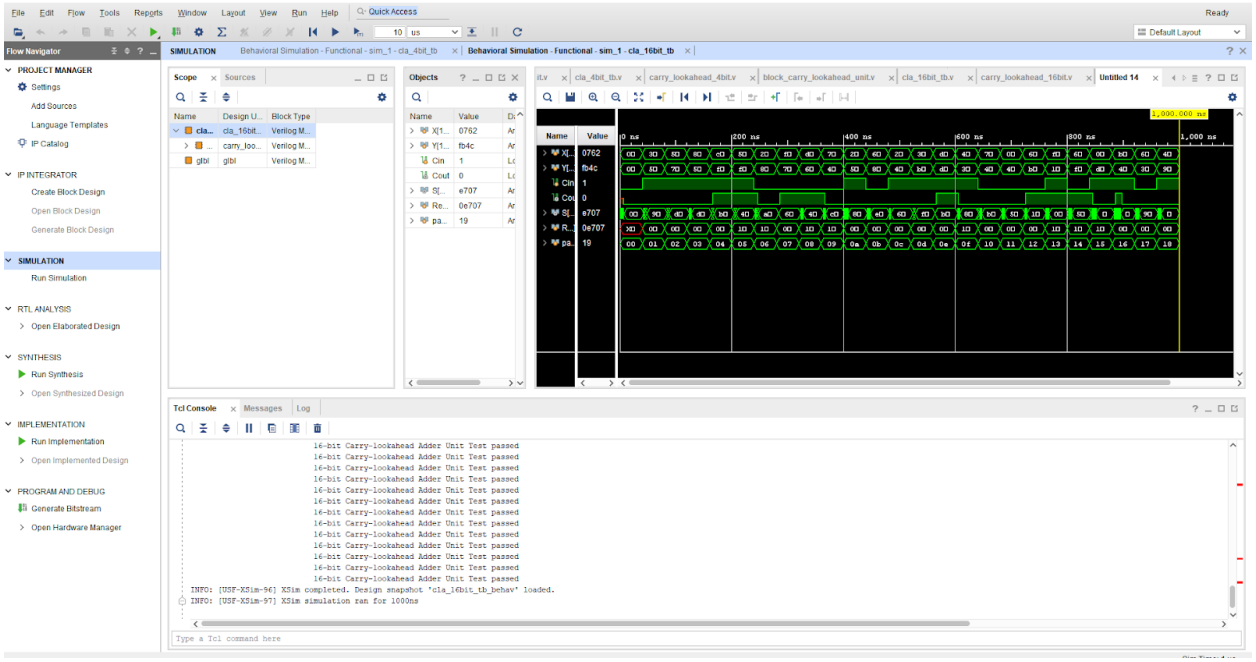
Cla_4bit



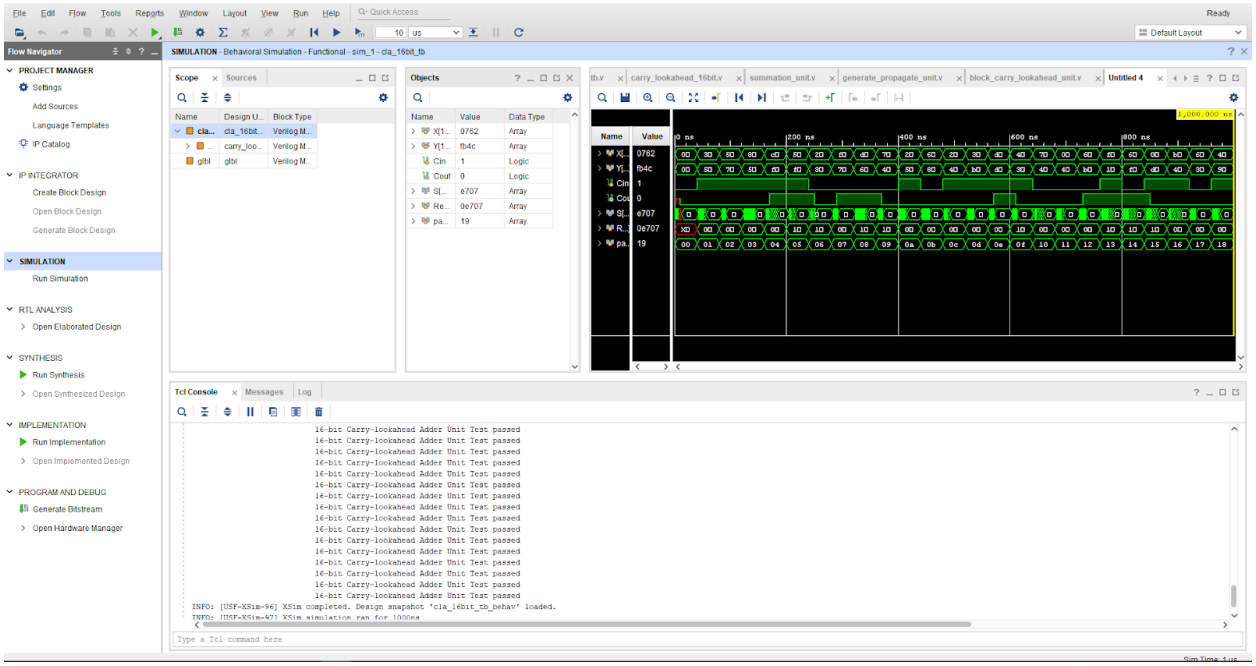
Cla_4bit time delay



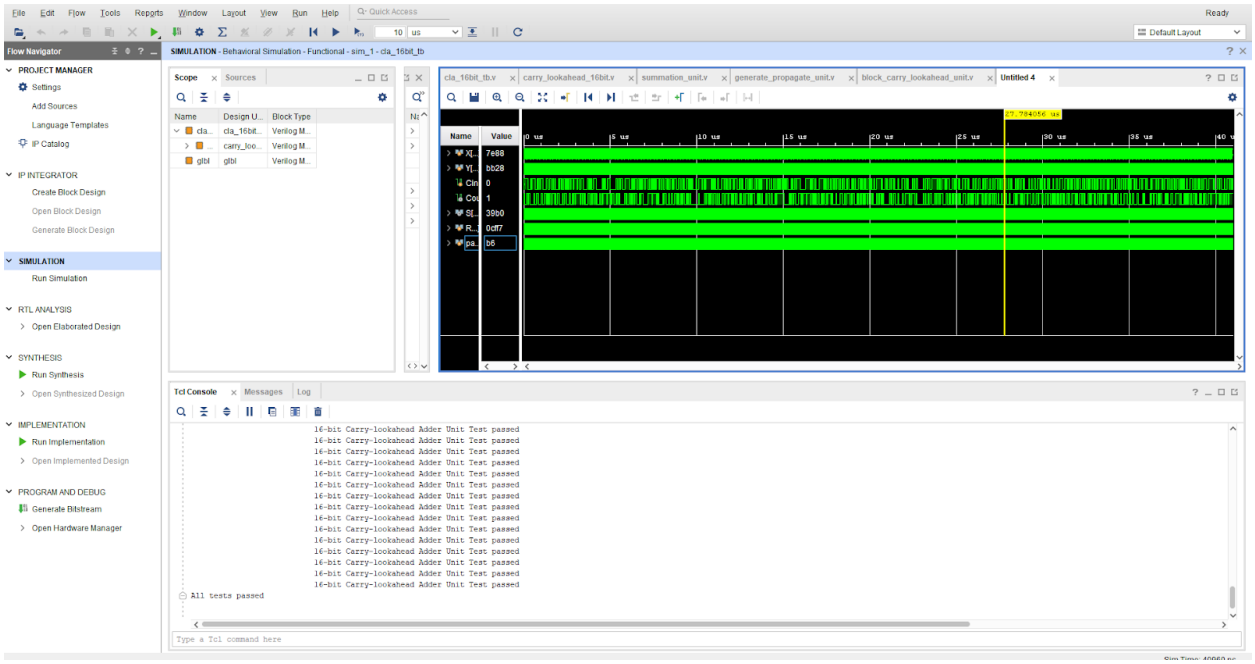
Cla_16bit



Cla_16bit time delay



16bit test case



Conclusion

The goal of this lab was to introduce a fast adder circuit for two-operand addition, which is the carry-lookahead addition. I learned how to design necessary components using data flow and structural Verilog and simulated the results via waveforms. I was able to comprehend a faster concept on adders through the lookahead.

Post - Lab Questions

1. Include the source code with comments for all modules in the lab. You do not have to include a test bench code. The code without comments will not be accepted!

In the design section.

2. Include the simulation screenshots requested in the above experiments in addition to the corresponding test bench console output.

In the results section.

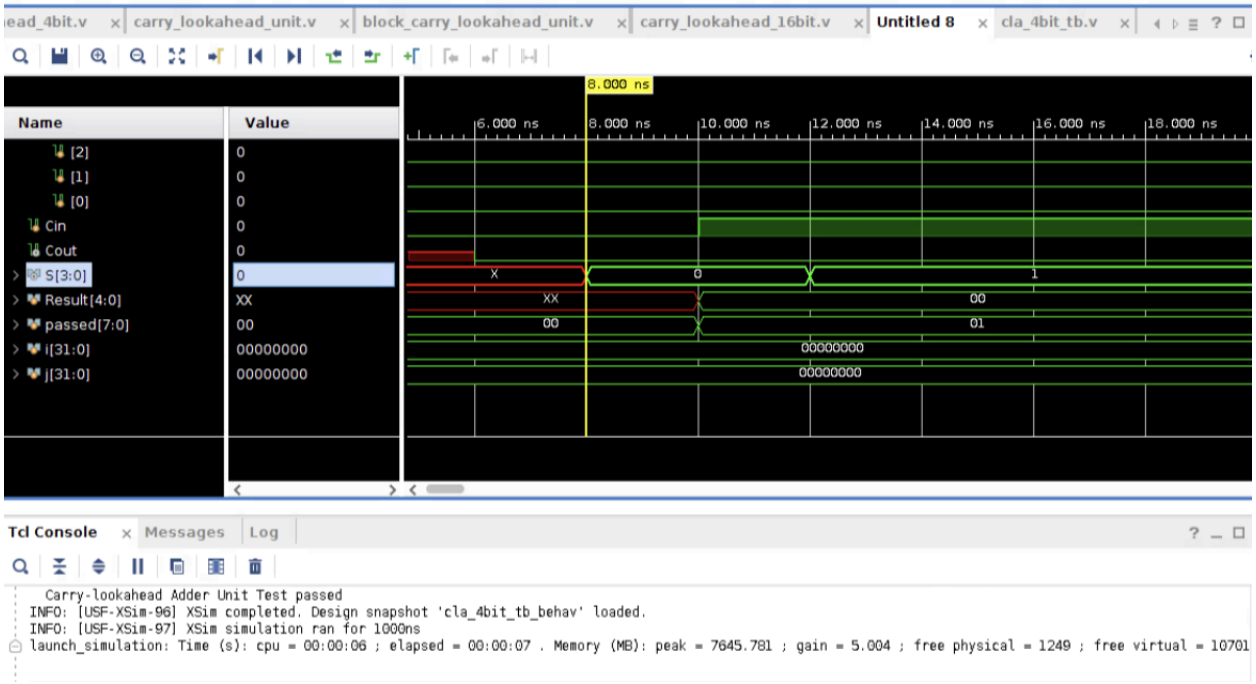
3. What is the gate-count of your 4-bit carry-lookahead adder?

The gate count is 26 gates.

4. What is the propagation delay of the 16-bit, 2-level carry-lookahead adder in Figure 2? Likewise, what is the gate-count?

The propagation delay of the 16-bit is 16 ns, a 2-level carry-lookahead adder is 8 gates with a gate count of 82.

5. With our 4-bit carry-lookahead adder working properly, re-simulate the test bench and measure the propagation delay with the markers in the waveform viewer built into Vivado. The propagation delay does not end with the generation of the carries!



6. If your calculations in the prelab are correct and you correctly added delays to your sub-modules, you should find that the computed delay matches the measured delay. Is this the case?

I calculated delta-g to be 2 ns and that the coefficient was 8. Hence, the time delay of 16 ns in prelab was what it showed on the circuit.

7. How does the gate-count of the 16-bit carry-lookahead adder compare to that of a ripple-carry adder of the same size?

The 16-bit carry look-ahead adder has 82 gates while a 16-bit ripple carry adder has about 80 gates. The number of gates is around the same, but the 16-bit carry look-ahead adder has the ripple-carry adder, and the carry look-ahead works at a higher speed.

8. How does the propagation delay of the 4-bit carry-lookahead adder compare to that of a ripple-carry adder of the same size. Similarly, how does the 16-bit carry-lookahead adder compare to that of a ripple-carry adder of the same size?

The propagation delay is $3\Delta_g$ for the 4-bit carry-lookahead adder. The propagation delay is $9\Delta_g$, for a 4-bit ripple carry. For the 16-bit carry look-ahead adder, there is a delay of 8 and for the 16-bit ripple carry adder it is 33. The carry look-ahead adder has a small delay in most instances because it works much faster than the ripple carry adder.

Feedback

1. I liked the clear instructions on how to code the look ahead units. I did not like the lack of instructions on creating a GPU, su, etc.
2. The lab manual was pretty clear.
3. I wouldn't change anything about the lab.