Lab 3: Rudimentary Adder Circuits

ECEN 248 - 505

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Objectives

The objective of this lab is to get an understanding of how to design, build, and debug a half-adder, full-adder, and ripple carry adder. There was also an underlying reinforcement about the application of karnaugh maps in terms of large Boolean functions.

Design

Pre-Lab

In the Prelab, we were required to make a truth table, karnaugh map for every output, and a gate-level schematic is created for a half and full adder circuit. For the ripple carry adder circuit, the truth table and gate-level schematic were required.

Experiment 1

The half adder circuit is made on the breadboard using a design from the Prelab. A DIP switch is used to supply input bits, which are A and B, and 2 LEDs that are used to display two output bits, Cout and S.

Half-Adder

Truth Table

X	Y	C_{out}	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Karnaugh Maps

S:

	0	1
0	0	1
1	1	0

C_{out}:

	0	1
0	0	0

1	0	1

Logical Expression

Schematic

Experiment 2

The second experiment was with the Full adder part of the PreLab and required to construct a full adder circuit on the breadboard. The DIP switch supplies the input bits (A, B, and C_{in}), and the two LEDs displayed as the output bits were C_{out}, and S1.

Full Adder

Truth Table

C	X	Y	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Karnaugh Maps

S:

	00	01	11	10
0	0	1	0	1
1	1	0	1	0

C_{out}:

	00	01	11	10
0	0	0	1	0
1	0	1	1	1

Logical Expression

Schematic

Experiment 3

For experiment 3, the carry ripple adder design from the PreLab is used to design the carry ripple adder on the breadboard. The DIP switch supplies the input bits (A1, A0, B1, and B0) and the 3 LEDs display the output bits which are S0, S1, and C_{out}.

Truth Table

A0	B0	A1	B1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

C_{in}=0

S0	S1	C_{out}
0	0	0
0	1	0
0	1	0
0	0	1
1	0	0
1	1	0
1	1	0
1	0	1
1	0	0
1	1	0
1	1	0
1	0	1
0	1	1
0	0	1
0	0	1
0	1	1

C_{in}=1

S0	S1	C_{out}
1	0	0
1	1	0
1	1	0
1	0	1
0	1	0
0	0	1
0	0	1
0	1	1
0	1	0
0	0	1
0	0	1
0	1	1
1	1	0
1	0	1
1	0	1
1	1	1

Schematic

Result

The lab was designed for the student to gain hands-on experience with half adders, full adders, and carry ripple adders, hence there are no data points or abnormalities with the execution. While building it took a few attempts, there's just a bunch of test cases to get by in order to determine if one's execution is accurate, otherwise, they may have to debug. Therefore, while there are no concrete deliverables, it did help students understand the function of the different adders and learn how to debug their own gate-level circuits.

Conclusion

This experiment had no concrete outputs or readings to present, just test cases to determine if the right LEDs turn on. This gave me the hands-on experience to apply everything I've learned during lectures, getting a deeper-rooted understanding about the different kinds of adders. Being organized for this lab when the building was necessary because it required so many jumper wires, and could often become very confusing as it progresses. Being organized also helps with debugging. Some helpful techniques is using specific colored wires for a purpose to know where to debug. The lab did get tedious with the amount of equipment being used but the results at the end was satisfying as well.

Post - Lab Questions

1. Provide all design items found in the pre-lab deliverables. If you found that the design needed corrections while executing the lab, supply the updated version of that material.

The design items from the prelab are done is the Design section of the lab report.

2. Determine the worst-case propagation delay for your full adder design. Assume each gate has the same delay of 1 unit. Show the maximum delay path in your schematic. The maximum delay path is known as the critical path for that particular combinational block.

The worst case propagation delay for the adder circuit occurs when the input bits go through the ma number of gates prior to the output bits being generated.

The thicker lines demonstrate the pathway:

3. Design a 2-bit carry ripple adder assuming you only have half adder circuits and OR gates to work with. Draw up a schematic for your design using half adder building blocks and OR gates. Be sure the clearly label all inputs and outputs of your blocks.

There are 4 half adders, 2 OR gates, and a 2 bit carry ripple adder.

Feedback

1. What did you like most about the lab assignment and why? What did you like least about it and why?

Overall, I enjoyed building the full adders and carry ripple adders, seeing the results after days of trial was quite satisying. I personally am a visual learner, so seeing more diagrams and demonstration videos particularly help me while conducting these experiments at home, and I wish the video was a little more clear to follow,

2. Were there any section of the lab manual that were unclear? If so, what was unclear? Do you have any suggestions for improving clarity?

The instructions of the lab were straightforward, and the instructions were clearly written in terms of understanding the goal of the experiment.

3. What suggestions do you have to improve the overall lab assignment?

A suggestion I would make for future experiments is a clearer video of how to do the initial parts of the procedure, so it doesn't take away so much time nor gets frustrating.