Esha Adhawade

Lab 3: Cell Characterization using Spectre

ECEN 454 - 503

October 2, 2022

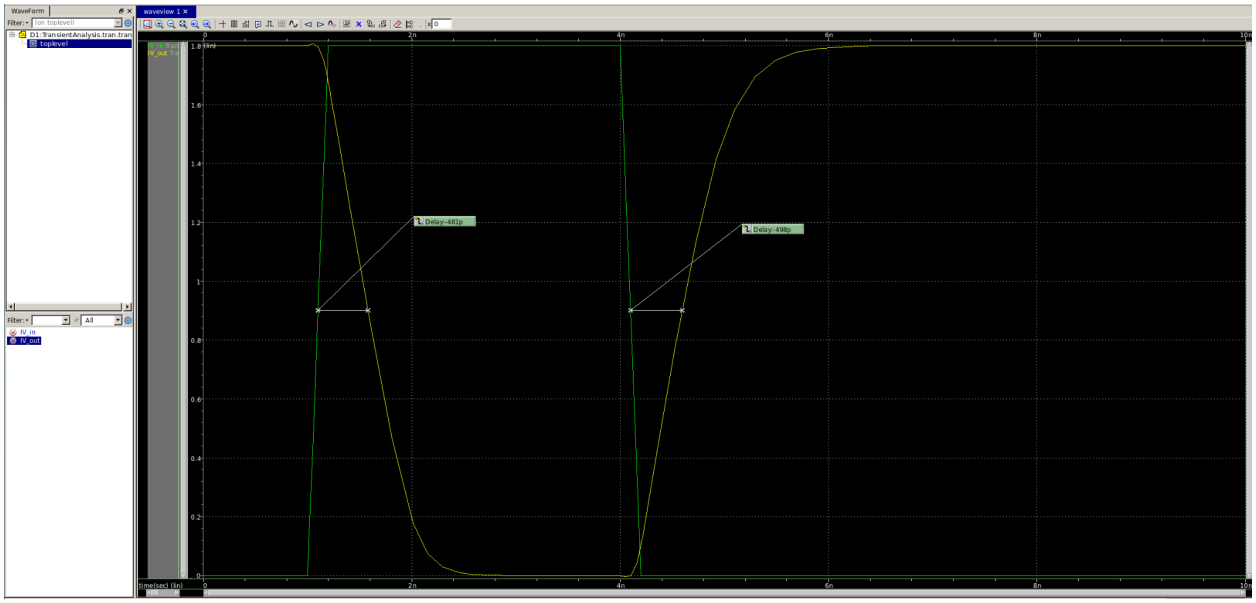
Introduction

The purpose of this lab was to characterize standard cells while gaining familiarity with using Spectre.

Result

Inverter

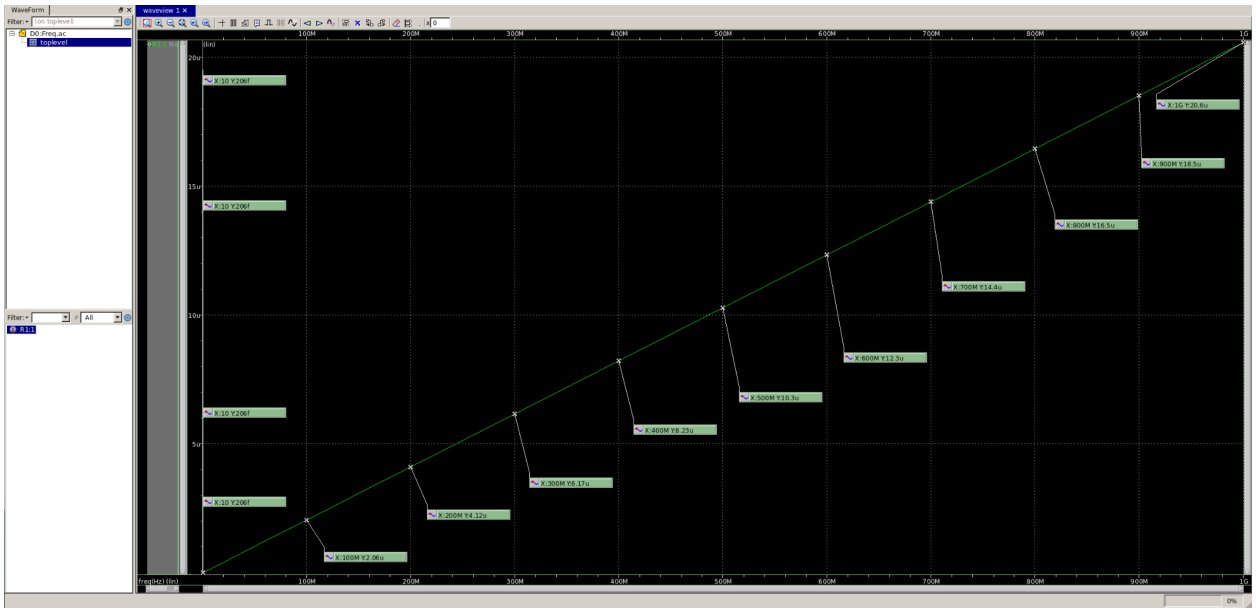
Time Delay Waveform



Delay Table

Capacitance (fF)	Rising Delay (ps)	Falling Delay (ps)	Error (% Difference)
1	27.1	45.2	66.79
5	57.7	74.5	29.12
10	85.8	101	17.72
20	131	144	9.92
25	153	166	8.50
30	175	188	7.43
40	219	232	5.94
50	262	277	5.73
60	306	321	4.90
70	351	368	4.84
75	372	389	4.57
80	393	410	4.33
85	416	430	3.37
90	439	451	2.73
100	481	498	3.53

Sink Capacitance



Sink Capacitance Table (Sink Capacitance: 3.275fF)

Frequency (MHz)	Ifrequency (uA)	Capacitance (fF)
100	2.06	3.279
200	4.12	3.279
300	6.17	3.273
400	8.23	3.275
500	10.3	3.279
600	12.3	3.263
700	14.4	3.274
800	16.5	3.283
900	18.5	3.272
1G	20.6	3.279

Inverter.spi

```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.6u lp=0.2u wn=0.3u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

InverterDelayTable.spi

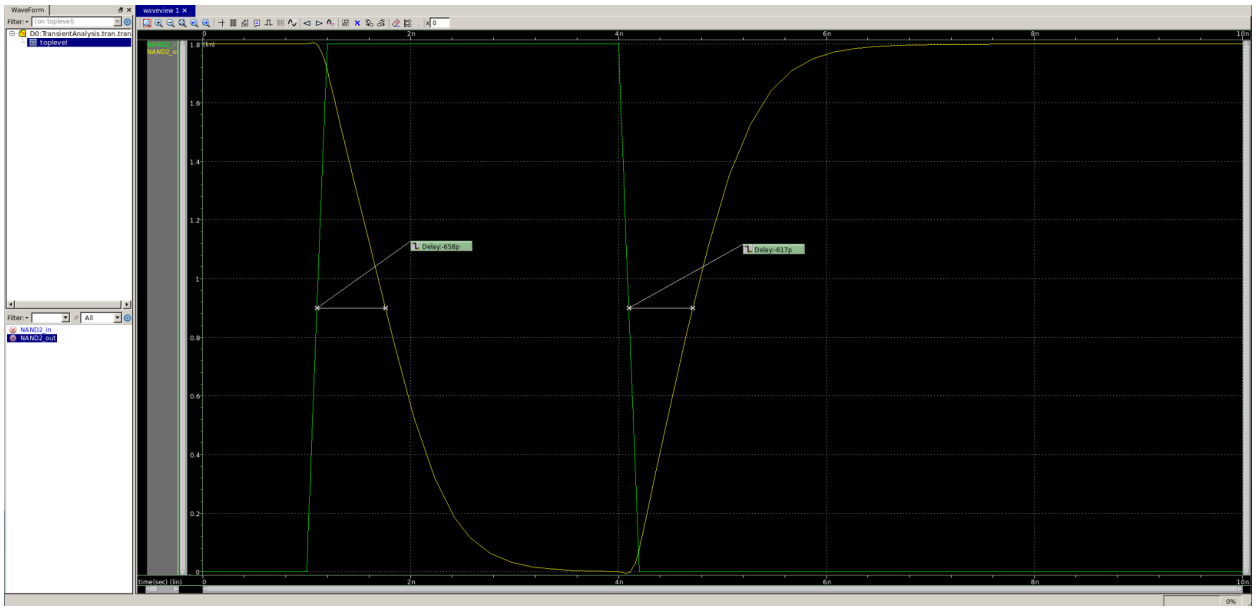
```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

;R1 (IV_out 1) resistor r=1
C1 (IV_out 0) capacitor c=1f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

Simcap.spi

```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (IV_in 0) vsource dc=0 mag=1

R1 (IV_in IV_in1) resistor r=0

X1 (IV_in1 IV_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.4u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

NAND

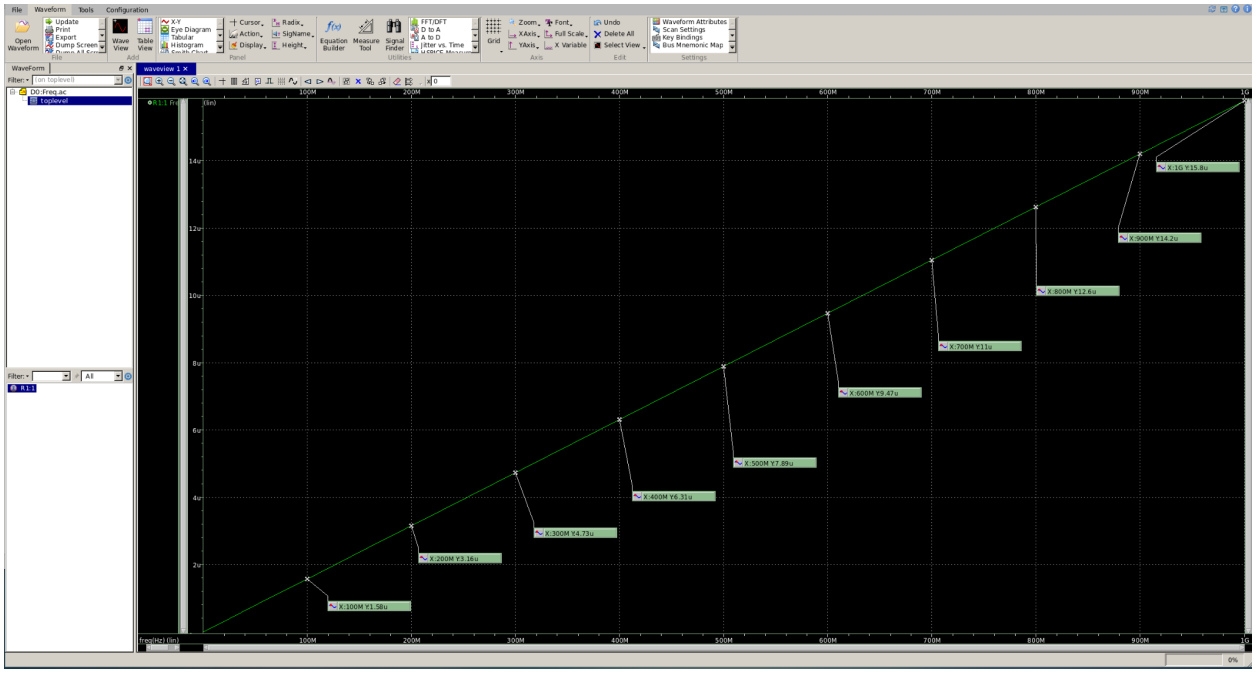
Time Delay Waveform



Delay Table

Capacitance (fF)	Rising Delay (ps)	Falling Delay (ps)	Error (% Difference)
1	38.6	54.9	42.23
5	74.8	87.2	16.58
10	109	116	6.42
20	170	172	1.18
25	200	200	0.00
30	232	227	2.20
40	293	284	3.13
50	353	341	3.52
60	416	395	5.32
70	476	451	5.54
75	506	478	5.86
80	536	505	6.14
85	567	535	5.98
90	598	562	6.41
100	658	617	6.65

Sink Capacitance



Sink Capacitance Table (Sink Capacitance: 2.511fF)

Frequency (MHz)	Ifrequency (uA)	Capacitance (fF)
100	1.58	2.515
200	3.16	2.515
300	4.73	2.509
400	6.31	2.511
500	7.89	2.511
600	9.47	2.512
700	11	2.501
800	12.6	2.507
900	14.2	2.511
1G	15.8	2.515

NAND.spi

```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (NAND2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (NAND2_in vdd NAND2_out vdd gnd) NAND2 wp=0.7u lp=0.2u wn=0.3u ln=0.2u

R1 (NAND2_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save NAND2_in NAND2_out
```

NANDDelayTable.spi

NAND2.spi × *NAND2_dela

```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (NAND2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (NAND2_in vdd NAND2_out vdd gnd) NAND2 wp=0.7u lp=0.2u wn=0.3u ln=0.2u

;R1 (NAND2_out 1) resistor r=1
C1 (NAND2_out 0) capacitor c=1f

TransientAnalysis tran start=0 stop=10ns step=1ps
save NAND2_in NAND2_out
```

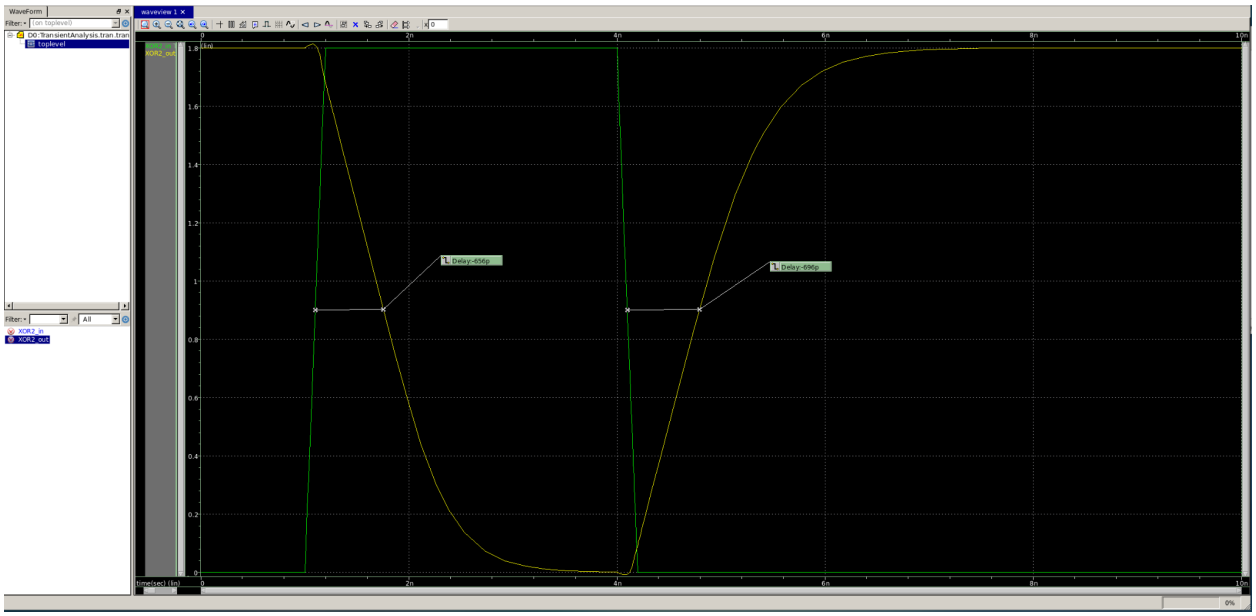
Simcap.spi

NAND2.spi × *NAND2_delaytable.spi × *simca

```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (NAND2_in 0) vsource dc=0 mag=1

R1 (NAND2_in NAND2_in1) resistor r=0

X1 (NAND2_in1 vdd NAND2_out vdd gnd) NAND2 wp=0.7u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

XOR

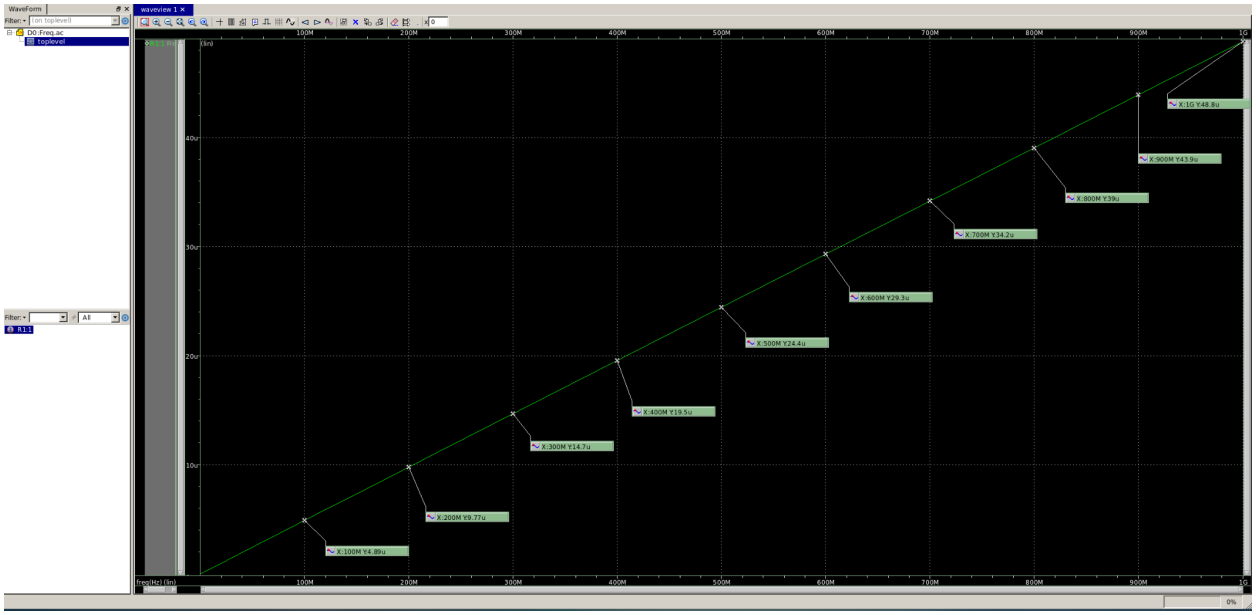
Time Delay Waveform



Delay Table

Capacitance (fF)	Rising Delay (ps)	Falling Delay (ps)	Error (% Difference)
1	41.3	51.3	24.21
5	70.4	81.7	16.051
10	103	117	13.59
20	166	182	9.64
25	197	214	8.63
30	228	247	8.33
40	290	311	7.24
50	351	374	6.55
60	412	441	7.04
70	473	503	6.34
75	504	537	6.55
80	535	569	6.36
85	566	599	5.83
90	596	633	6.21
100	656	696	6.10

Sink Capacitance



Sink Capacitance Table **(Sink Capacitance: 7.772fF)**

Frequency (MHz)	Ifrequency (uA)	Capacitance (fF)
100	4.89	7.783
200	9.77	7.775
300	14.7	7.799
400	19.5	7.759
500	24.4	7.767
600	29.3	7.772
700	34.2	7.776
800	39	7.759
900	43.9	7.763
1G	48.8	7.767

XOR.spi

```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XOR2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XOR2_in vdd XOR2_out vdd gnd) XOR2 wp=1.2u lp=0.2u wn=0.3u ln=0.2u

R1 (XOR2_out 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XOR2_in XOR2_out
```

XORDelayTable.spi

```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XOR2_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XOR2_in vdd XOR2_out vdd gnd) XOR2 wp=1.2u lp=0.2u wn=0.3u ln=0.2u

;R1 (XOR2_out 1) resistor r=1
C1 (XOR2_out 0) capacitor c=1f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XOR2_in XOR2_out
```

Simcap.spi

*XOR2_delaytable.spi ×

```
;Spice netlist for an inverter and a capacitor
;UIN 528000252
simulator lang=spectre

include "~/ecen454_503/cellcharacs/model18.spi"
include "~/ecen454_503/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

acinput (XOR2_in 0) vsource dc=0 mag=1

R1 (XOR2_in XOR2_in1) resistor r=0

X1 (XOR2_in1 vdd XOR2_out vdd gnd) XOR2 wp=1.2u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9
save R1:currents
```

Cell18.spi

File Edit Options Buffers Tools Help

Save Undo

```
//Spice netlist for an inverter
//UIN 528000252

simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV


subckt NAND2 (A B output VDD VSS)
       parameters wp=0.7u lp=0.2u wn=0.3u ln=0.3u

       //pmos
       M1 output A VDD VDD tsmc18P w=wp l=lp
       M2 output B VDD VDD tsmc18P w=wp l=lp

       //nmos
       M3 output A n_wire VSS tsmc18N w=wn l=ln
       M4 n_wire B VSS VSS tsmc18N w=wn l=ln

ends NAND2


subckt XOR2 (A B output VDD VSS)
       parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u

       //pmos
       M1 p_wire1 B VDD VDD tsmc18P w=wp l=lp
       M2 output A_inv p_wire1 VDD tsmc18P w=wp l=lp

       M3 p_wire2 B_inv VDD VDD tsmc18P w=wp l=lp
       M4 output A p_wire2 VDD tsmc18P w=wp l=lp

       //nmos
       M5 output A_inv n_wire1 VSS tsmc18N w=wn l=ln
       M6 n_wire1 B_inv VSS VSS tsmc18N w=wn l=ln

       M7 output A n_wire2 VSS tsmc18N w=wn l=ln
       M8 n_wire2 B VSS VSS tsmc18N w=wn l=ln

       //Inverter A
       M9 A_inv A VDD VDD tsmc18P w=wp l=lp
       M10 A_inv A VSS VSS tsmc18N w=wn l=ln

       //Inverse B
       M11 B_inv B VDD VDD tsmc18P w=wp l=lp
       M12 B_inv B VSS VSS tsmc18N w=wn l=ln

ends XOR2
```