Lab 2-Prelab: Logic Minimization with Karnaugh Maps

ECEN 248 - 505

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1. Truth table for profit calculator.

	C	H	I	S	P2	P1	P0
0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0
2	0	0	1	0	0	0	1
3	0	0	1	1	0	1	1
4	0	1	0	0	0	1	1
5	0	1	0	1	1	0	1
6	0	1	1	0	0	1	1
7	0	1	1	1	1	0	1
8	1	0	0	0	1	0	0
9	1	0	0	1	1	1	1
10	1	0	1	0	0	1	1
11	1	0	1	1	0	1	1
12	1	1	0	0	1	1	1
13	1	1	0	1	1	0	1
14	1	1	1	0	0	1	1
15	1	1	1	1	1	1	1

2. Karnaugh Maps for each of the output bits, P2, P1, P0.

P0:

	00	01	11	10
00	0	0	1	1
01	1	1	1	1
11	1	1	1	1
10	0	1	1	1

P1:

	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	1	0	1	1
10	0	1	1	1

P2:

	00	01	11	10
00	0	0	0	0
01	0	1	1	0
11	1	1	1	0
10	1	1	0	0

3. Minimized boolean algebra expression in terms of input bits (I, S, C, and H) for each output bit.

4. Gate level schematic of your profit calculator which includes DIP switches and LED