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Lab 9: Optimization using Logical Effort

ECEN 454 - 503

November 16, 2022

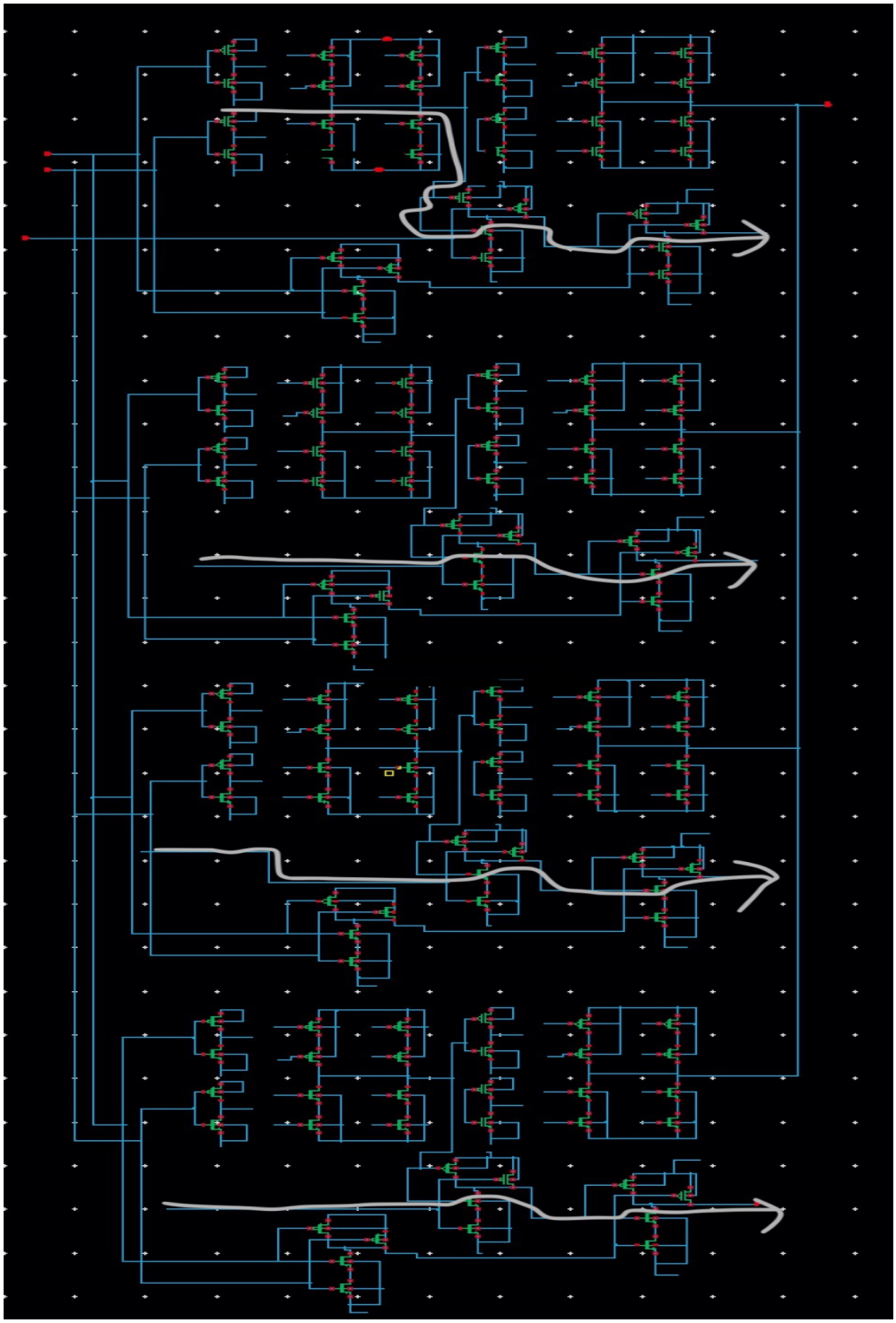
Introduction

Build 4bit adder and reduce delay using different techniques.

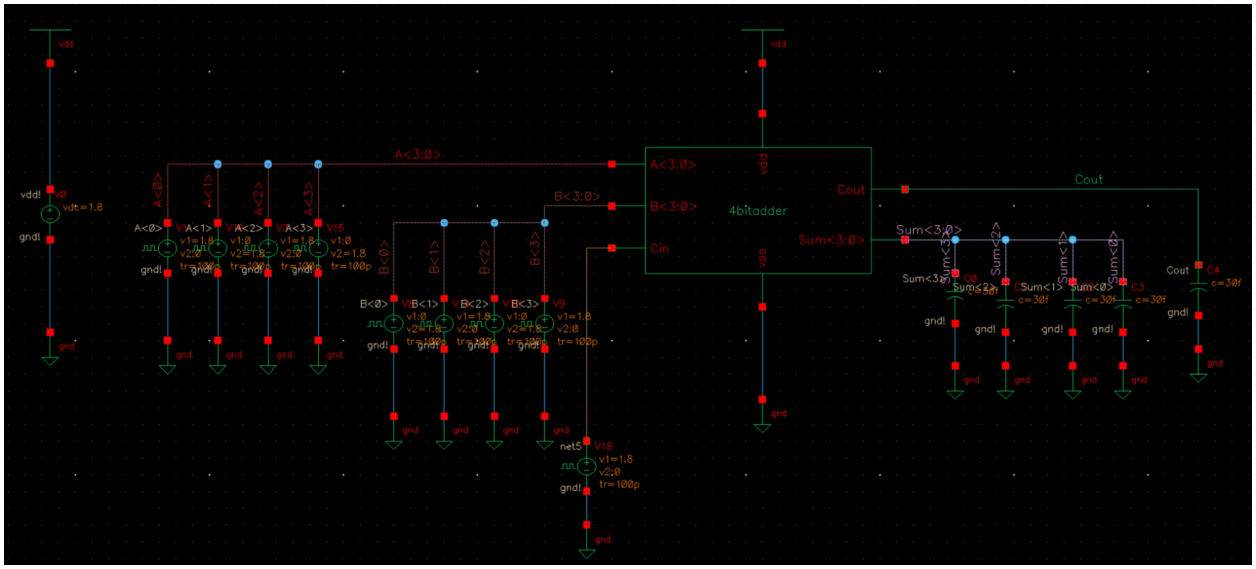
Result

Schematics

Schematic

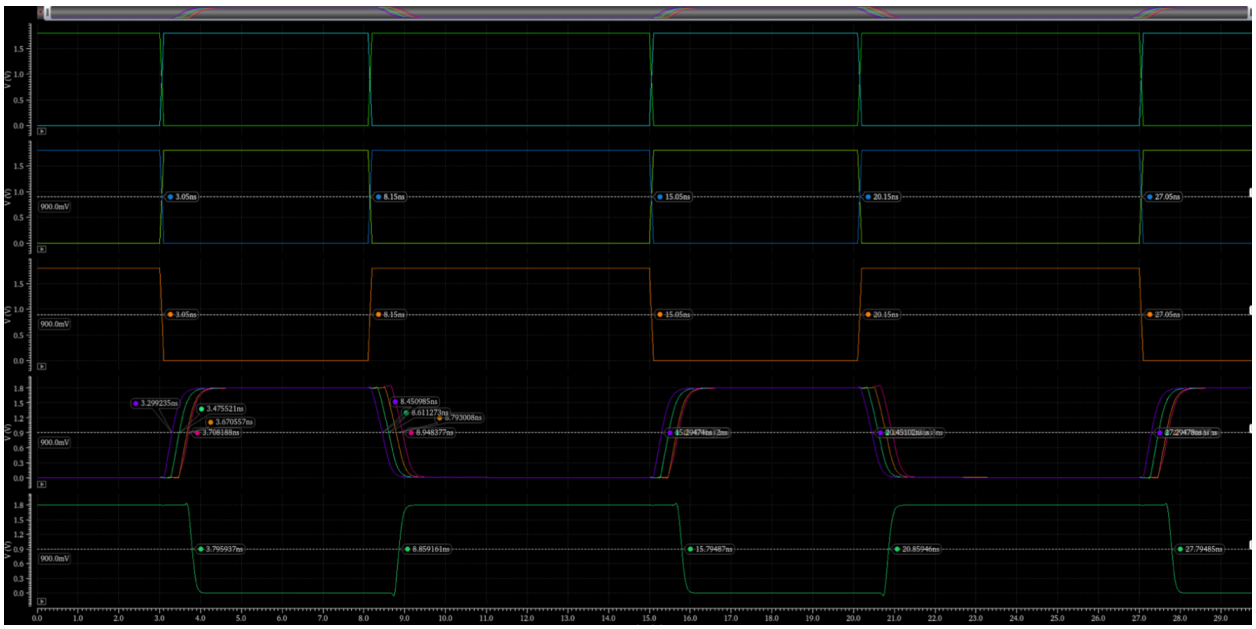


Simulation Schematic



Waveforms before Optimization

Waveform (A = 0000, B = 1111, C = 1)



Delay

	Delay
S0	270.13
S1	442.5
S2	631.23

S3	730.40
Cout	775.4

Waveform (A = 1010, B = 0101, C = 0)

Delay

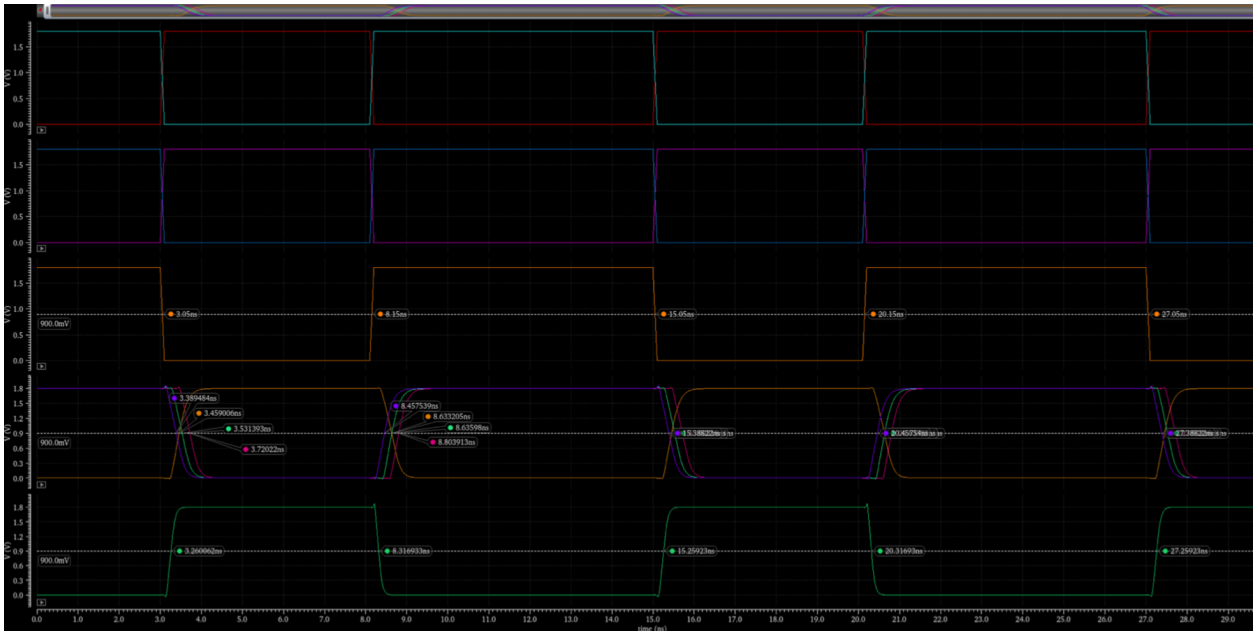
	Delay
S0	275.11
S1	443.4
S2	631.8
S3	728.3
Cout	727.5

Waveform (A = 1010, B = 0101, C = 1)

Delay

	Delay
S0	270.11
S1	443.1
S2	631.7
S3	714.4
Cout	731.5

Waveform (A = 1100, B = 1000, C = 0)



Delay

	Delay
S0	323.5
S1	446.1
S2	483.7
S3	662.4
Cout	188.5

Calculations

Power before optimization

Case	Power (uW)
1	141.9
2	152.7
3	142.7
4	151.9

Logical Effort Calculation

Critical path : XOR11 – NAND11 – NAND12–NAND21 – NAND22 – NAND31 – NAND32 – NAND41 – NAND42 (From the Schematic)

Here
Number of transistor = 9
F = GBH
G = $\Pi g_i = 4 \times \frac{4}{3} \times \frac{4}{3} \times \frac{4}{3} \times \frac{4}{3} \times \frac{4}{3} \times \frac{4}{3} \times \frac{4}{3} \times \frac{4}{3} = \frac{4^9}{3^8}$

H = $\frac{C_{load}}{C_{xor}} = \frac{30}{4.46} = 6.726$
Now for B we have
$B = \Pi b_i$
And we Know
$b_i = \frac{C_{on-path}+C_{off-path}}{C_{on-path}}$

Again
$b_1 = \frac{C_{XOR}+C_{NAND}}{C_{NAND}} = \frac{4.46-3.25}{3.25} = 2.37$
$b_2 = b_4 = b_6 = b_8 = b_9 = 1$
$b_3 = b_5 = b_7 = b_1 = 2.37$

For all
B = $2.37^4 \times 1^5 = 31.55$

Now
F = $BGH = 31.55 \times 6.725 \times \frac{4^9}{3^8} = 8478.52$
And
$\hat{f} = F^{\frac{1}{N}} = 8478.52^{\frac{1}{9}} = 2.73$

Sizing Transistors

We have, with $C_{gate} = 4.46$

$C_{in1} = \frac{gC_{out1}}{\hat{f}} = 4 \times \frac{7.71}{2.73} = 11.3 > 4.46$
Sizing Factor = $\frac{11.3}{4.46} = 2.53$

with $C_{gate} = 3.25$

$C_{in2} = \frac{gC_{out2}}{\hat{f}} = \frac{4}{3} \times \frac{3.25}{2.73} = 1.16 < 3.25$
Since $C_{in_2} < C_{gate}$, the sizing factor is not required.

$C_{in3} = \frac{gC_{out3}}{\hat{f}} = \frac{4}{3} \times \frac{7.71}{2.73} = 3.77 > 3.25$
Sizing Factor = $\frac{3.77}{4.46} = 2.53$

$C_{in4} = \frac{gC_{out4}}{\hat{f}} = \frac{4}{3} \times \frac{3.25}{2.73} = 1.16 < 3.25$
Since $C_{in_2} < C_{gate}$, the sizing factor is not required.

$C_{in5} = \frac{gC_{out5}}{\hat{f}} = \frac{4}{3} \times \frac{7.71}{2.73} = 3.77 > 3.25$
Sizing Factor = $\frac{3.77}{4.46} = 2.53$

$C_{in6} = \frac{gC_{out6}}{\hat{f}} = \frac{4}{3} \times \frac{3.25}{2.73} = 1.16 < 3.25$
Since $C_{in_2} < C_{gate}$, the sizing factor is not required.

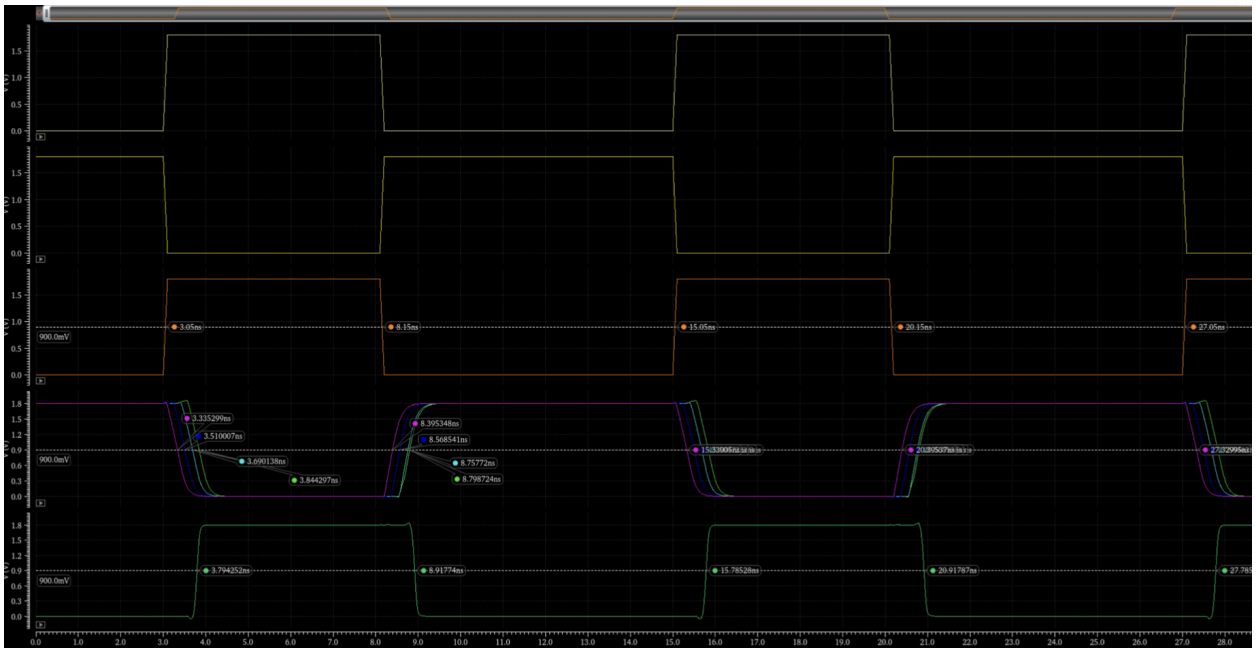
$C_{in7} = \frac{gC_{out7}}{\hat{f}} = \frac{4}{3} \times \frac{7.71}{2.73} = 3.77 > 3.25$
Sizing Factor = $\frac{3.77}{4.46} = 2.53$

$C_{in8} = \frac{gC_{out8}}{\hat{f}} = \frac{4}{3} \times \frac{3.25}{2.73} = 1.16 < 3.25$
Since $C_{in_2} < C_{gate}$, the sizing factor is not required.

$C_{in9} = \frac{gC_{out9}}{\hat{f}} = \frac{4}{3} \times \frac{30}{2.73} = 14.65 > 3.25$
Sizing Factor = $\frac{14.65}{4.46} = 4.5$

Waveforms after Optimization

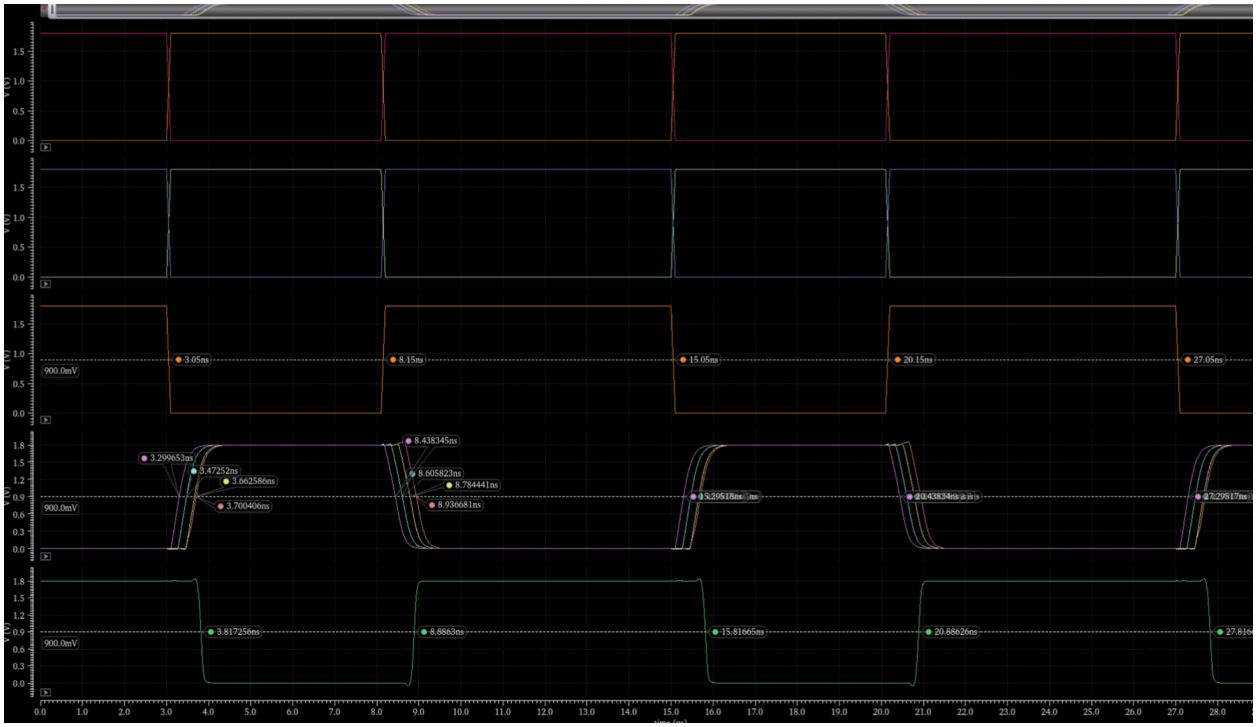
Waveform (A = 0000, B = 1111, C = 1)



Delay

	Delay
S0	265.3
S1	439.3
S2	623.9
S3	721.5
Cout	756.5

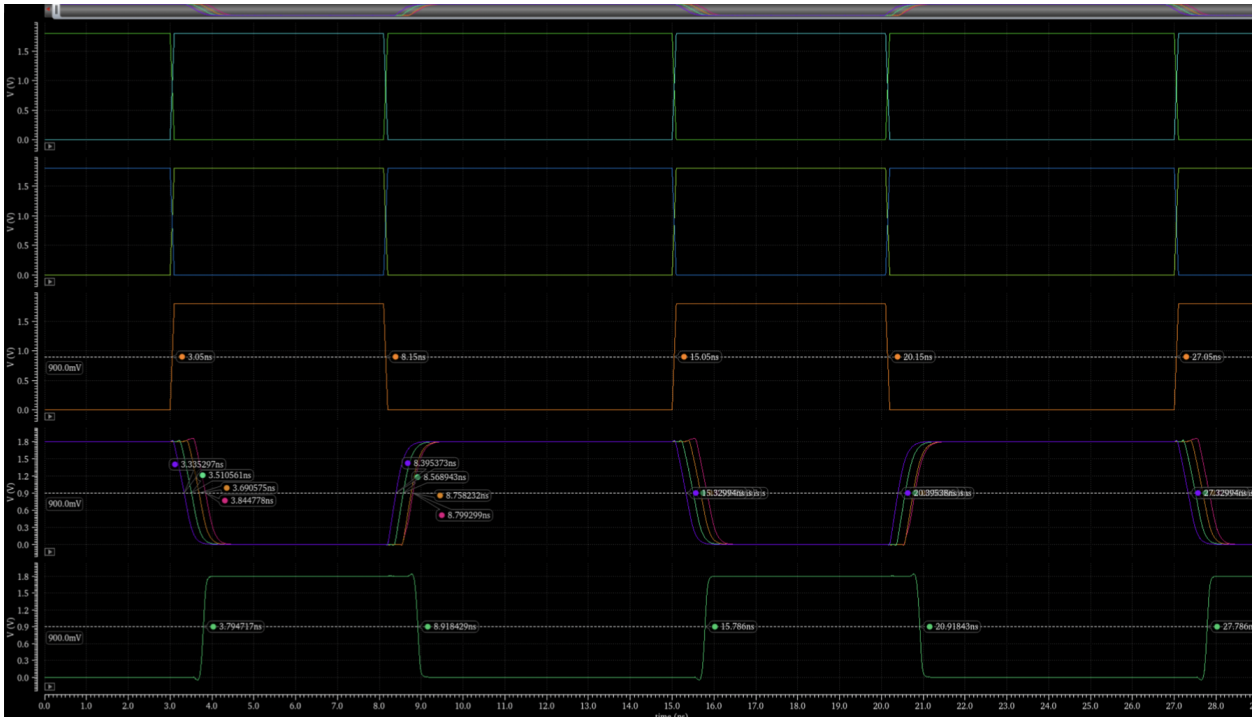
Waveform (A = 1010, B = 0101, C = 0)



Delay

	Delay
S0	269.1
S1	439.1
S2	623.2
S3	719.5
Cout	719.1

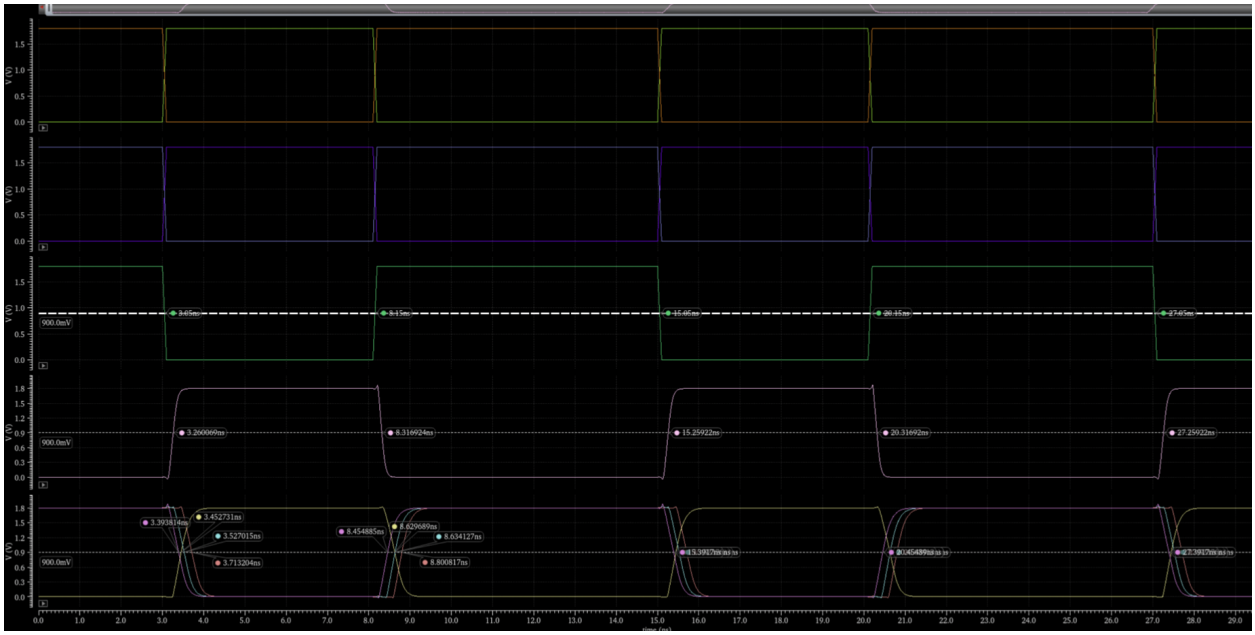
Waveform (A = 1010, B = 0101, C = 1)



Delay

	Delay
S0	265.1
S1	439.7
S2	624.4
S3	723.4
Cout	724.1

Waveform (A = 1100, B = 1000, C = 0)



Delay

	Delay
S0	324.4
S1	441.1
S2	480.5
S3	657.0
Cout	188.4

Calculations

Power after optimization

Case	Power (uW)
1	171.2
2	183.5
3	172.1
4	167.1

Tables

Comparison Table

Delays:

Case	Pin	Non-optimized(ps)	optimized(ps)
A=0000 B=1111 Carry in=1	SUM.0	270.127	265.32
	SUM.1	442.51	439.27
	SUM.2	631.23	623.93
	SUM.3	730.40	721.51
	CARRY	775.37	756.0
A=1010 B=0101 Carry in=0	SUM.0	275.11	269
	SUM.1	443.40	439.17
	SUM.2	631.78	623.51
	SUM.3	728.28	719.89
	CARRY	727.55	719.12
A=1010 B=0101 Carry in=1	SUM.0	270.11	265.34
	SUM.1	442.92	439.75
	SUM.2	631.64	624.00
	SUM.3	714.34	723.46
	CARRY	731.49	724.06
A=1100 B=1000 Carry in=1	SUM.0	323.51	324.35
	SUM.1	446.10	441.21
	SUM.2	483.68	480.57
	SUM.3	668.07	657.01
	CARRY	188.50	188.50

Power Consumption:

case	Optimized(uW)	Non-optimized(uW)
A=0000, B=1111, CarryIn=1	171.2	141.9
A=1010, B=1010, CarryIn=0	183.5	152.7
A=1010, B=0101, CarryIn=1	172.1	142.7
A=1100, B=1000, CarryIn=1	167.1	151.9

Area:

Optimized (u^2m^2)	Non-Optimized (u^2m^2)
37.978	30.24

Area Calculation before Optimization

Stages	XOR1 width	XOR2 width	NAND1 width	NAND2 width	NAND3 width	Total	Area
Stage1	10.2	10.2	5.8	5.8	5.8	37.8	7.56
Stage2	10.2	10.2	5.8	5.8	5.8	37.8	7.56
Stage3	10.2	10.2	5.8	5.8	5.8	37.8	7.56
Stage4	10.2	10.2	5.8	5.8	5.8	37.8	7.56
						Total Area	30.24

Area Calculation after Optimization

Stages	XOR1 width	XOR2 width	NAND1 width	NAND2 width	NAND3 width	Total	Area
Stage1	25.806	10.2	5.8	5.8	6.728	54.334	10.8668
Stage2	10.2	10.2	5.8	5.8	6.728	38.728	7.746
Stage3	10.2	10.2	5.8	5.8	6.728	38.728	7.746
Stage4	10.2	10.2	5.8	5.8	26.1	58.1	11.62
						Total Area	37.978