Lab 4: Simple Arithmetic Logic Unit

ECEN 248 - 505

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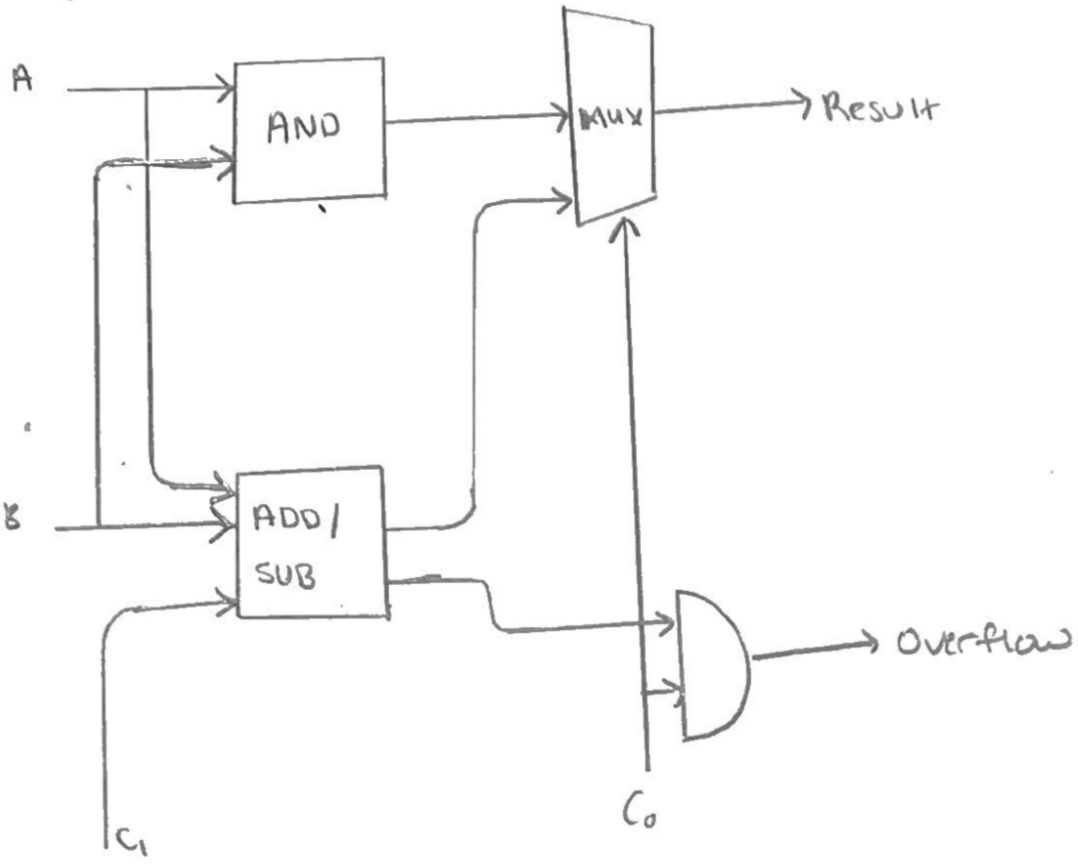
Objectives

The purpose of this lab was for the student to gain an understanding of a simple 4-bit Arithmetic Logic Unit (ALU) and to demonstrate our understanding of a Two's Complement Arithmetic and multiplexors. This is for us to design and implement the tests, which perform addition, subtraction, and bit-wise AND.

Design

The first part of this lab was to test the ADD/ SUB unit which utilizes a ripple carry adder component. There was also a test for a 4-bit 2:1 MUX chip with LEDs to ensure it is working properly.

Design Schematic for ALU



Result

This lab took multiple tries when it came to wiring and using the right logic gates. While performing the lab, I made the mistake of placing AND_0, AND_1, AND_2, and AND_3, in step 5 to R_0, R_1, R_2, and R_3 instead of the and gate. However, in step 6 I quickly learned from that mistake and was able to go back and change that. I also had to determine which IC chip is the output and input. I performed this lab twice since the first time failed, and I learned from my mistakes on the first trial.

Conclusion

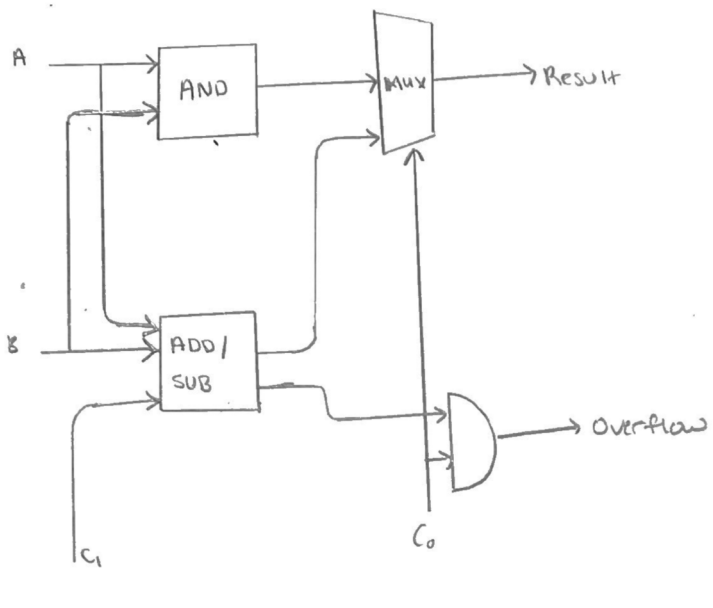
_____In this lab, I successfully learned the importance of powering and grounding the necessary ICs. I gained a very good understanding of a simple 4-but Arithmetic Logic Unit, along with understanding the function s of a Two's Complement Arithmetic and a multiplexor. I also learned that the positioning of wires for this lab-made a difference, hence it took me a few attempts. It was important to place the wires in the right positions, because it also made the organization a lot easier to follow, as it could get confusing at times. It also made debugging a lot more effective, because I know where I had to look for each step. Wiring the ALU was a little bit simpler and it is an essential component of the lab, hence gaining an understanding of it was crucial.

Post - Lab Questions

1. Observe and fill in Table 1. Both A and B are two's complement numbers. The result should be a 4-bit binary number. Determine whether overflow occurs or not.

C_0	C_1	Operation	A	B	Result	Overflow
0	0	AND	0100	0110	0100	0
0	1	AND	0110	1101	0100	0
1	0	ADD	0100	0110	1010	0
1	0	ADD	0100	1101	0001	1
1	0	ADD	1101	1001	0110	1
1	1	SUB	0100	0111	1101	0
1	1	SUB	0110	1001	1101	0

2. Determine the maximum gate delay through your final ALU circuit assuming each gate has a delay of 1 unit. Highlight the critical path on the gate-level schematic.

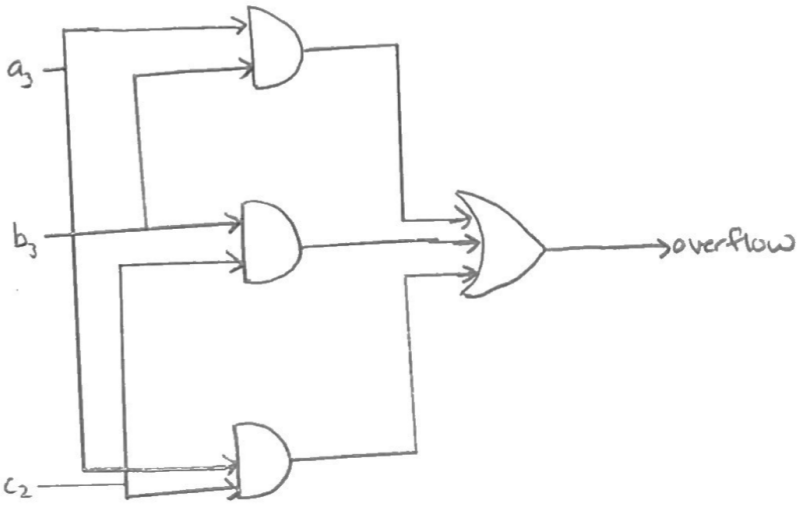


3. Please design the overflow detecting unit in Figure 7. You can use all available signals except the signals inside the chip package. Show your process and draw a gate-level schematic.

a_3	b_3	c_2	overflow
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

c_2 \ a_3b_3	00	01	11	10
0	0	0	1	1
1	0	1	1	1

Overflow $= a_3 b_3 + b_3 c_2 + a_3 c_2$



Feedback

1. What did you like most about the lab assignment and why? What did you like least about it and why?

Overall, I enjoyed working through this lab, seeing the results after many trials were quite satisfying. I am a visual learner, so the demo pdf was very helpful which it came to performing the lab. I just wish there were more test cases for us to follow after each step, so we know if we are doing it correctly on the way.

2. Were there any section of the lab manual that was unclear? If so, what was unclear? Do you have any suggestions for improving clarity?

The instructions of the lab were straightforward, and the instructions were clearly written in terms of understanding the goal of the experiment.

3. What suggestions do you have to improve the overall lab assignment?

A suggestion I would make for future experiments is having more details and test case in the demonstrations, so students can debug as they move on and not just at the end.