Pre-Lab 6: Introduction to Behavioral Verilog and Logic Synthesis

[redacted]

ECEN 248 - 505

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1. Verilog code with comments for the 2:4 binary decoder, the 4:2 binary encoder, and the 4:2 priority encoder. Do not use behavioral Verilog for these descriptions! Use the structural and dataflow concepts introduced in the previous lab.

2:4 Binary decoder

```
module two_four_decoder(
        input wire[1:0] W,
        input wire En,
        output wire [3:0] Y
);
        assign Y[0] = ~W[0] & ~W[1] & En;
        assign Y[1] = ~W[0] & W[1] & En;
        assign Y[2] = W[0] & ~W[1] & En;
        assign Y[3] = W[0] & W[1] & En;
endmodule
```

4:2 Encoder

```
`timescale 1ns / 1ps
module four_two_encoder(
        input wire [3:0] W,
        output wire [1:0] Y,
         output wire zero
);
        assign zero = ~W;
        assign Y[0] = W[1] | W[3];
        assign Y[1] = W[2] | W[3];
endmodule
```

4:2 Priority Encoder

```
`timescale 1ns / 1ps
module priority_encoder(
        input wire [3:0] W,
        output wire [1:0] Y,
        output wire zero
);
        wire [3:0] I;
        assign I[0] = ~W[3]&~W[2]&~W[1]&W[0];
        assign I[1] = ~W[3]&~W[2]&W[1];
        assign I[2] = ~W[3]&W[2];
         assign I[3] = W[3];
```

```
        four_two_encoder En1(I,Y,zero);
endmodule
```

2. The complete truth table for the gate-level schematic shown in Figure 2. This truth table should not include "don't care" (i.e. 'X')!

4:2 Binary Encoder Truth Table

W_3	W_2	W_1	W_0	Y_1	Y_0	zero
0	0	0	0	0	0	1
0	0	0	1	0	0	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	1	0	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	1	1	0
1	0	0	1	1	1	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	1	1	0
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	0

3. A brief comparison of the behavioral implementation of a multiplexer described in the background section with the multiplexer you described in the previous lab using structural and dataflow.

The behavioral implementation of a multiplexor is less complicates and less likely to have any errors since your arent required to instantiate and assign values for the wires inside the circuit whereas you would for structural/dataflow description used before.