Pre-Lab 8: Counters, Clock Dividers, and Debounce Circuits
ECEN 248 - 505
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1. Supposed we want to build a 32-bit counter using the circuit in Figure 1. If the gates used to construct the half-adders in the circuit are assumed to have a 2 ns delay each and the flip-flop overhead is assumed to be negligible, what is the maximum clock frequency we could use to drive our counter? Given the clock frequency you just calculated, how long would it take this counter to roll over (i.e. return to 0). Please show your calculations.

Total Delay = 2 x 32

64ns

Maximum clock frequency = $\frac{1}{\text{Total Delay}}$

$= \frac{1}{64ns}$: f_{max} = 15.625 MHz

$= 2^{32} = 4.29s$

f_{max} = 15.625MHz

t = 4.29s

2. Consider the use of a counter to divide an incoming clock. If our incoming clock signal is 32.768 kHz and we need a 64 Hz signal, how many bits would our counter need to have (i.e. what is n) to divide the incoming clock correctly?

$f_2 = \frac{f_1}{2^n} = 64 = \frac{32768}{2^n}$

$2^n = \frac{32768}{64}$

$2^n = 512$

$n = \log_2(512)$ $\quad n=9$

3. If the Seconds per Division setting for Figure 3 was set to 1 ms/div, what do you think would be a good bit width for the counter in Figure 4, assuming a 50 MHz clock signal was driving the counter? Explain your answer.