Pre-Lab 7: Introduction to Sequential Logic
ECEN 248 - 505
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1. Create a new Verilog source file named “adder_2bit.v” with the module named “adder_2bit”. You can use your full adder module created in lab6.

```
module adder_2bit(
        input wire [3:0] W,
        input wire [3:0] W1,
        output wire [3:0] Y,
        output wire [3:0] Z,
        output overflow [1:0]  overflow 1,
        output overflow [1:0]  overflow 2
        );
        full_adder full_adder1(Y, W, overflow 1);
        full_adder full_adder2(Z, W1, overflow 2);
endmodule
```

2. If the circuit in Figure 7 utilizes the 2-bit carry ripple adder designed in lab3, what would be the maximum clock rate given that each gate delay is 4 ns? You can refer to your post-lab deliverable answer.

There are a total of nine gates, hence the max clock rate is f= 1/(9*4x10^-9) = 27.7 uHz

3. Compare all the three memory components discussed in the background part in the same table. Explain their differences and improvements.

The undefined state is when 2 inputs are pressed simultaneously, and the latch is caught in a forever loop. For clocks, there are two kinds which are rising edge clocks and falling edge clocks. This is the control where the latch in the flip flop is going to move the new result to Q and which is going to keep the old value.