

Esha Adhawade
Lab 4: Design & Simulation of 1 bit-adder
ECEN 454 - 503
October 9, 2022

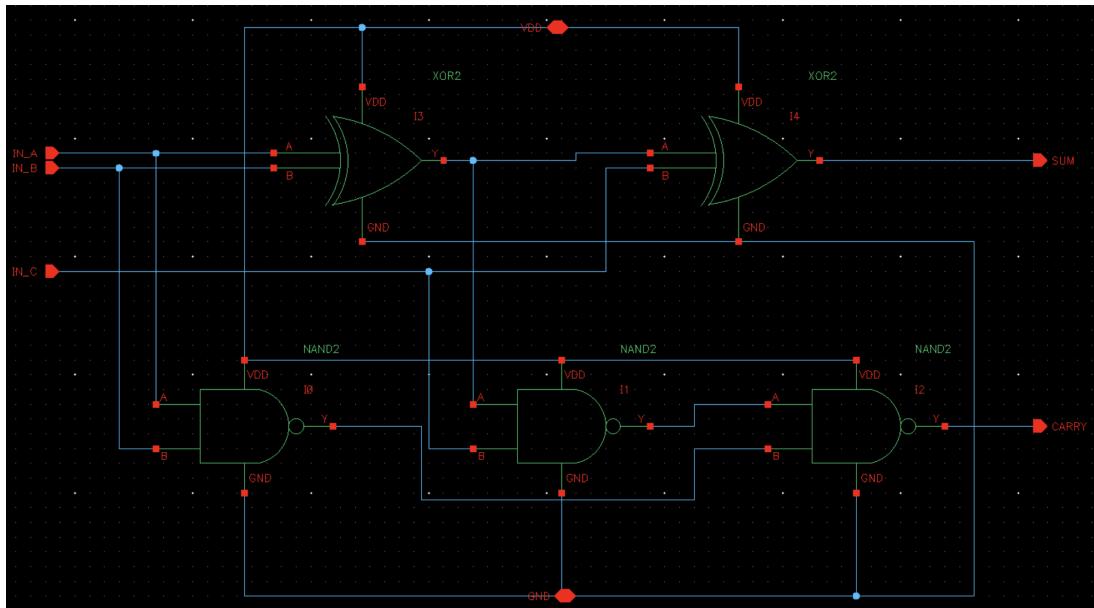
Introduction

The purpose of this lab is to build a one-bit adder and to perform post-layout simulations.

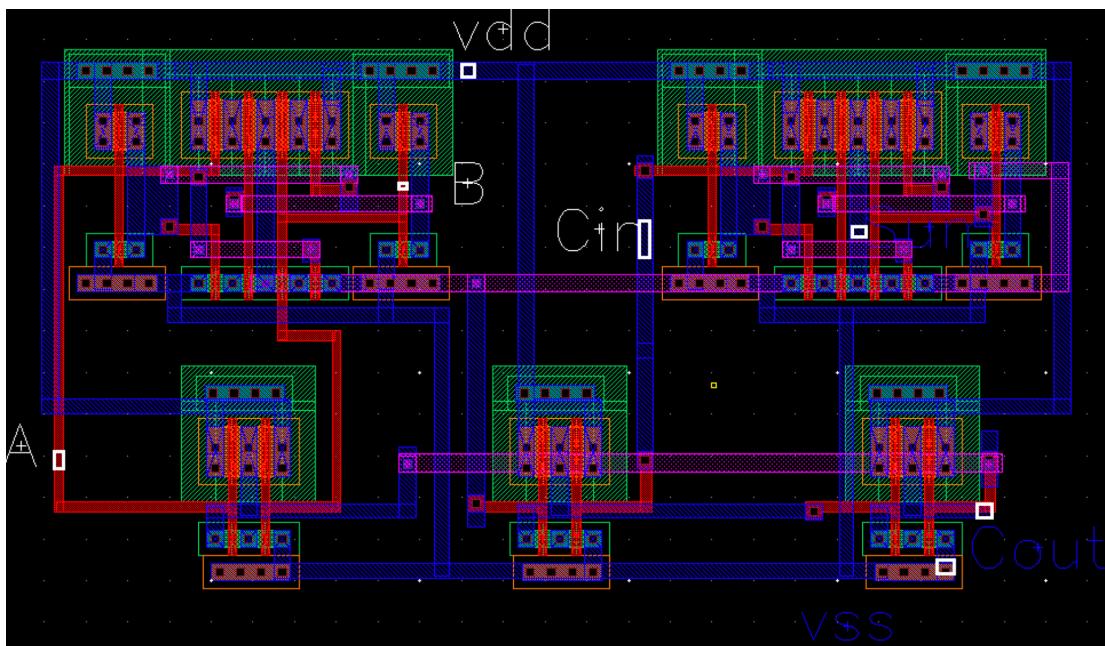
Result

1 Bit Adder

Schematic

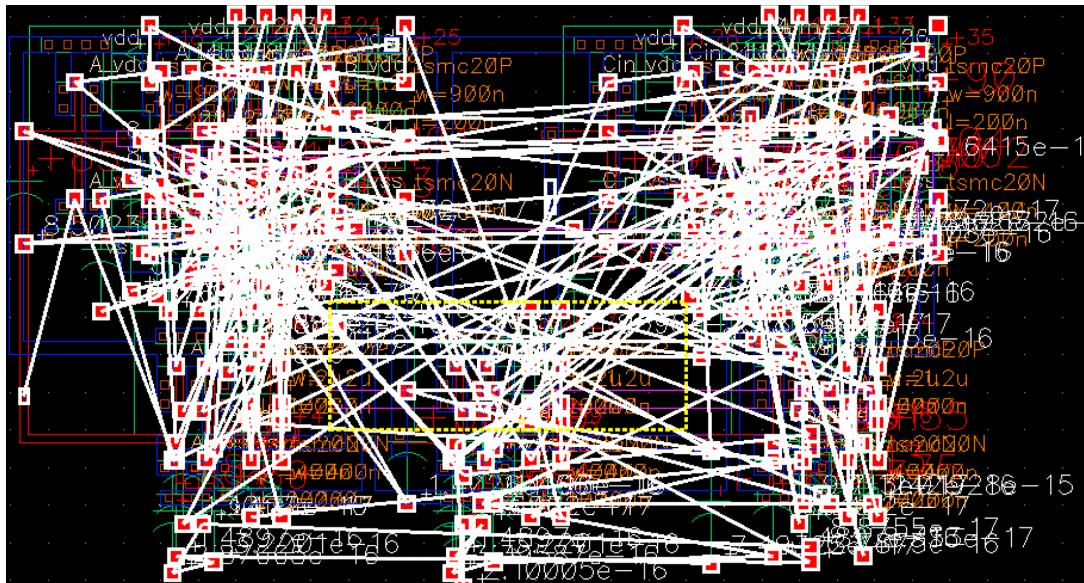


Layout



DRC

```
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "1bitadder layout" *****
Total errors found: 0
```



LVS

The net-lists match.

	layout	schematic
instances	0	0
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	36	36
total	36	36

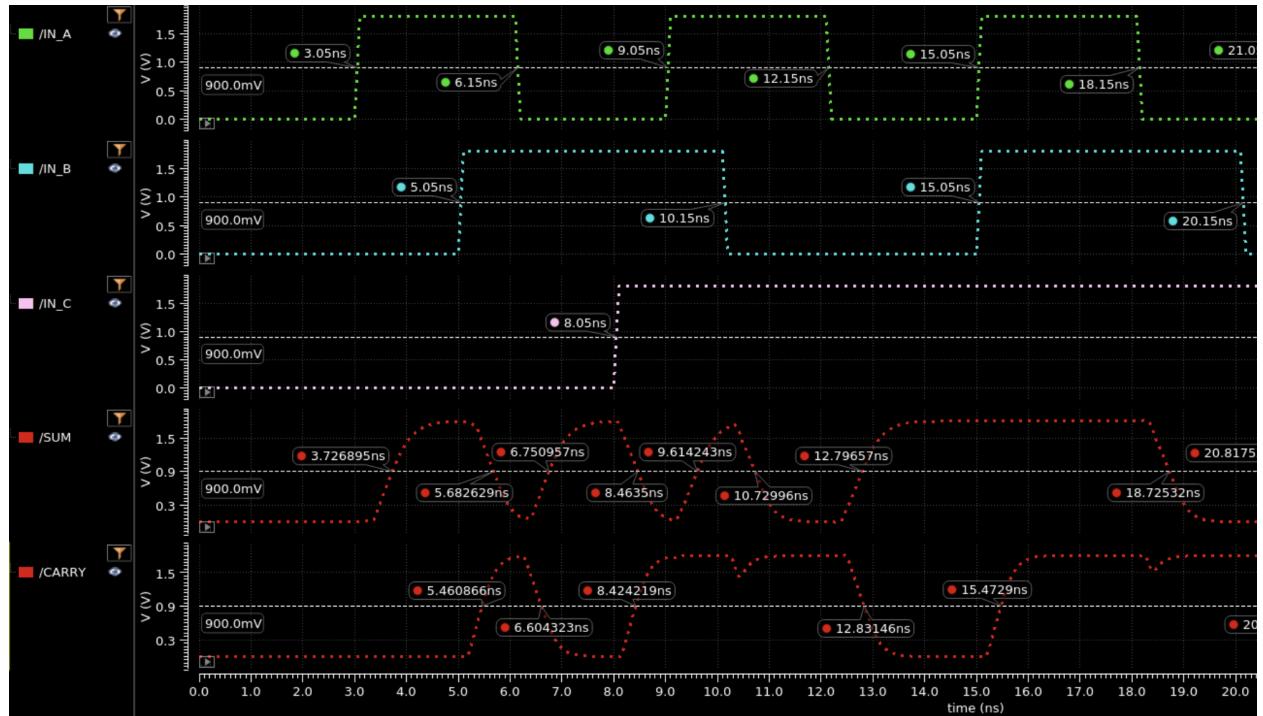
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	26	26
total	26	26

	terminals	
un-matched	0	0
matched but different type	0	0
total	7	7

Rising Delay / Falling Delay

Output	Rising Delay (ns)	Falling Delay (ns)	Error
Sum	0.677	0.633	7%
Carry	0.411	0.455	10.61%

Waveform



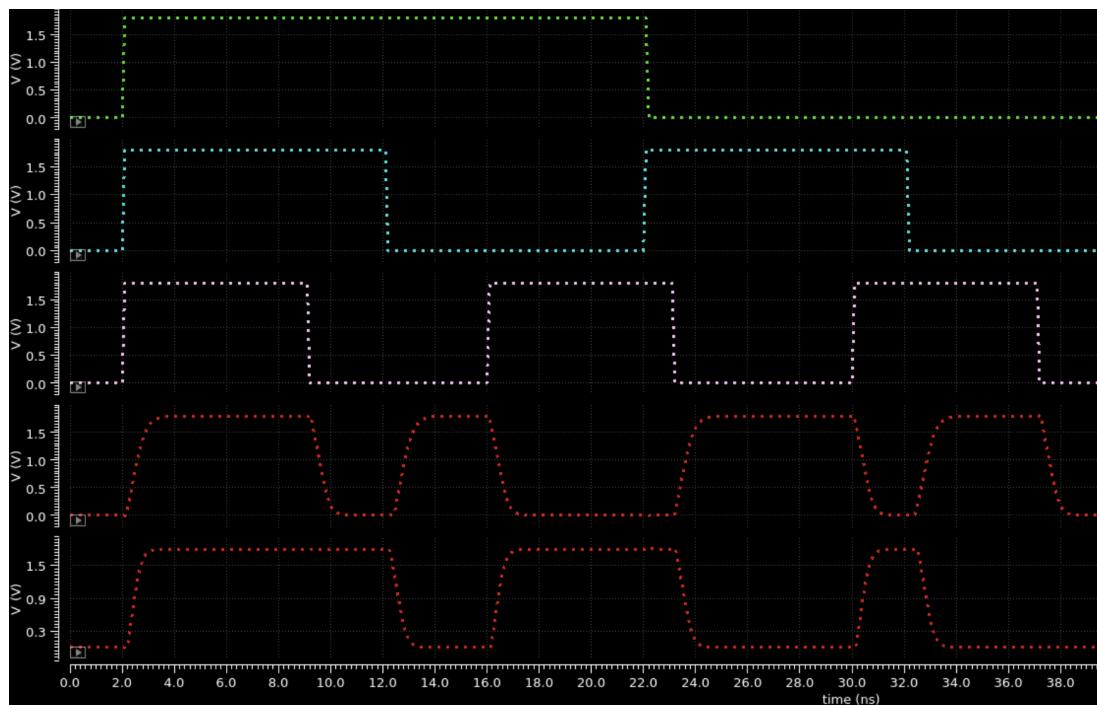
Power Dissipations

Power Source	Value (uW)
VDC	-110.51
IN_A	-0.761
IN_B	-0.807
IN_C	0.191

Max Frequency (Waveform)

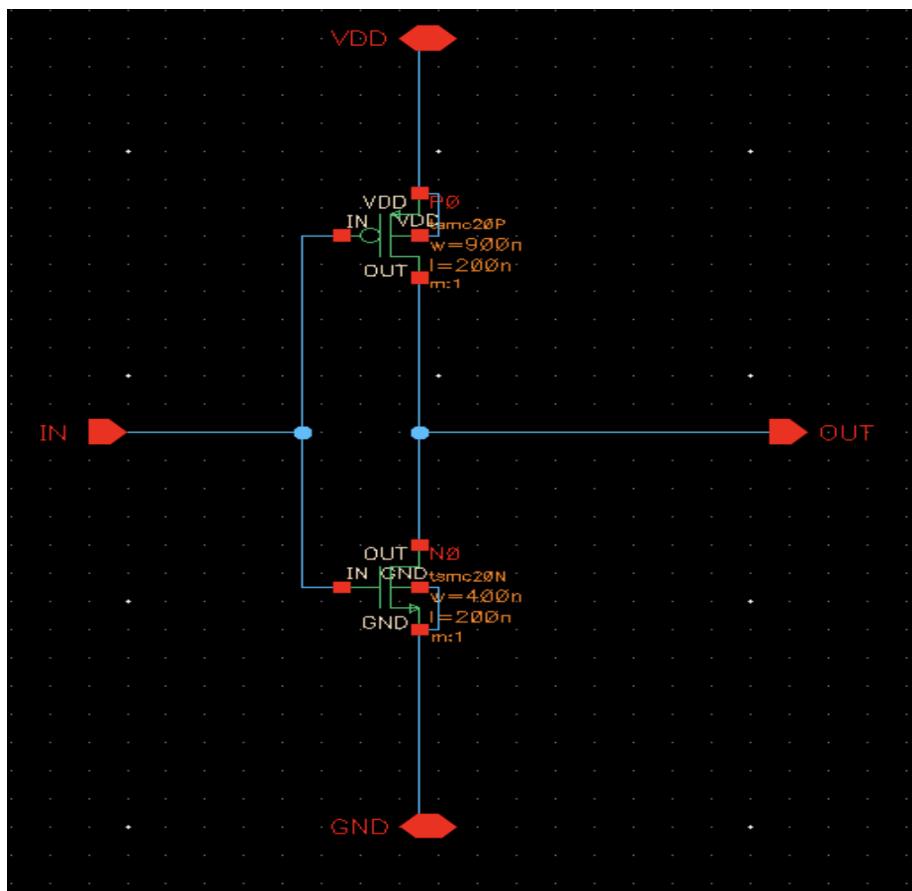
Max Frequency: 71MHz

Max Period: 14 ns

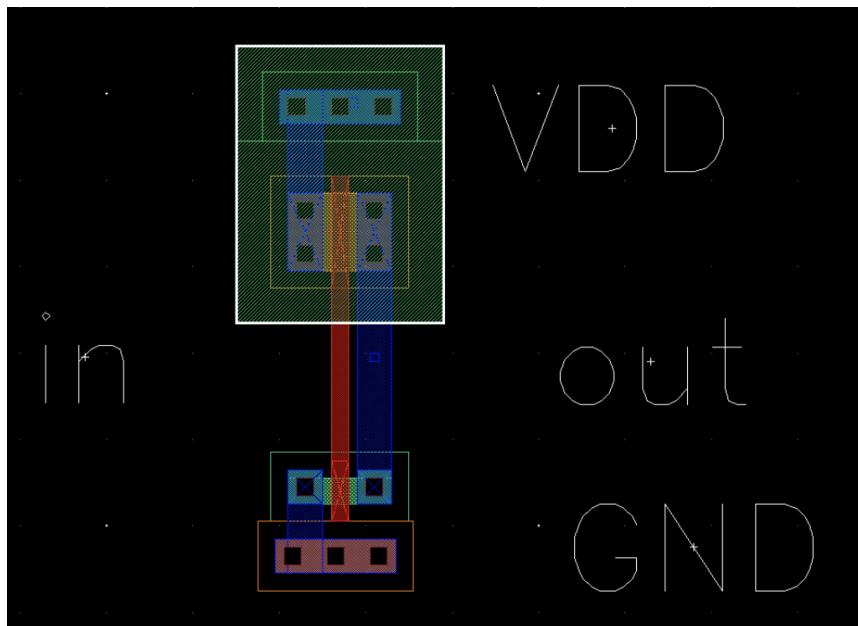


Inverter

Schematic



Layout



LVS

The net-lists match.

```

layout schematic
  instances
un-matched      0      0
rewired          0      0
size errors      0      0
pruned           0      0
active           2      2
total            2      2

  nets
un-matched      0      0
merged           0      0
pruned           0      0
active           4      4
total            4      4

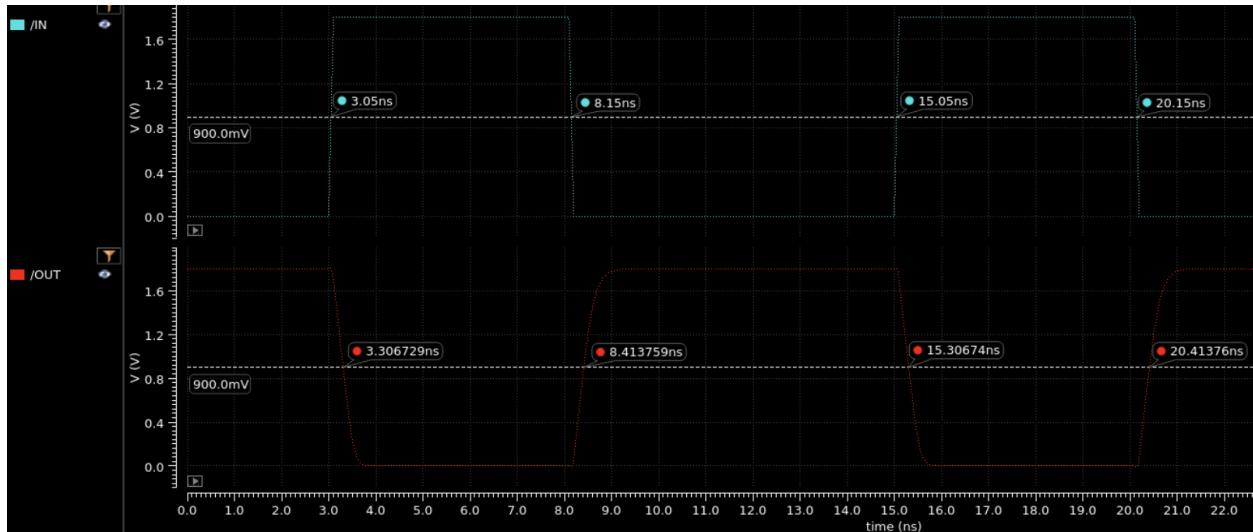
  terminals
un-matched      0      0
matched but
different type   0      0
total            4      4

```

Rising Delay / Falling Delay

Rising Delay (ns)	Falling Delay (ns)	Error
0.264	0.257	2.76%

Waveforms

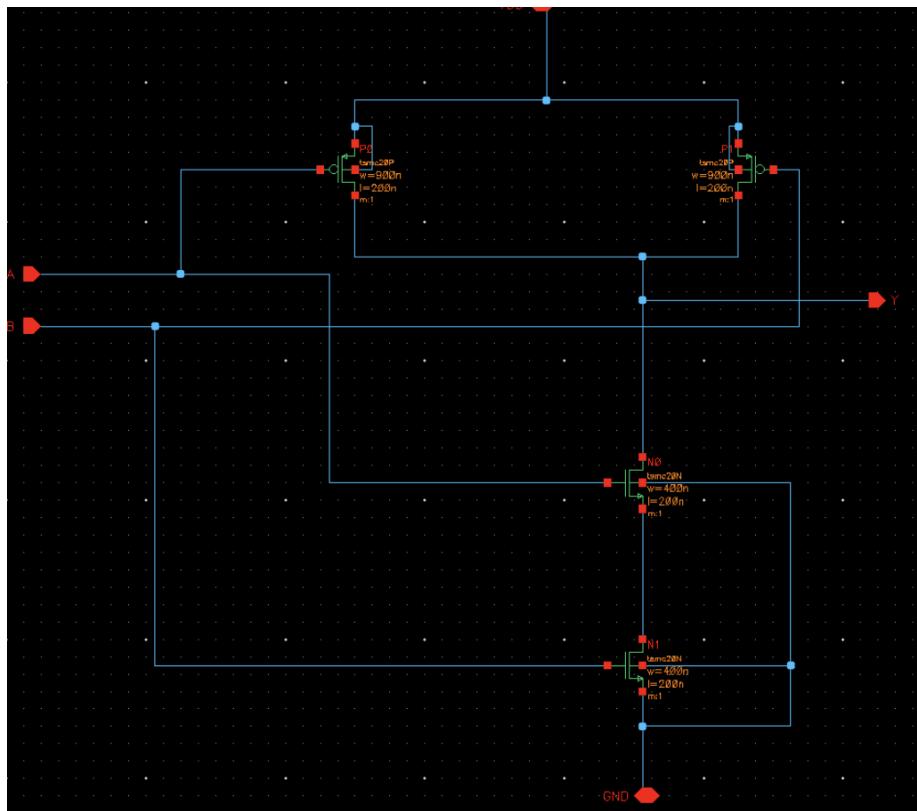


Power Dissipations

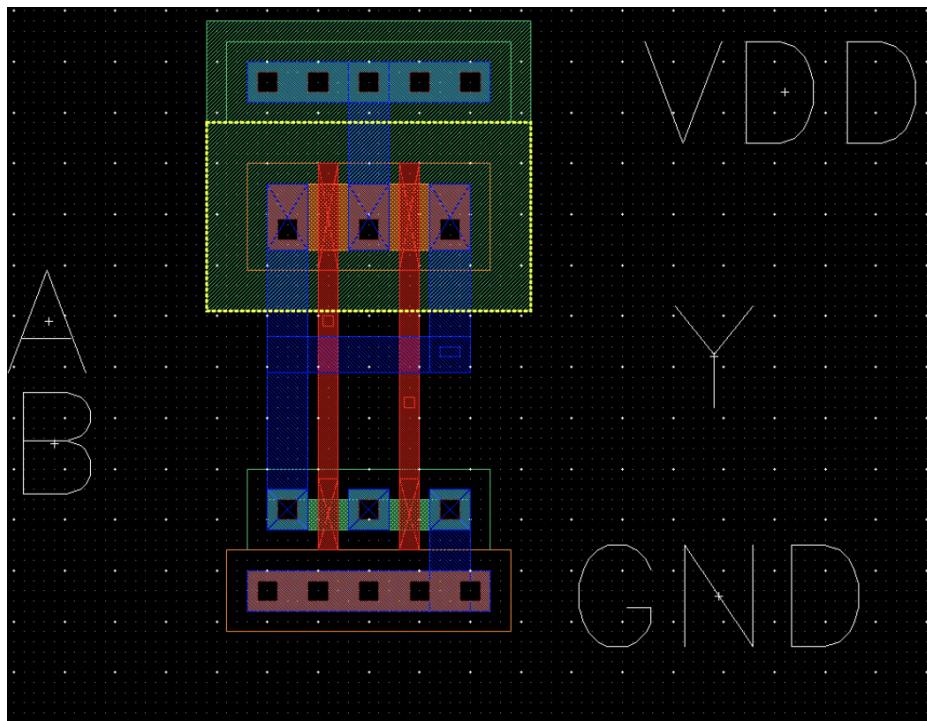
Power Source	Value (uW)
VDC	-11.57
IN	-0.18

NAND

Schematic



Layout



LVS

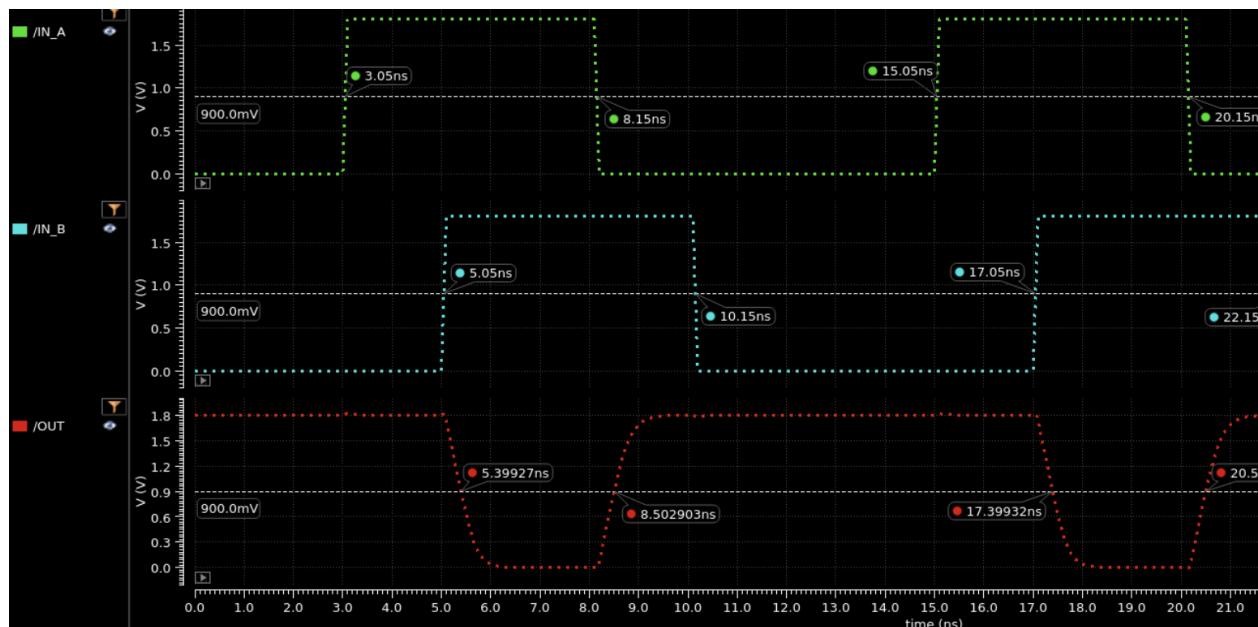
The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	4	4
total	4	4
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	6	6
total	6	6
	terminals	
un-matched	0	0
matched but different type	0	0
total	5	5

Rising Delay / Falling Delay

Rising Delay (ns)	Falling Delay (ns)	Error
0.353	0.350	1.03%

Waveforms

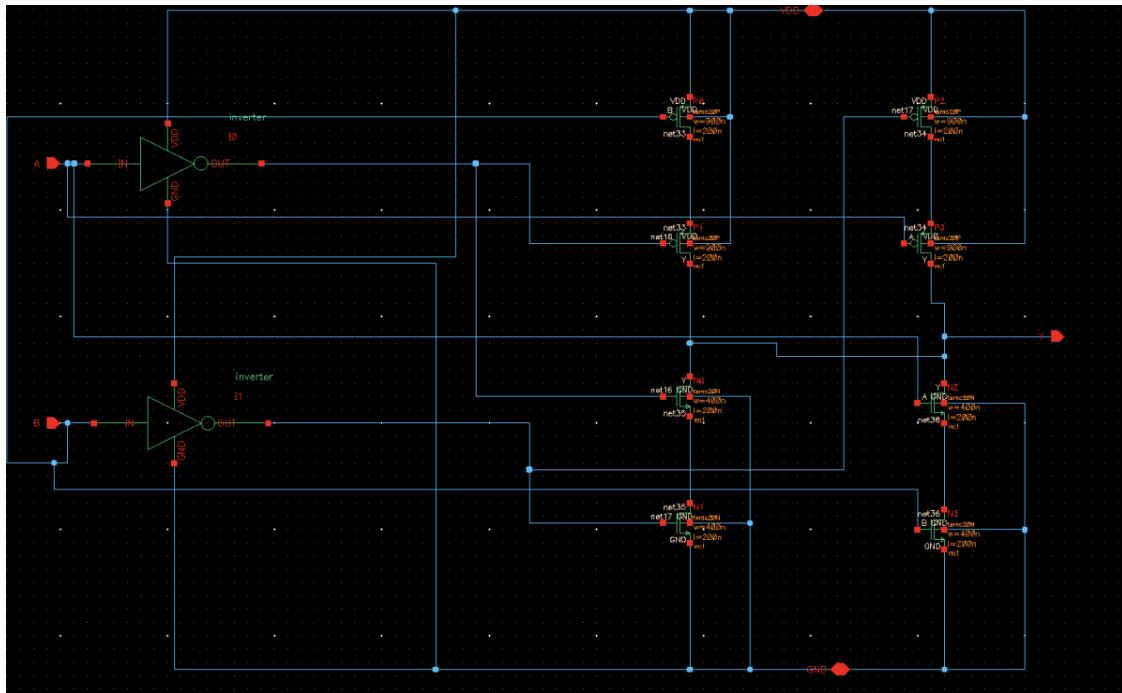


Power Dissipations

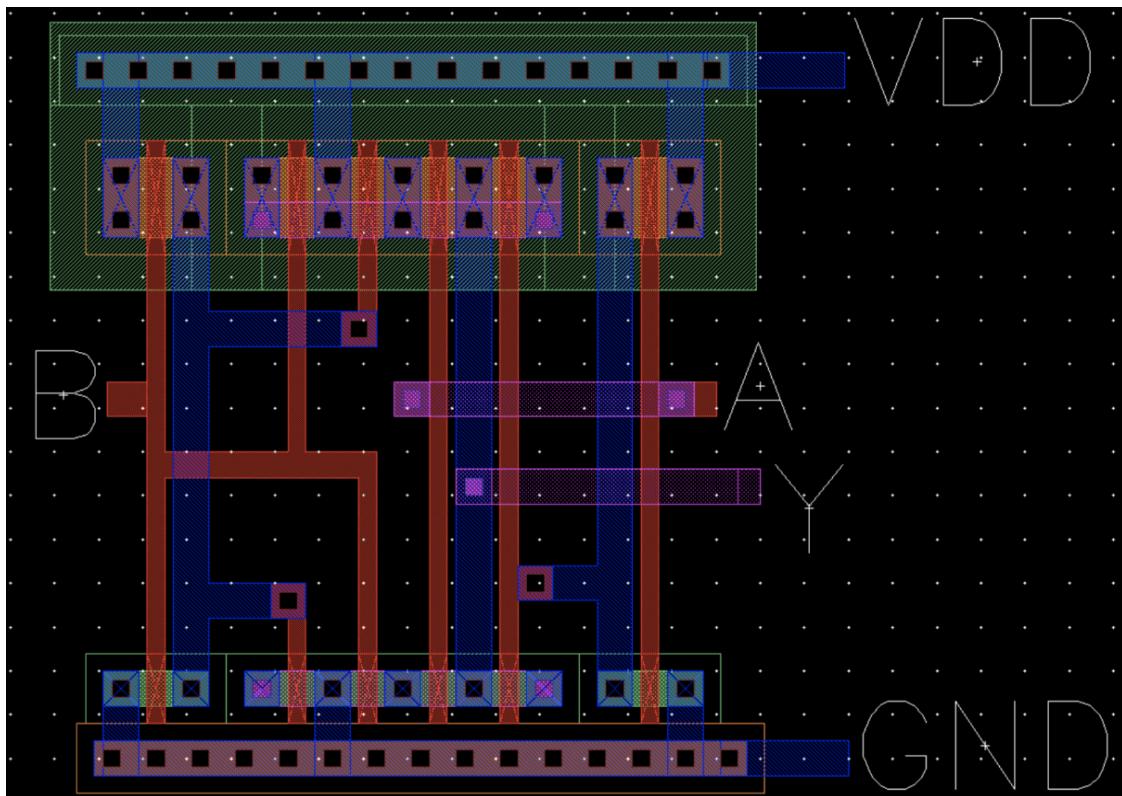
Power Source	Value (uW)
VDC	-11.73
IN_A	-0.136
IN_B	-0.131

XOR

Schematic



Layout



LVS

The net-lists match.

```

layout schematic
instances
un-matched      0      0
rewired          0      0
size errors     0      0
pruned          0      0
active          4      4
total           4      4

nets
un-matched      0      0
merged          0      0
pruned          0      0
active          6      6
total           6      6

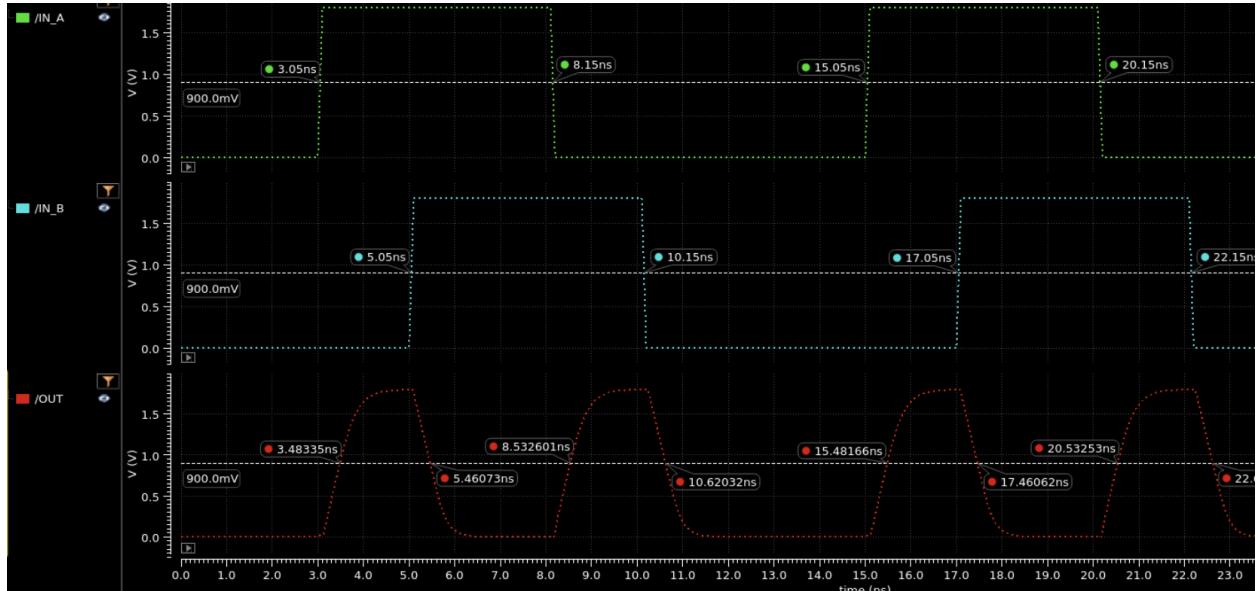
terminals
un-matched      0      0
matched but
different type  1      1
total           5      5

```

Rising Delay / Falling Delay

Rising Delay (ns)	Falling Delay (ns)	Error
0.434	0.411	5.5%

Waveforms



Power Dissipations

Power Source	Value (uW)
VDC	-36.3
IN_A	-0.3
IN_B	-0.324

