

**Esha Adhawade**  
**Lab 5: Design & Simulation of 4-bit-adder**  
**ECEN 454 - 503**  
**October 24, 2022**

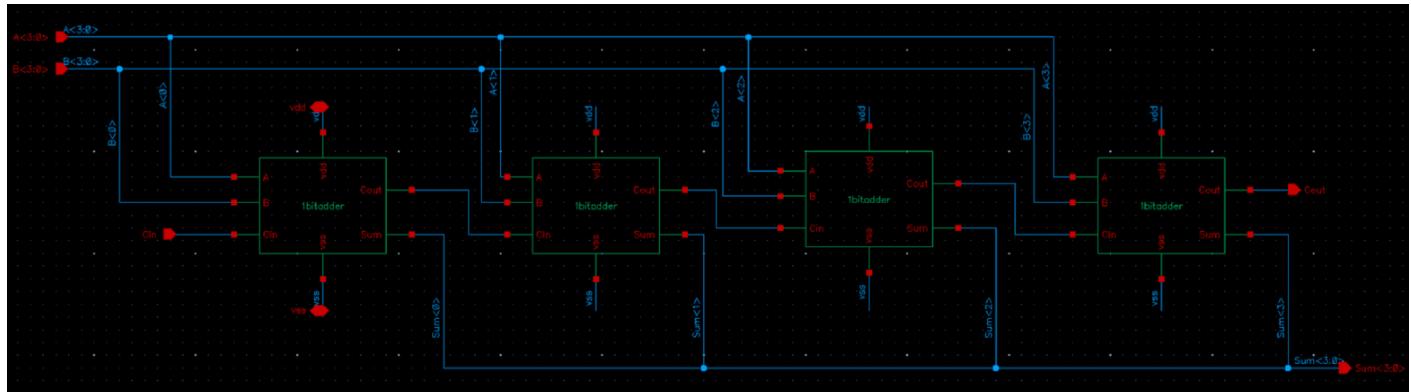
## Introduction

The purpose of this lab is to design a 4-bit adder.

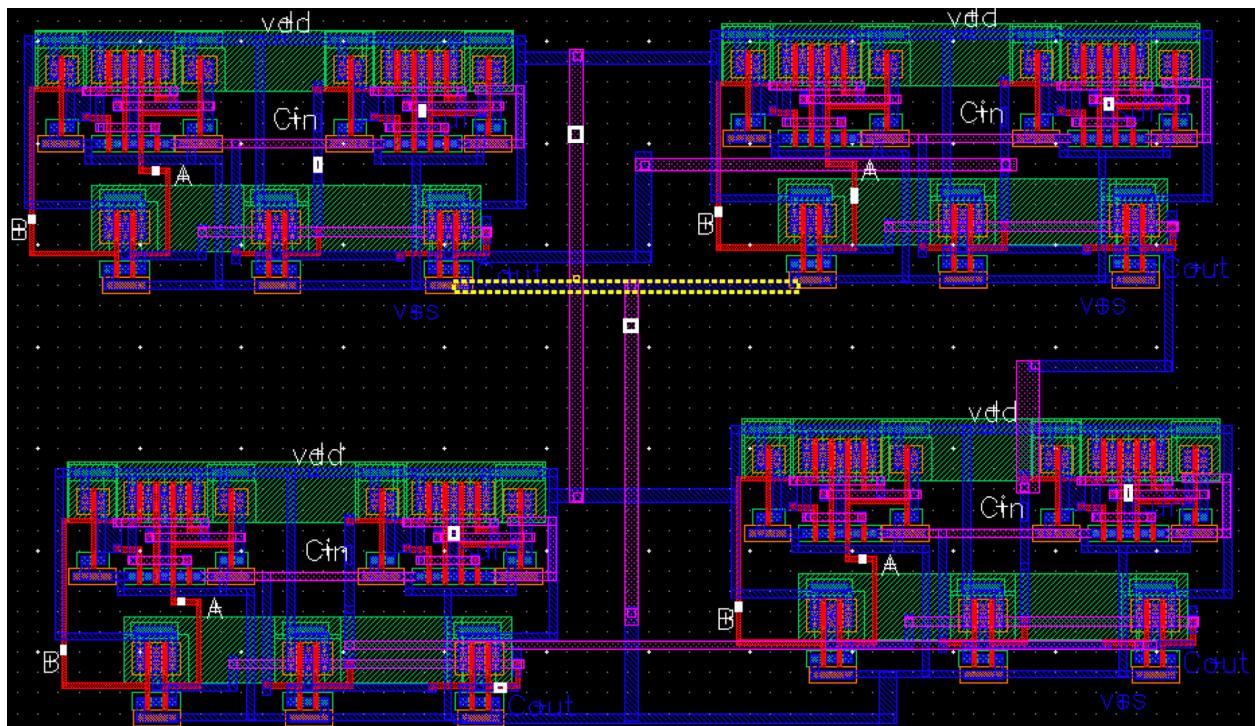
## Result

### 4 Bit Adder

Schematic



Layout



## LVS

|             | instances |     |
|-------------|-----------|-----|
| un-matched  | 0         | 0   |
| rewired     | 0         | 0   |
| size errors | 0         | 0   |
| pruned      | 0         | 0   |
| active      | 144       | 144 |
| total       | 144       | 144 |

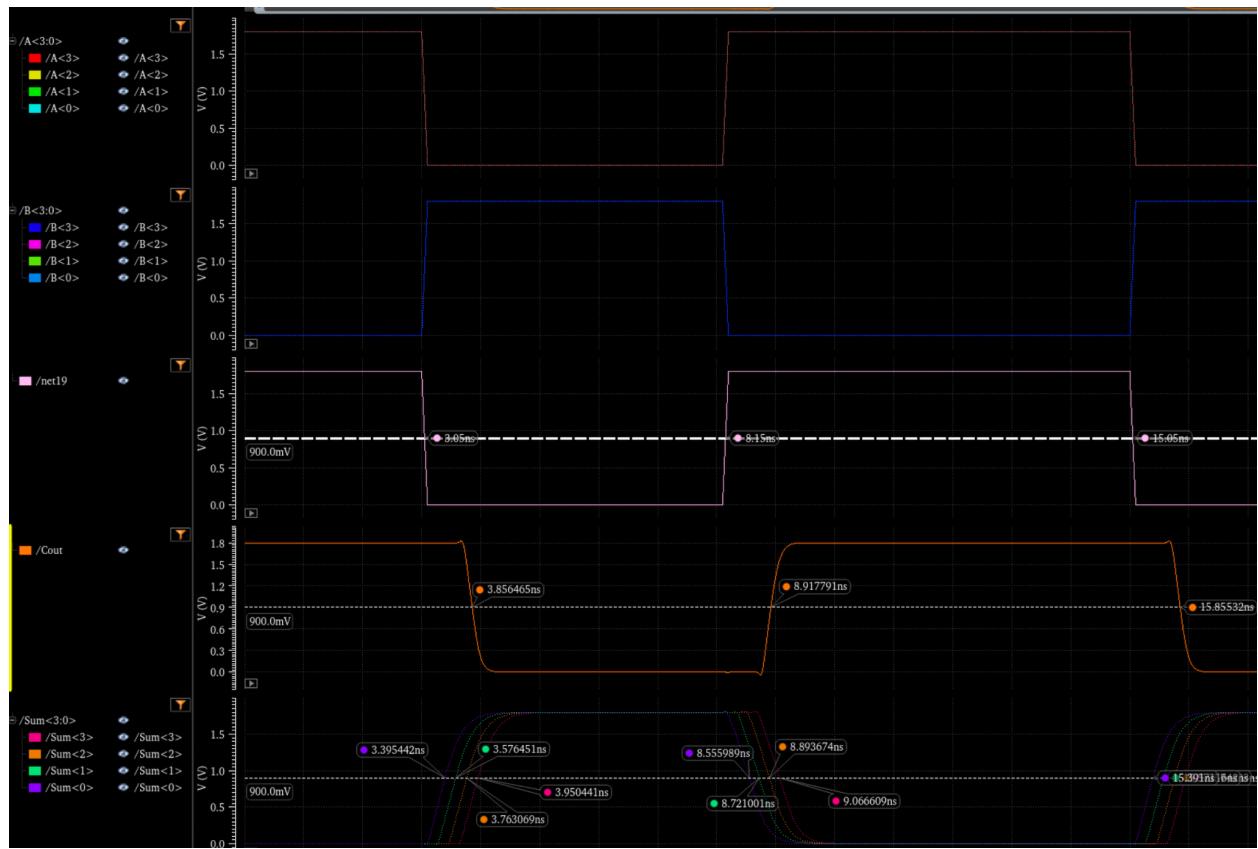
|            | nets |    |
|------------|------|----|
| un-matched | 0    | 0  |
| merged     | 0    | 0  |
| pruned     | 0    | 0  |
| active     | 91   | 91 |
| total      | 91   | 91 |

|                               | terminals |    |
|-------------------------------|-----------|----|
| un-matched                    | 0         | 0  |
| matched but<br>different type | 0         | 0  |
| total                         | 16        | 16 |

A=0000, B=1111, Carry In=1

### Waveform



### Rising Delay / Falling Delay

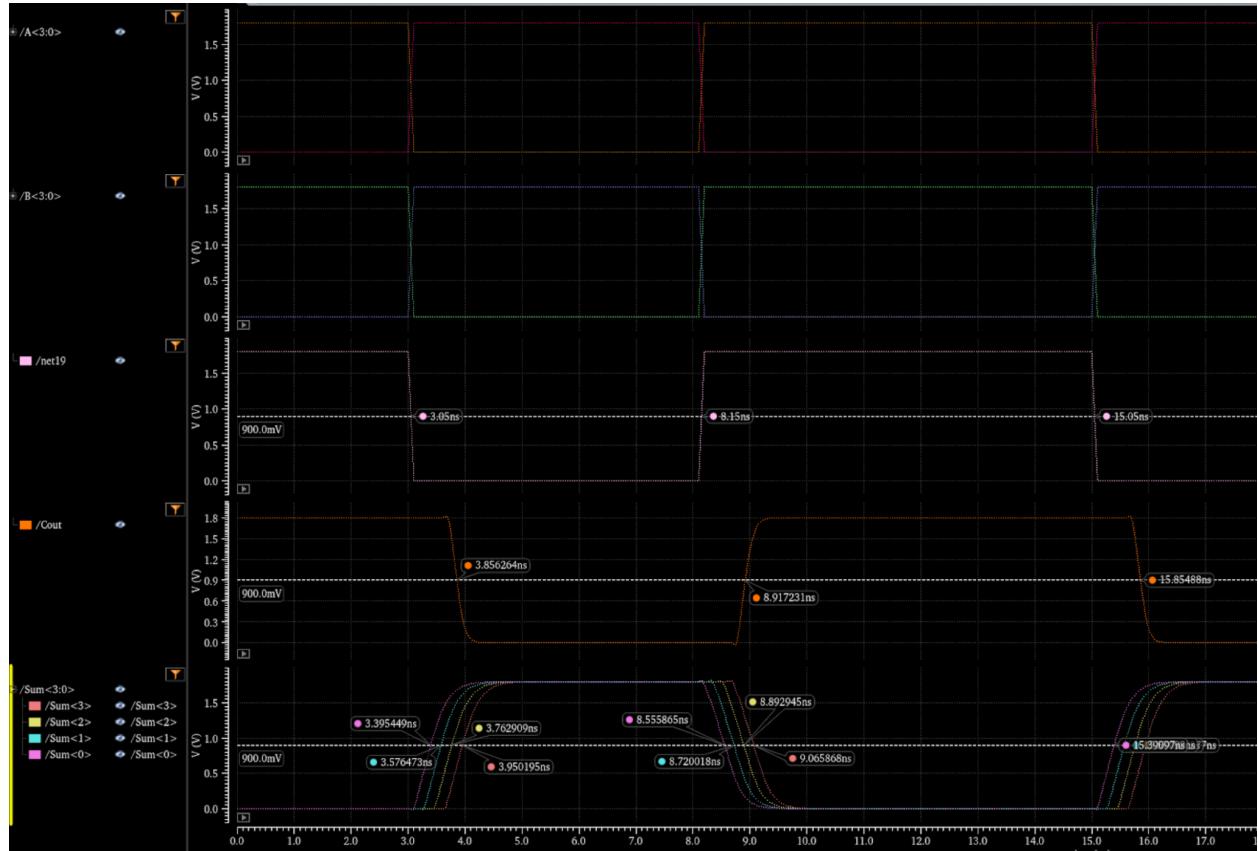
| Pins   | Rising Delay (ns) | Falling Delay (ns) |
|--------|-------------------|--------------------|
| Cout   | 0.806             | 0.768              |
| Sum<0> | 0.345             | 0.406              |
| Sum<1> | 0.526             | 0.571              |
| Sum<2> | 0.713             | 0.744              |
| Sum<3> | 0.900             | 0.917              |

### Power Dissipations

| Voltage Source | Value (uW) |
|----------------|------------|
| VDD            | -169.6     |

A=1010, B=0101, Carry In=0

### Waveform



### Rising Delay / Falling Delay

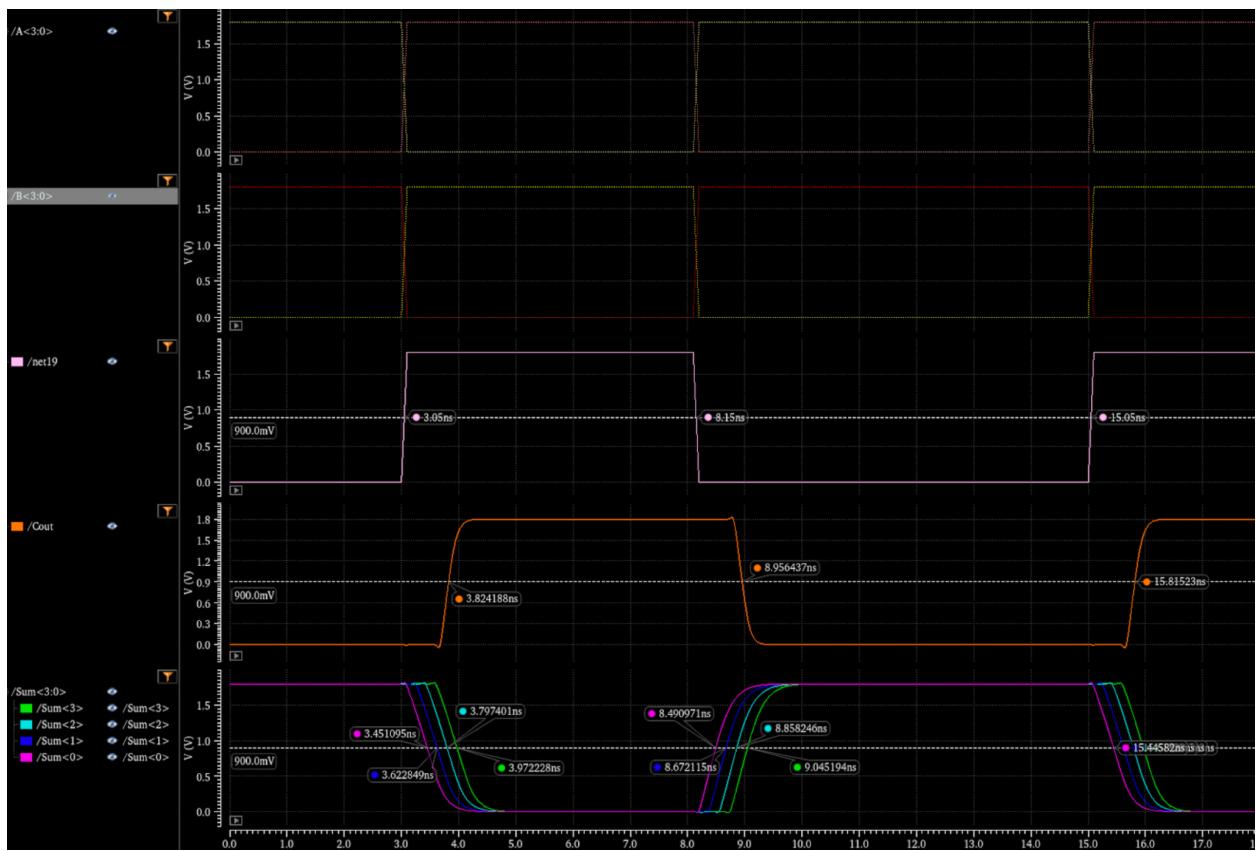
| Pins   | Rising Delay (ns) | Falling Delay (ns) |
|--------|-------------------|--------------------|
| Cout   | 0.806             | 0.767              |
| Sum<0> | 0.345             | 0.406              |
| Sum<1> | 0.526             | 0.570              |
| Sum<2> | 0.713             | 0.743              |
| Sum<3> | 0.900             | 0.916              |

### Power Dissipations

| Voltage Source | Value (uW) |
|----------------|------------|
| VDD            | -186.6     |

A=1010, B=0101, Carry In=1

### Waveform



### Rising Delay / Falling Delay

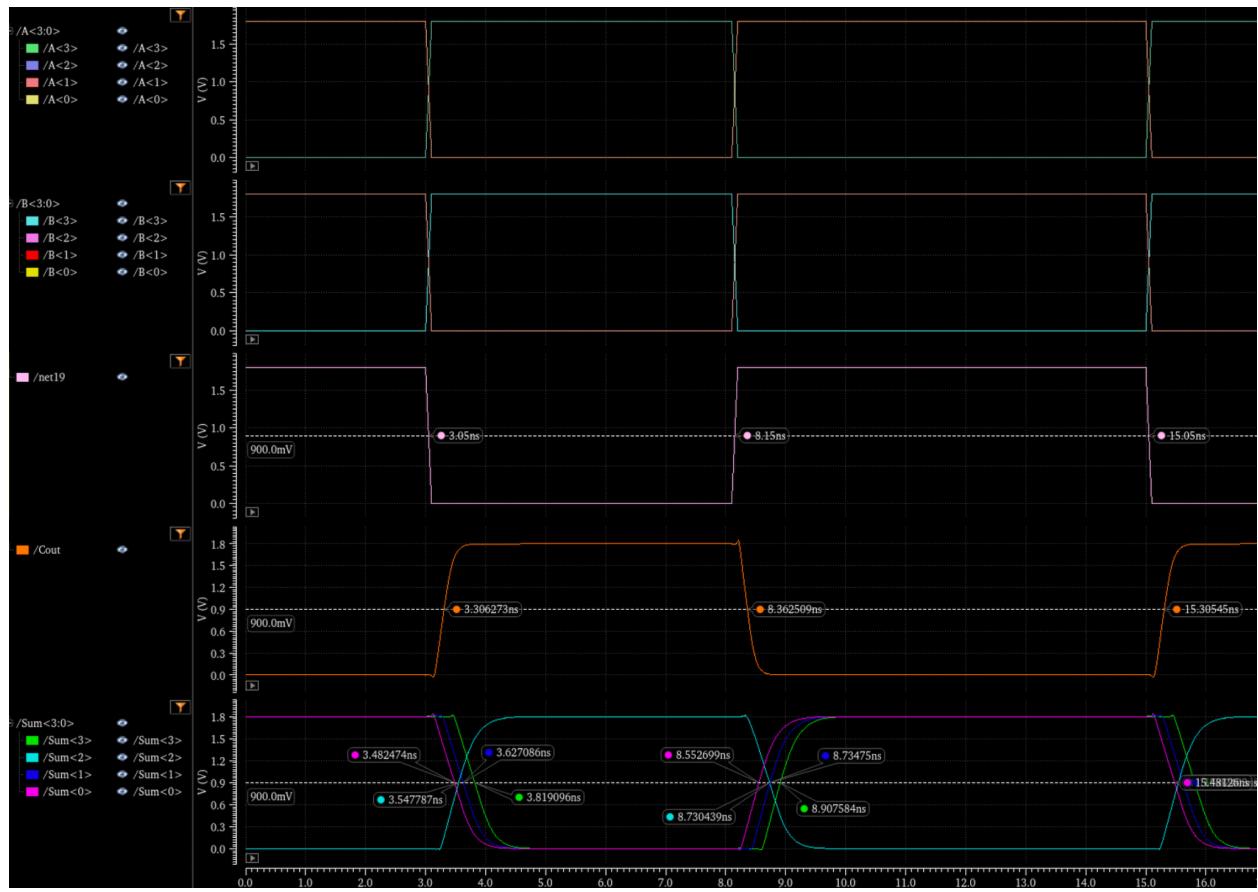
| Pins   | Rising Delay (ns) | Falling Delay (ns) |
|--------|-------------------|--------------------|
| Cout   | 0.774             | 0.806              |
| Sum<0> | 0.401             | 0.341              |
| Sum<1> | 0.573             | 0.522              |
| Sum<2> | 0.747             | 0.708              |
| Sum<3> | 0.922             | 0.895              |

### Power Dissipations

| Voltage Source | Value (uW) |
|----------------|------------|
| VDD            | -186.6     |

A=1100, B=1000, Carry In=0

### Waveform



### Rising Delay / Falling Delay

| Pins   | Rising Delay (ns) | Falling Delay (ns) |
|--------|-------------------|--------------------|
| Cout   | 0.256             | 0.213              |
| Sum<0> | 0.432             | 0.403              |
| Sum<1> | 0.498             | 0.580              |
| Sum<2> | 0.577             | 0.585              |
| Sum<3> | 0.769             | 0.758              |

### Power Dissipations

| Voltage Source | Value (uW) |
|----------------|------------|
| VDD            | -182.0     |

