Esha Adhawade

Lab 2: Cadence Custom Layout: Design Rules, Extraction & Verification

ECEN 454 - 503

September 25, 2022

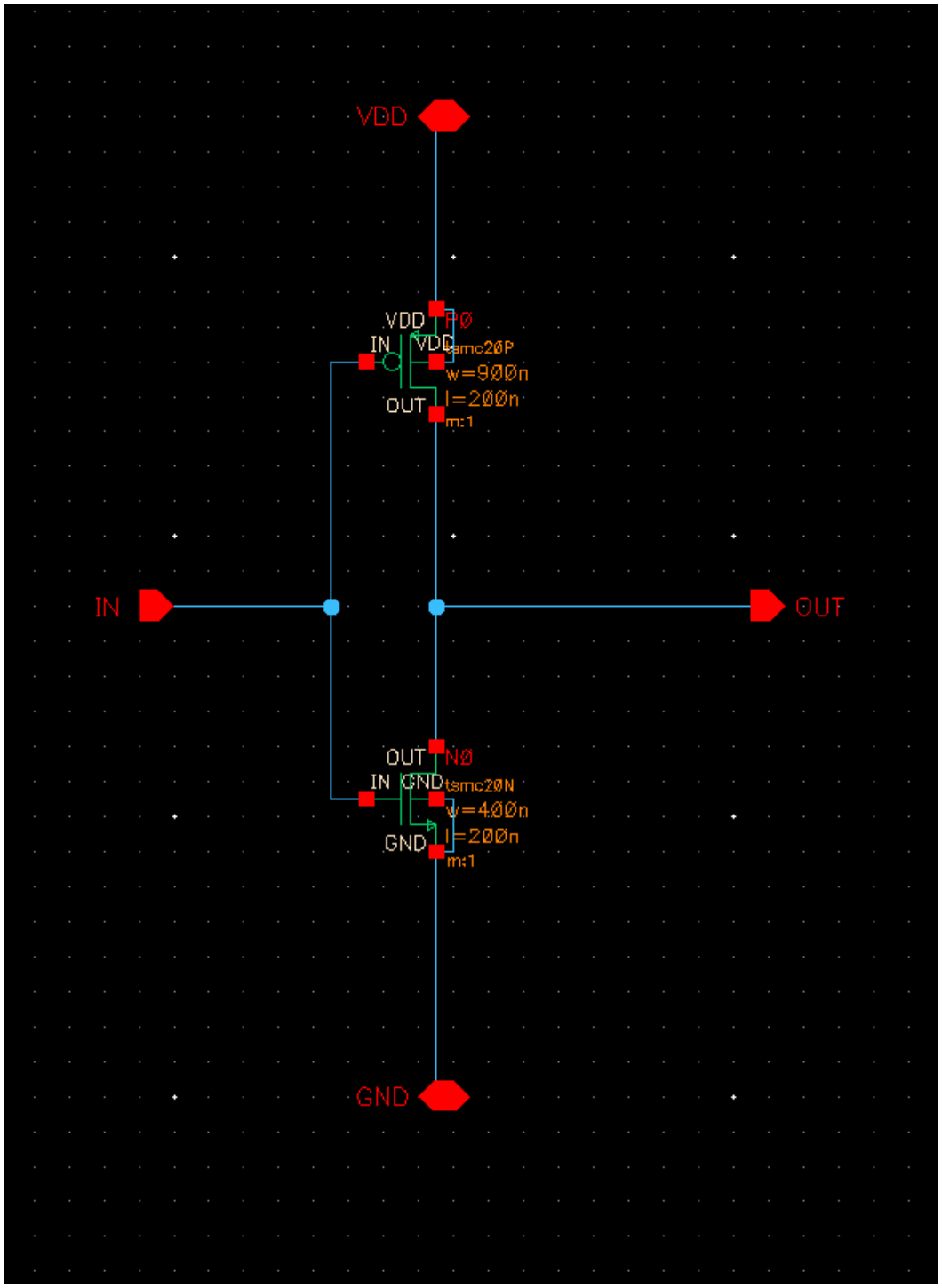
Introduction

The purpose of this lab is to create all layouts and extraction/ verifications for inverter, NAND, and XOR gates.

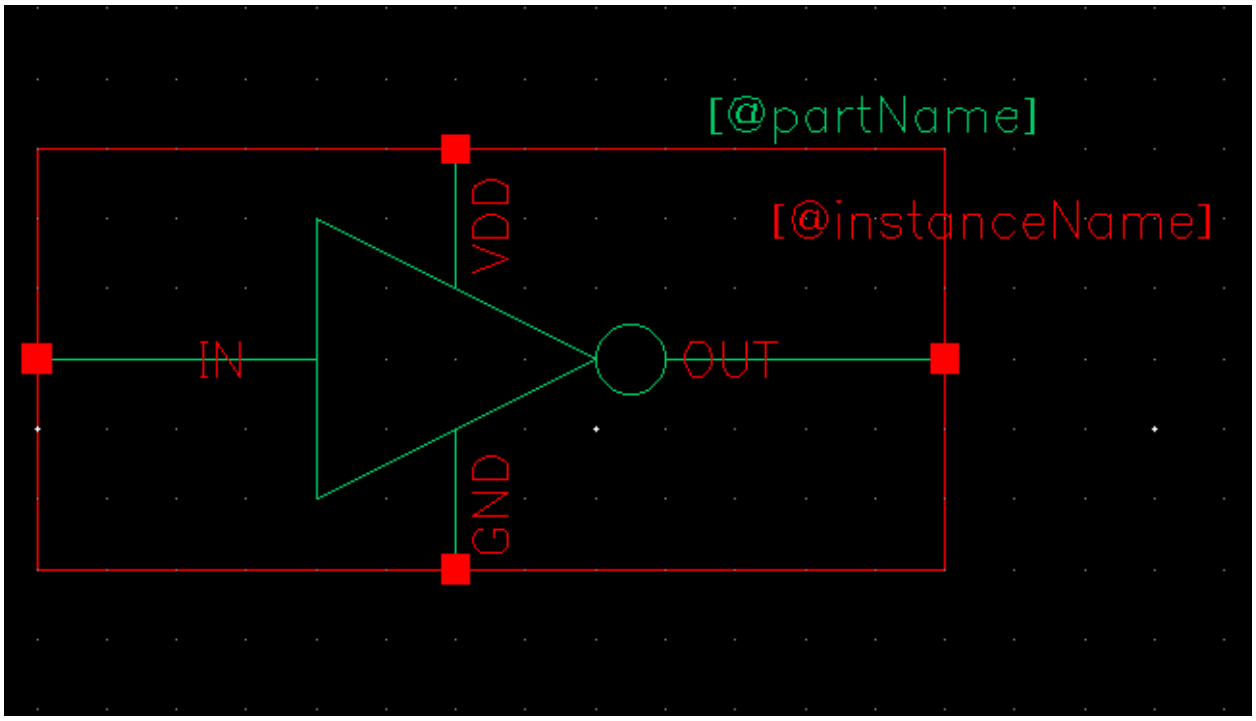
Result

Inverter

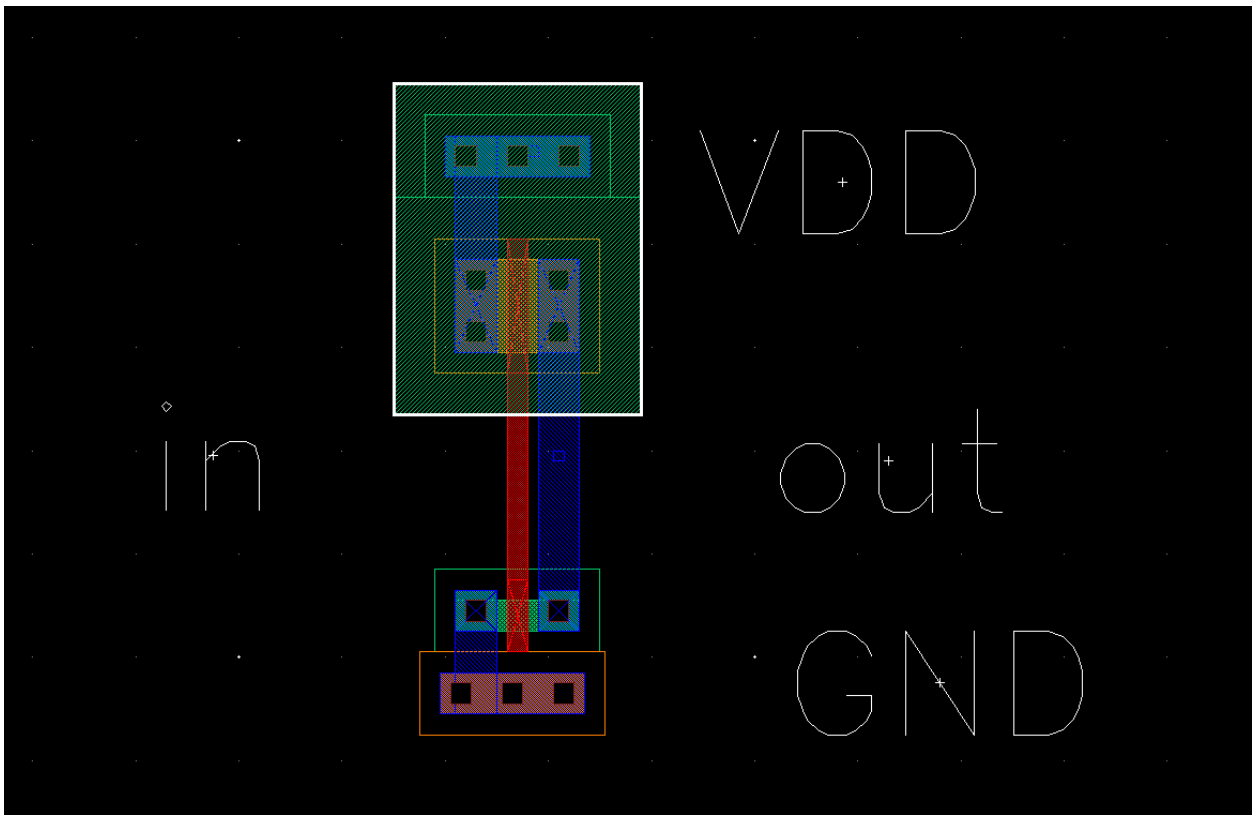
Schematic



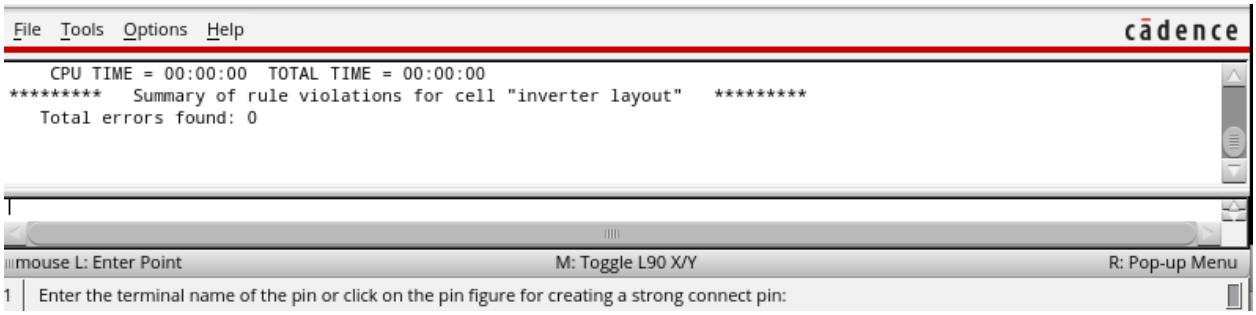
Symbol



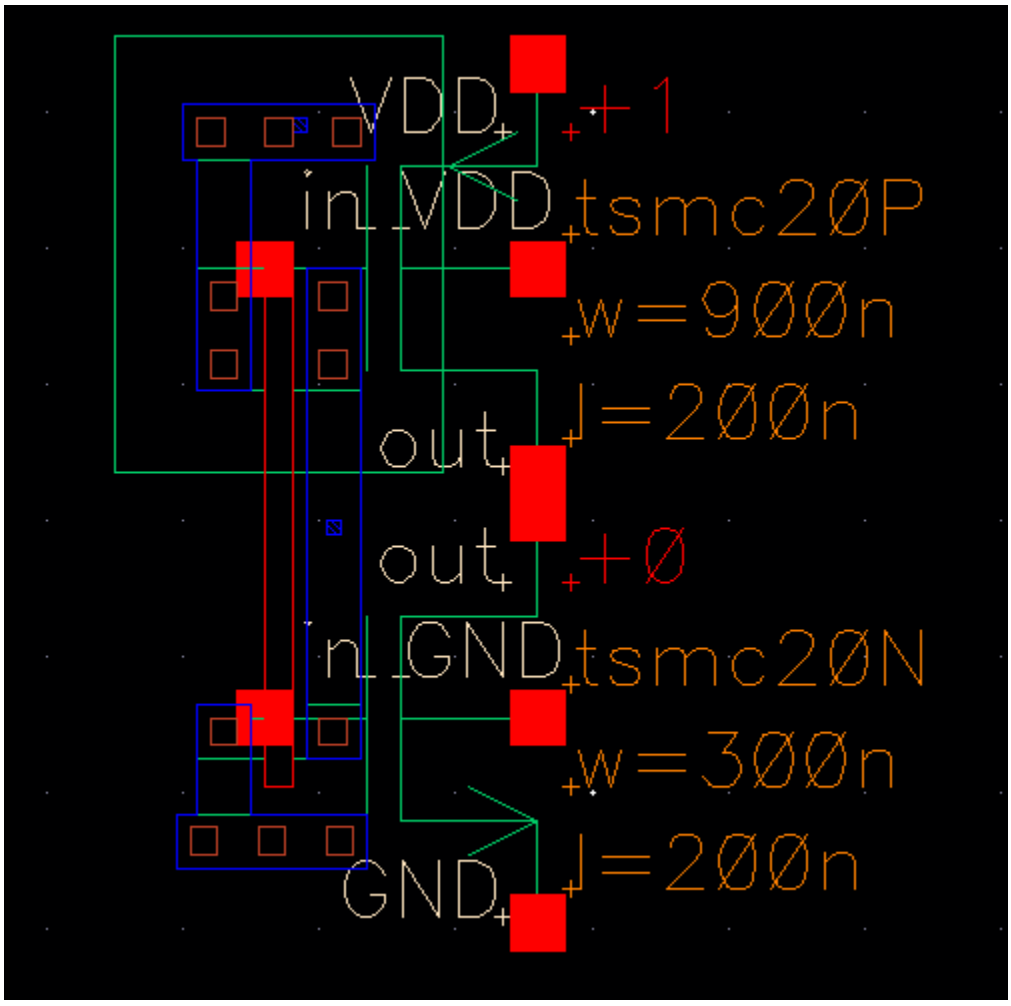
Layout



DRC - match



DRC

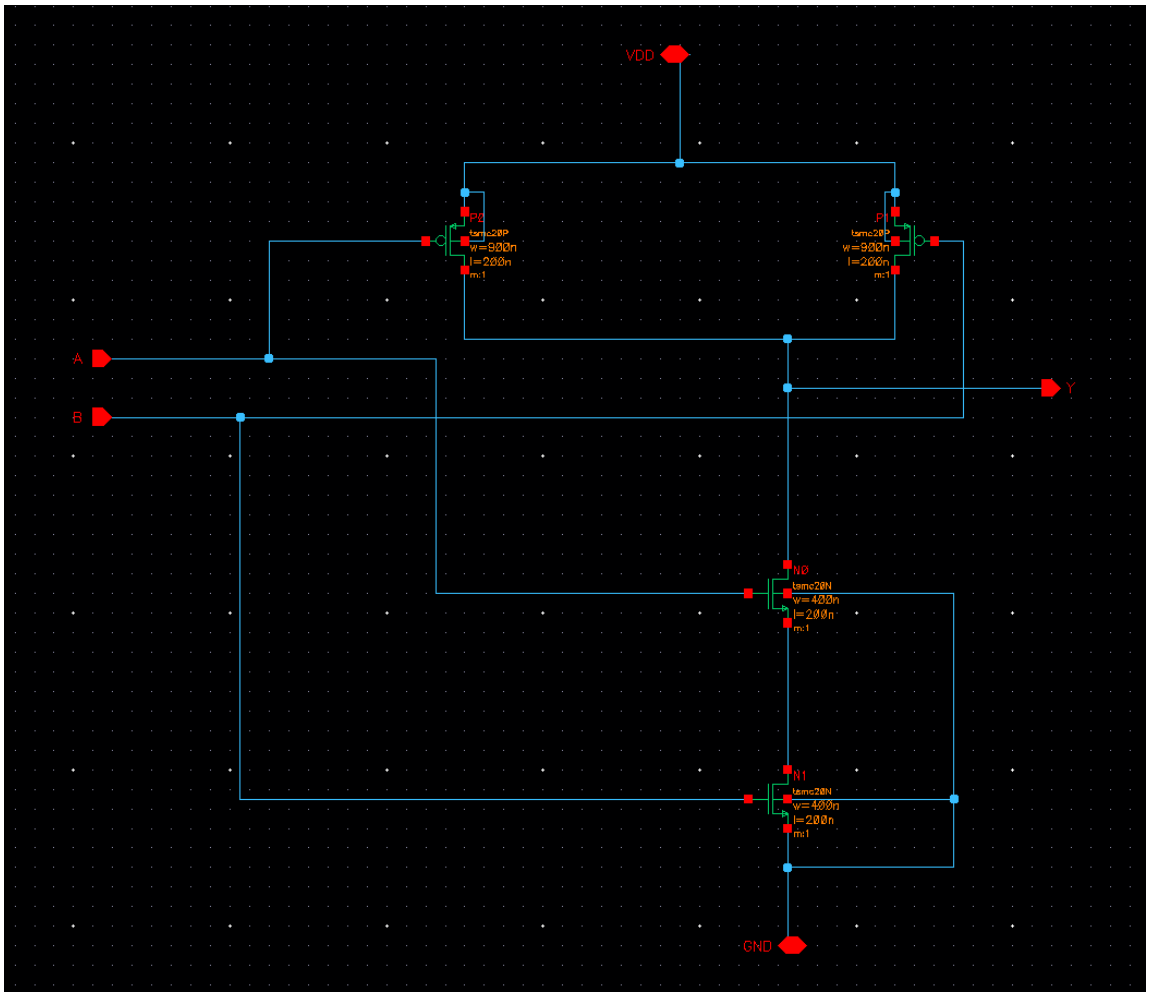


LVS (The net-lists match.)

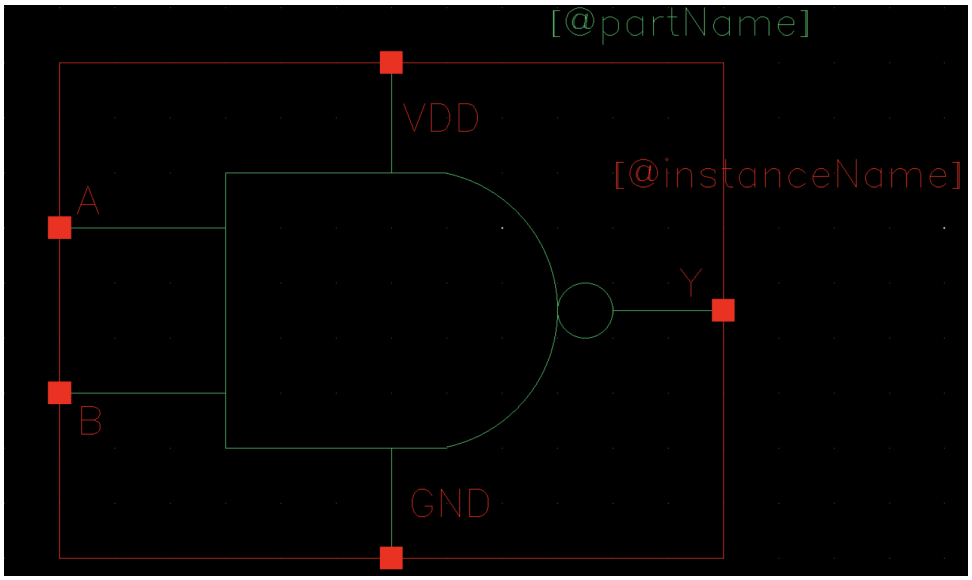
```
@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/e/esha.adhawade/ecen454_503/LVS -l -s -t /home/ugrads/e/esha.adhawade/ecen454_503/LVS/layout /home/ugrads/e/esha.adhawade/ecen454_503/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/e/esha.adhawade/ecen454_503/LVS/layout/netlist
       count
         4              nets
         4              terminals
         1              pmos
         1              nmos

    Net-list summary for /home/ugrads/e/esha.adhawade/ecen454_503/LVS/schematic/netlist
       count
         4              nets
         4              terminals
         1              pmos
         1              nmos


    Terminal correspondence points
    N0          N1          GND
    N2          N3          IN
    N1          N2          OUT
    N3          N0          VDD

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  2       2
        total                   2       2

                                  nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                                terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   4       4


Probe files from /home/ugrads/e/esha.adhawade/ecen454_503/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/ugrads/e/esha.adhawade/ecen454_503/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

NAND

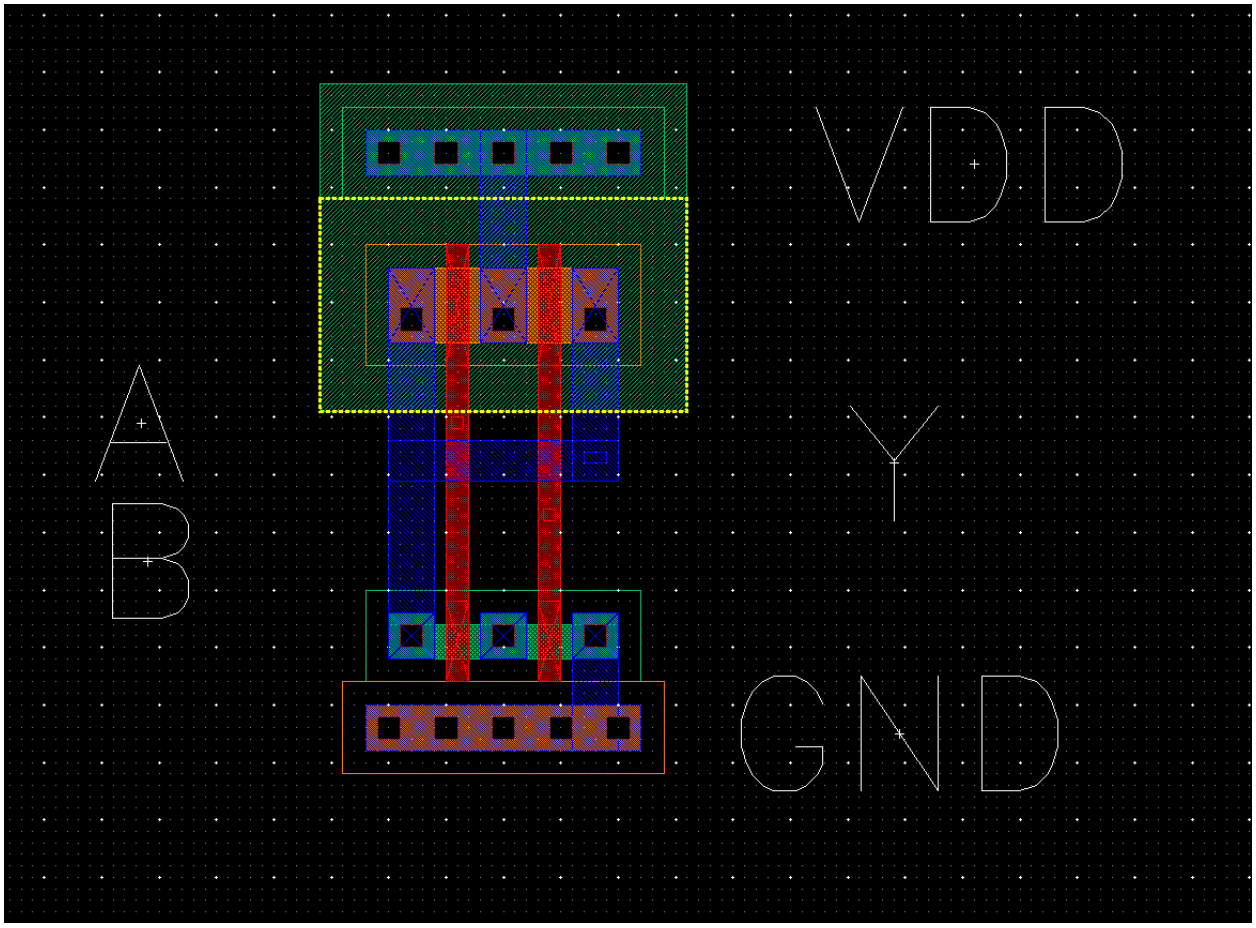
Schematic



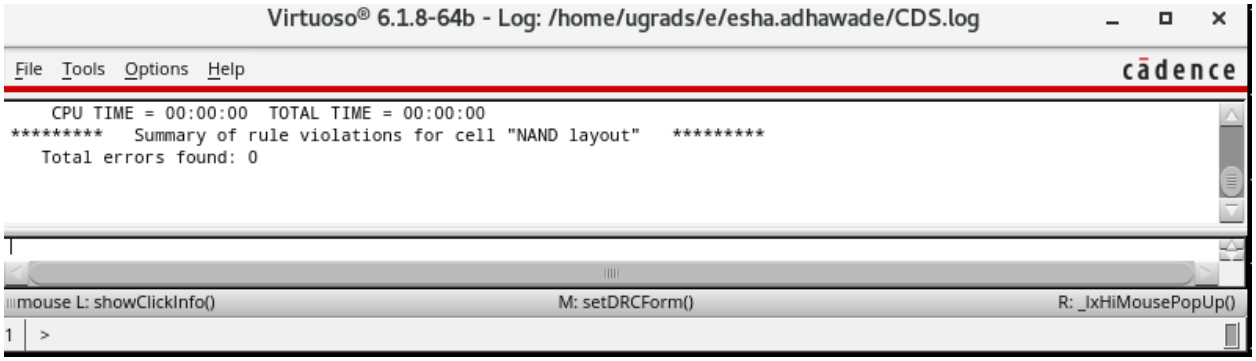
Symbol



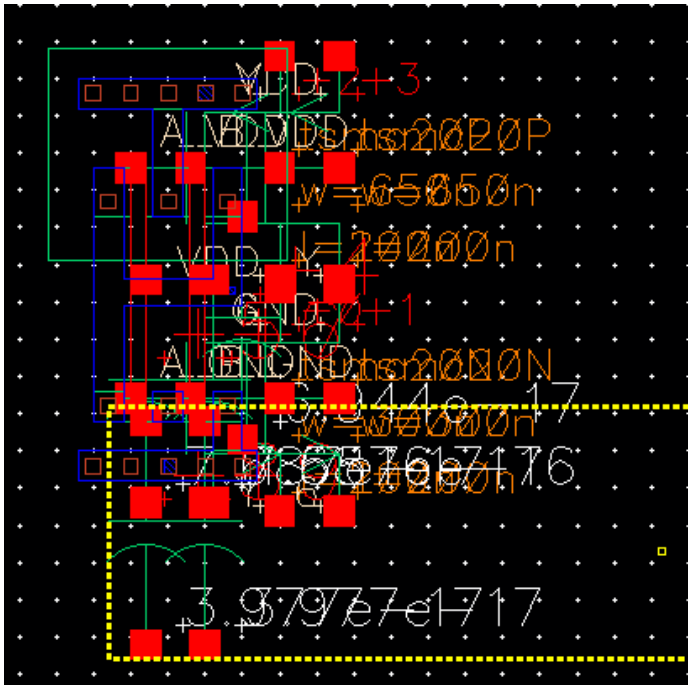
Layout



DRC - match



DRC

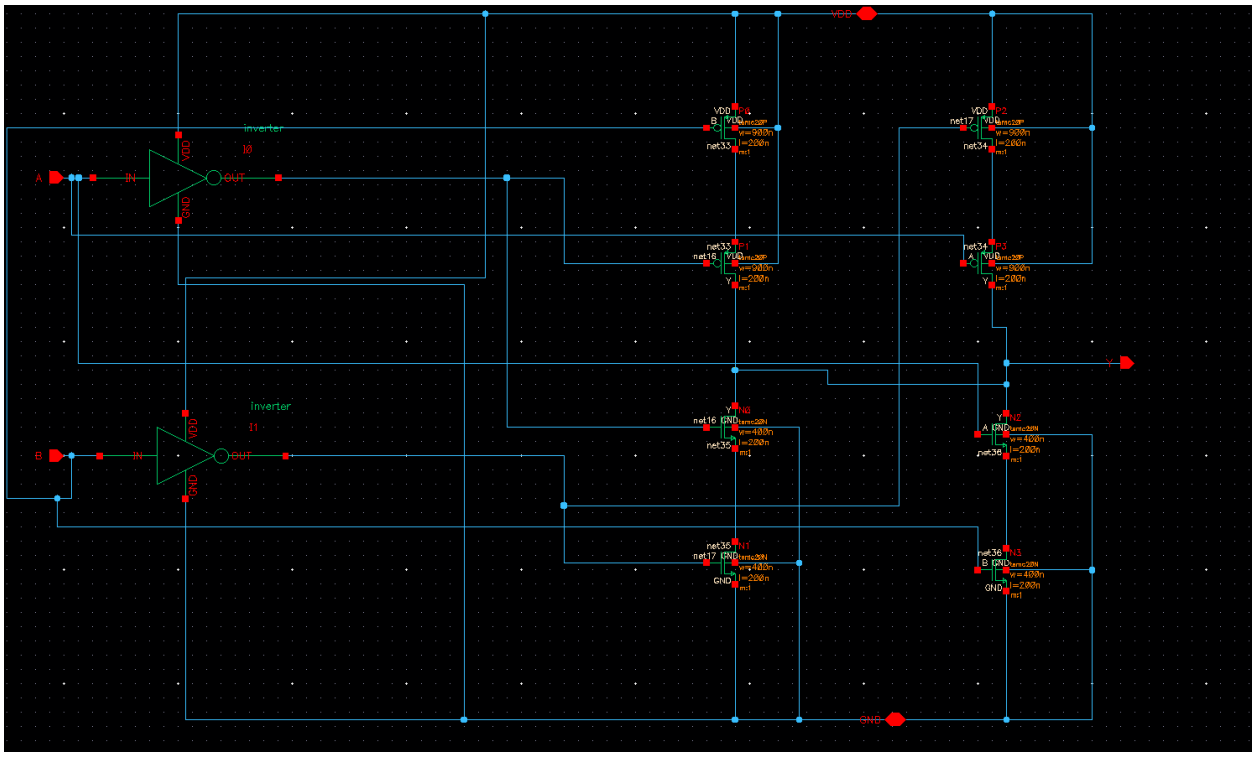


LVS (The net-lists match)

```
@(#)$CDS: LVS version 6.1.8-64b 08/04/2020 19:19 (cpgsrv11) $

Command line: /opt/coe/cadence/IC618/tools.lnx86/dfII/bin/64bit/LVS -dir /home/ugrads/e/esha.adhawade/ecen454_503/LVS -l -s -t /home/ugrads/e/esha.adhawade/ecen454_503/LVS/layout /home/ugrads/e/esha.adhawade/ecen454_503/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /home/ugrads/e/esha.adhawade/ecen454_503/LVS/layout/netlist
       count
         6              nets
         5              terminals
         2              pmos
         2              nmos

    Net-list summary for /home/ugrads/e/esha.adhawade/ecen454_503/LVS/schematic/netlist
       count
         6              nets
         5              terminals
         2              pmos
         2              nmos


    Terminal correspondence points
    N4          N5          A
    N3          N2          B
    N2          N3          GND
    N5          N0          VDD
    N1          N1          Y

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                              instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                                nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  6       6
        total                   6       6

                              terminals
        un-matched              0       0
        matched but
        different type          0       0
        total                   5       5


Probe files from /home/ugrads/e/esha.adhawade/ecen454_503/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:


Probe files from /home/ugrads/e/esha.adhawade/ecen454_503/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:
```

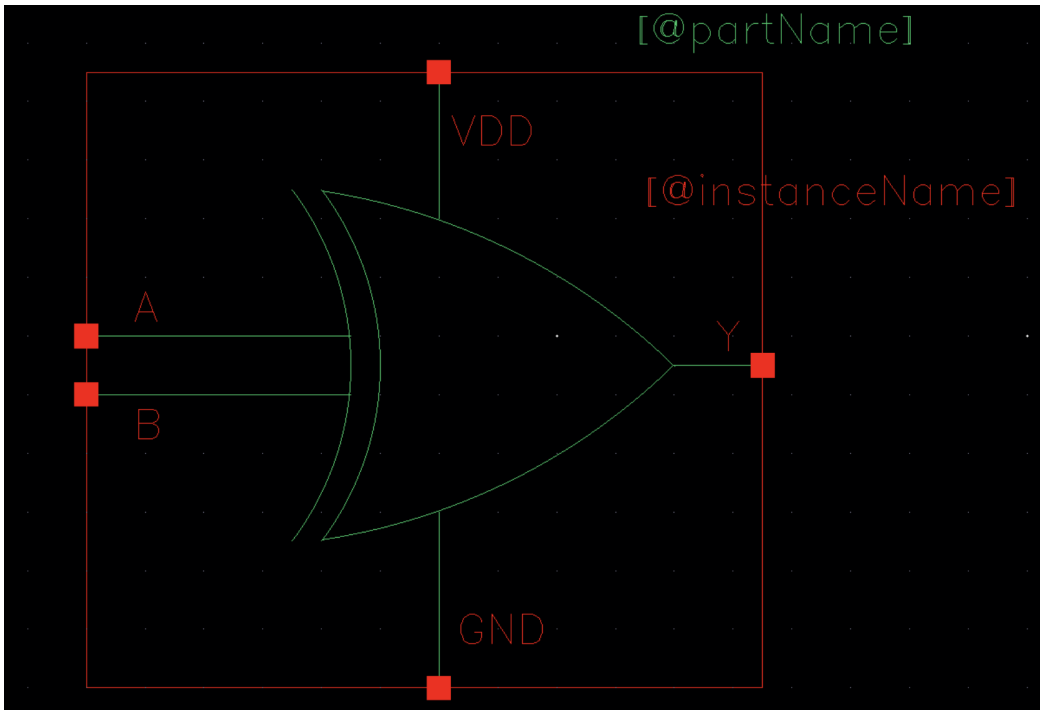
XOR

Schematic

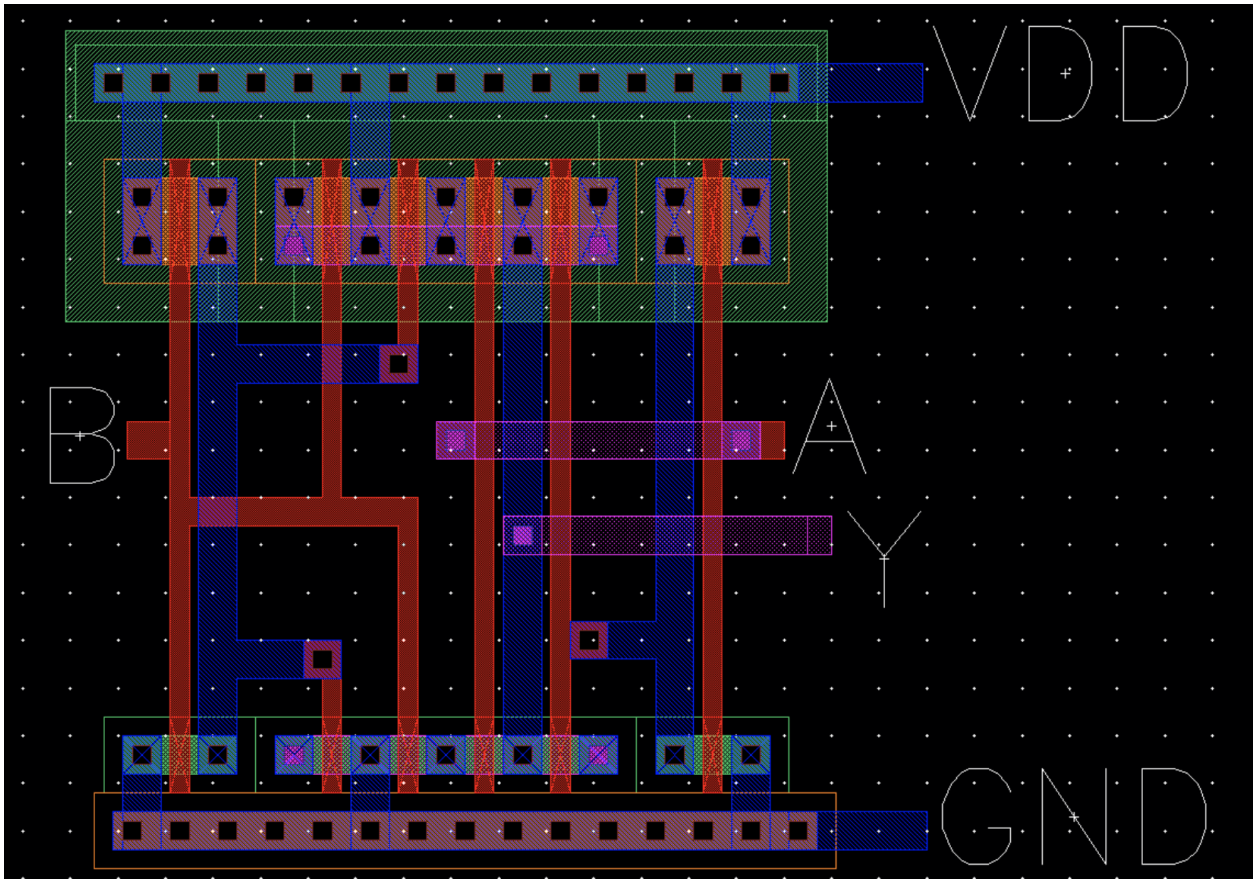


The wire labeling didn't work out so I just directly connect the inputs (A, B, _A (inverse), _B(inverse)) to corresponding terminals in order to pass check and save.

Symbol



Layout

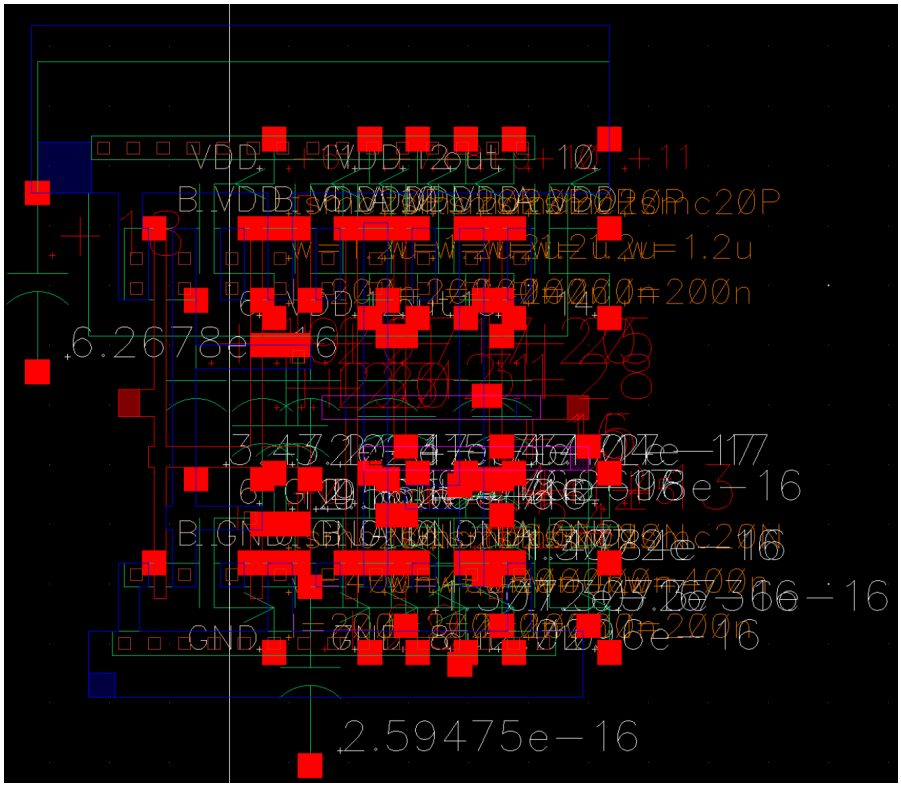


DRC - match

```
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "xor layout"   *********
   Total errors found: 0
```

vvv

DRC



LVS (The net-lists match)

```
    Terminal correspondence points
    N3          N1          A
    N2          N3          B
    N1          N2          GND
    N5          N0          VDD
    N4          N4          out

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
        active                   4       4
        total                    4       4

                                   nets
        un-matched               0       0
        merged                   0       0
        pruned                   0       0
        active                   6       6
        total                    6       6

                                 terminals
        un-matched               0       0
        matched but
        different type           1       1
        total                    5       5
```