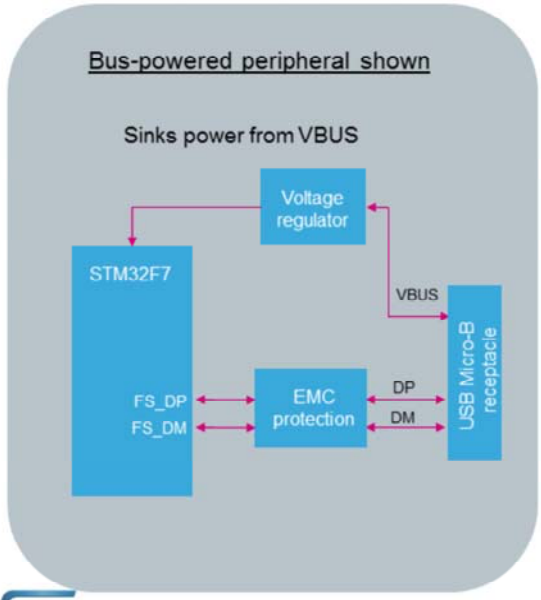
Hello, and welcome to this presentation of the STM32F7 USB Full Speed and High Speed interfaces. It covers all the features of these interfaces, which are widely used to connect either a PC or a USB device to the microcontroller.

Overview

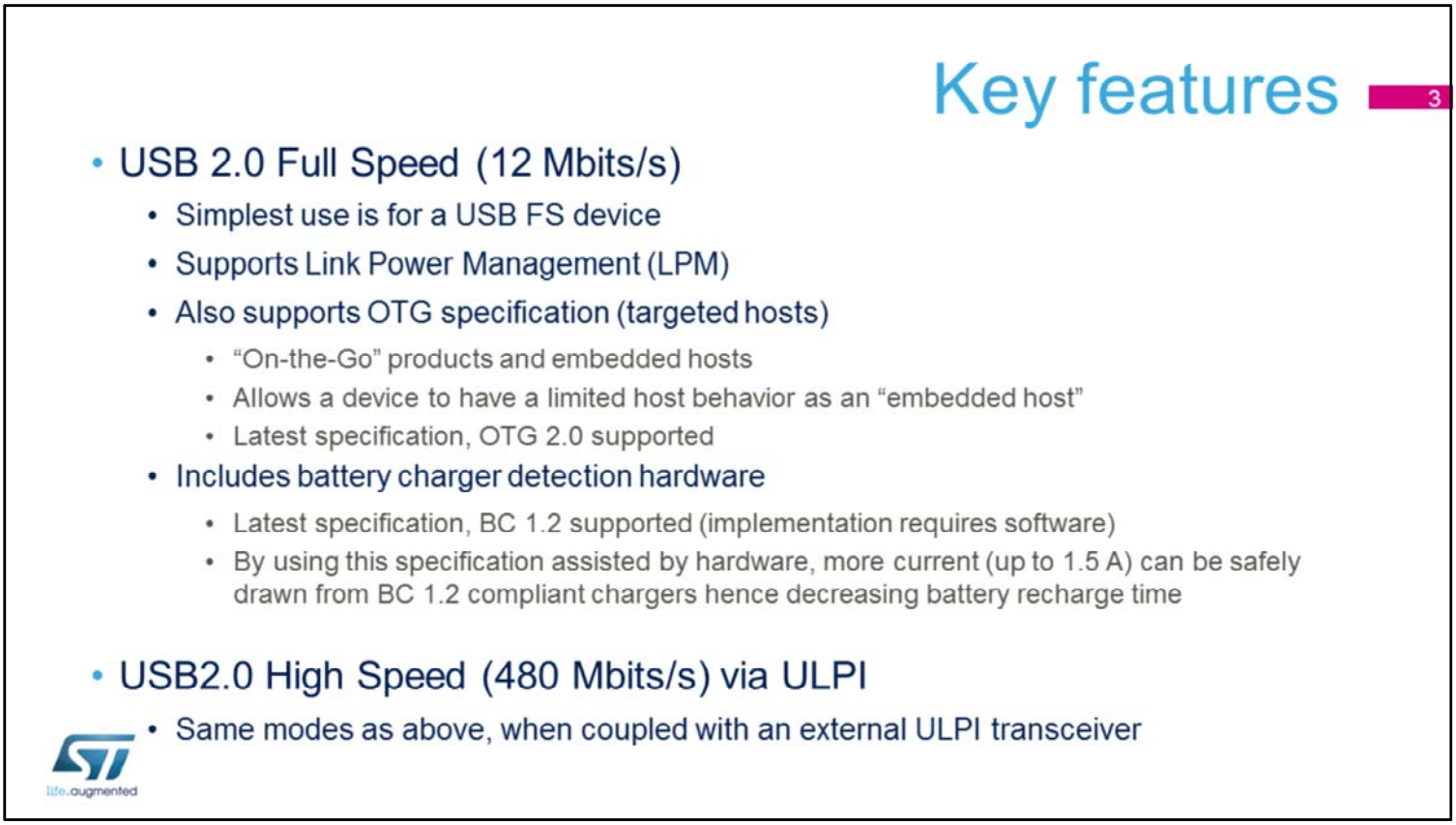


- Provides USB 2.0 Full Speed interface, and also High Speed ULPI interface in some versions
- Supports “On-the-Go” products

Application benefits

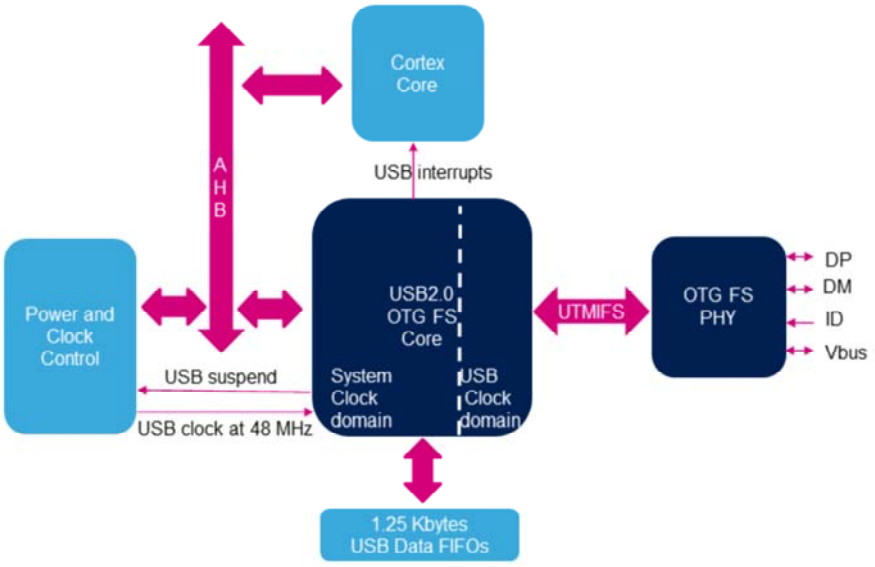
- Low-power implementation
- On-the-Go function
- Quicker charging via Battery Charger Detection

This figure shows the connections between a STM32F7 microcontroller and a USB connector. The STM32F7 features a USB Full Speed communication interface, allowing the microcontroller to communicate typically with a PC or a USB storage device. The simplest implementation is a USB peripheral device but the STM32F7 also supports the USB “On-the-go” functionality.



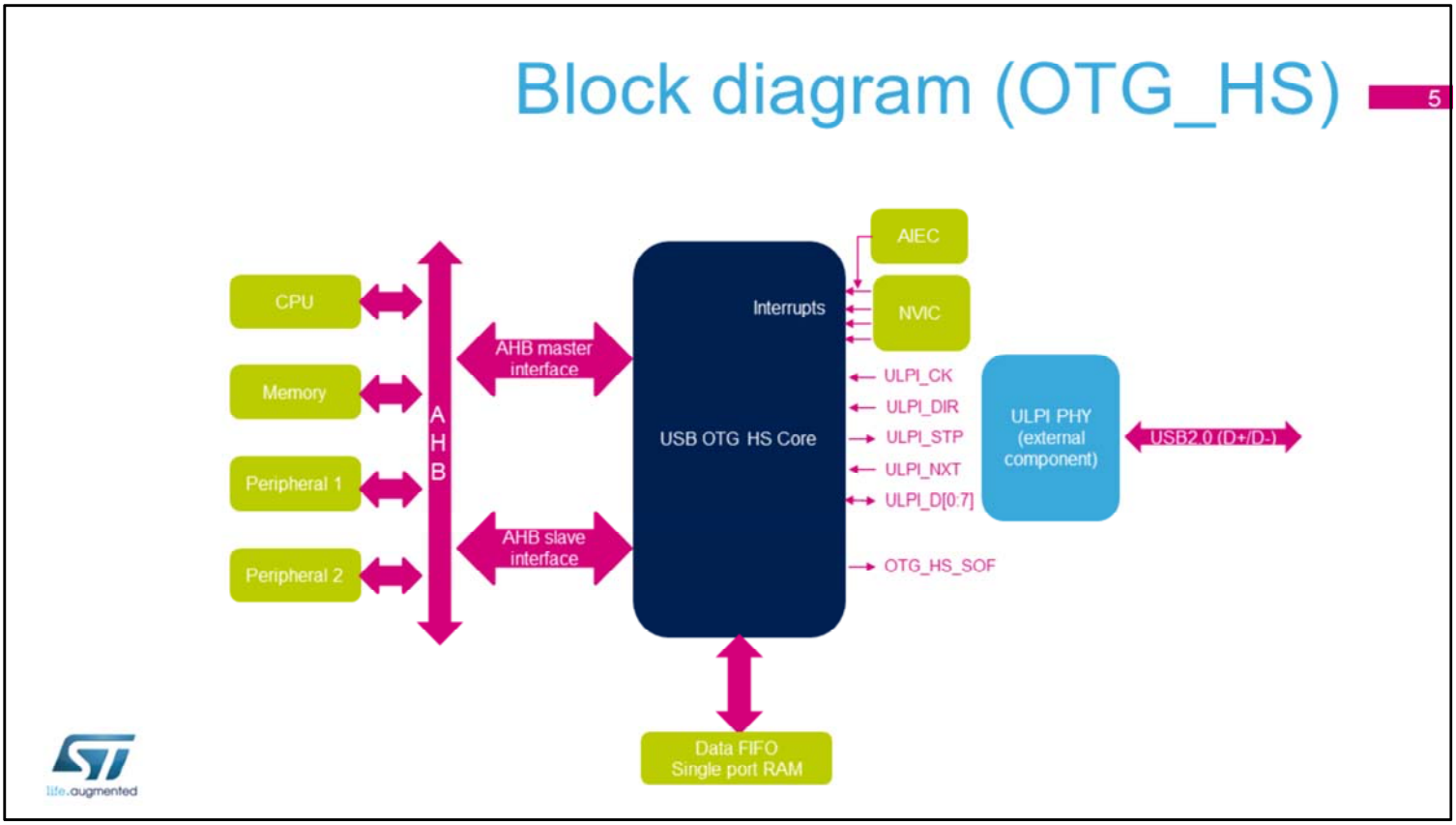
Let's look at some of the key features of this USB full speed interface, which is a USB specification 2.0 compliant interface that operates at a 12 Megabits per second bit rate.
In the simplest form, a USB FS device can be implemented.
Built-in support for Link Power Management adds enhanced power modes on top of the USB 2.0 specification.
In addition, the On-The-Go or "OTG" functionality enables implementation of an OTG product or an embedded host, both of which have the capacity to behave as a targeted host.
The battery charger detection function allows for increased current to be drawn from BC1.2-compliant chargers up to 1.5A.
USB 2.0 High Speed is also available via the ULPI interface. The same modes of operation are possible when coupling with an external ULPI transceiver.

Block diagram (OTG_FS)

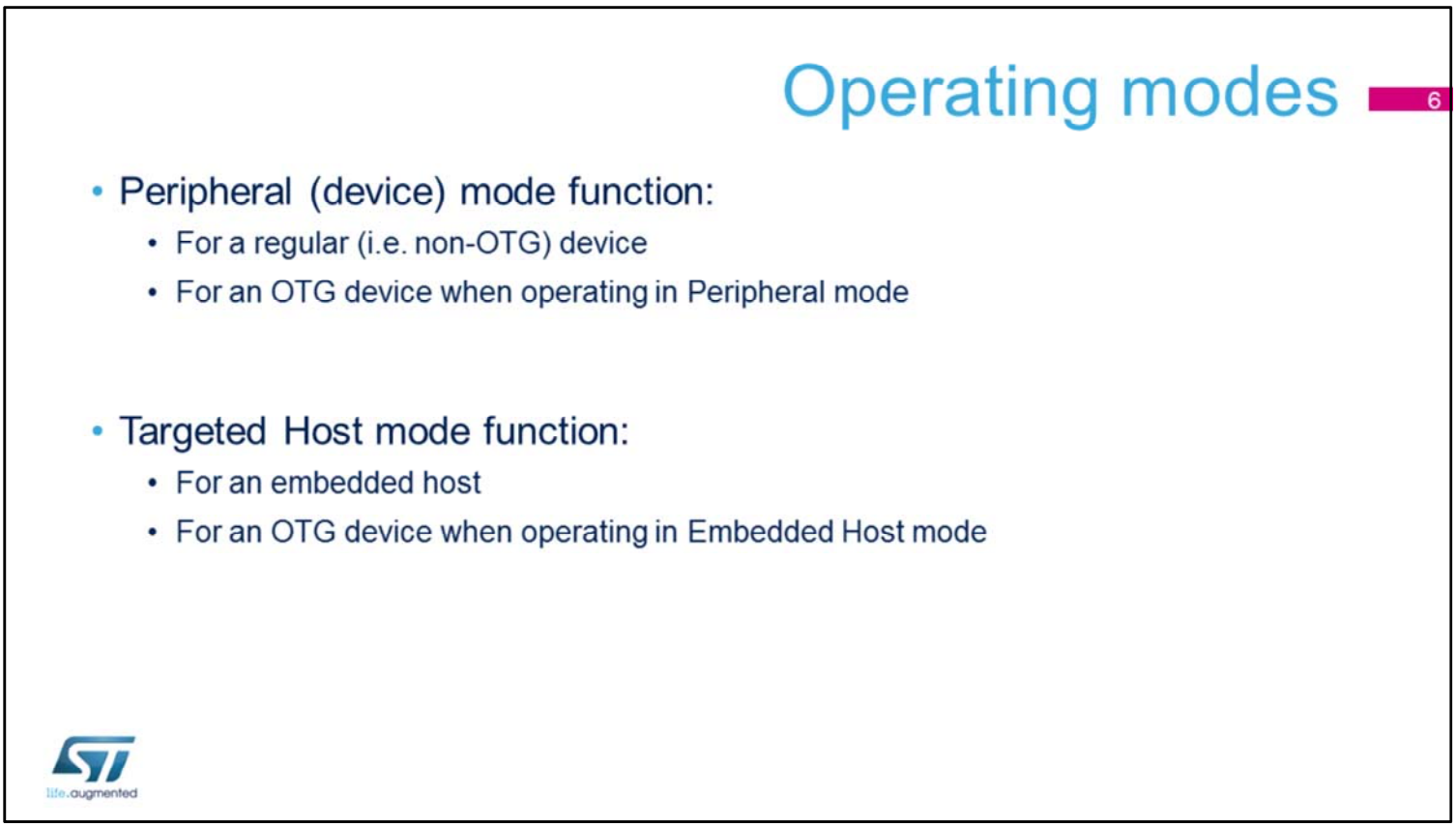


In this block diagram, the USB OTG Full Speed controller core is shown in the center with its data FIFOs below. The Physical Layer, or PHY, on its right side handles the analog signal levels including many specific level detections relating to On-The-Go and Battery Charger detection functions. The USB interrupt goes to the Cortex processor to signal various USB events. The AHB peripheral bus enables read/write access of the controller registers and the Power& Clock control block.

Depending on the use case (i.e. either device only or OTG device), a low- or high-speed crystal oscillator is necessary to provide an accurate timing reference for the USB block.



In this block diagram, the USB OTG High Speed controller core is shown in the center with its data FIFOs below. The PHY on its right side handles the analog signal levels including many specific level detections relating to On-The-Go and Battery Charger detection functions. The USB interrupt goes to the Cortex processor to signal various USB events. The AHB slave interface enables read/write access of the controller registers and the Power& Clock control block. Transfers to and from memory are handled by a DMA engine inside the controller via the AHB master interface.



At any given time, one of the two operating modes will be functional:
- Peripheral mode, which will be used for a regular device or an OTG device when operating in Peripheral mode.
- Targeted host mode, which will be used for an embedded host or an OTG device when operating in Host mode.

Interrupts

Interrupt event	Description
Resume/remote wakeup	Wakeup interrupt during suspend(L2) or LPM(L1) state.
Session request/ new session detected	Host mode: Session request is detected from the device. Device mode: VBUS in the valid range for B-peripheral device.
Disconnect detected	Asserted when a device disconnect is detected.
Connector ID status change	Change in connector ID status
LPM interrupt	Device: receives LPM transaction, responds with non-ERRORed response. Host: device responds to LPM transaction with non-ERRORed response or when host core has completed LPM transactions for programmed number of times.
Periodic Tx FIFO empty	When the periodic transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the periodic request queue.
Host channels interrupt	Interrupt pending on one of the channels of the core (in Host mode).
Host port interrupt	Indicates a change in port status of one of the OTG_FS(/HS) controller ports in Host mode.
Reset detected	In device mode, this interrupt is asserted when a reset is detected on the USB in partial power-down mode when the device is in Suspend mode.

Interrupts from this USB block can be triggered by a large number of events or state changes.
This slide and the following three slides show all the events that can trigger an interrupt. As can be seen, these interrupt sources are diverse; they range from events related to low power management and OTG, to events related to normal host behavior and regular USB reset and disconnect events.

Interrupts (continued)

Interrupt event	Description
Incomplete periodic transfer	Host: when there are incomplete periodic transactions still pending. Device: at least one isochronous OUT endpoint on which the transfer not completed.
Incomplete isochronous IN transfer	At least one isochronous IN endpoint on which the transfer is not completed in the current frame.
OUT endpoint interrupt	Interrupt is pending on one of the OUT endpoints of the core (in Device mode).
IN endpoint interrupt	Indicates that an interrupt is pending on one of the IN endpoints of the core (in Device mode).
End of periodic frame interrupt	Period specified in the periodic frame interval field has been reached in the current frame.
Isochronous OUT packet dropped interrupt	Failed to write an isochronous OUT packet into the Rx FIFO because the Rx FIFO does not have enough space to accommodate a maximum size packet for the isochronous OUT endpoint.
Enumeration done	Speed enumeration is complete.
USB reset	Device mode: A reset is detected on the USB (N.B. when not in partial Power-down mode).

In this second slide showing interrupts, another diverse set of sources is described.

Interrupts (continued)

Interrupt event	Description
USB suspend	Suspend was detected on the USB.
Early suspend	Idle state has been detected on the USB for 3 ms.
Global OUT NAK effective	Set global OUT NAK bit, set by the application, has taken effect in the core.
Global IN non-periodic NAK effective	Set global non-periodic IN NAK bit, set by the application, has taken effect in the core.
Non-periodic Tx FIFO empty	Non-periodic Tx FIFO is either half or completely empty.
Rx FIFO non-empty	At least one packet pending to be read from the Rx FIFO.
Start of frame	Host mode: core sets this bit to indicate that an SOF (FS), or Keep-Alive (LS) is transmitted on the USB. Device mode: core sets this bit to indicate that an SOF token has been received on the USB.
OTG interrupt	OTG protocol event.
Mode mismatch interrupt	Host mode register access, when the core is operating in Device mode (and vice versa).

In this third slide describing interrupt sources, many SUSPEND, OTG functions and FIFO status events are listed as well as a general register access error.

Low-power modes (OTG_FS)

Mode	Description
PHY: power down	Switches on/off the full-speed transceiver module of the PHY.
PHY: Vbus detection	Switches on/off the VBUS sensing comparators associated with OTG operations.
Suspend: Stop PHY clock	Most of the 48 MHz clock domain internal to the OTG full-speed core is switched off by clock gating.
Suspend: Gate HCLK	Most of the system clock domain internal to the OTG full-speed core is switched off by clock gating.
Suspend: USB system stop	Application may decide to drastically reduce the overall power consumption by a complete shut down of all the clock sources in the system.

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Now let's take a brief look at the various low-power modes of the PHY and the controller.
For the PHY, power down mode can be used for example when there is no VBUS present and session is identified to be not OTG ; it is also possible to disable the VBUS sensing related to OTG (A- and B- sessions) if the OTG function is not used.
During SUSPEND mode, there is no dynamic signaling occurring over the USB interface, so three different controls are offered to lower the power consumption as desired by the application.

Low-power modes (OTG_HS)

Mode	Description
Suspend: Gate HCLK	Most of the system clock domain internal to the OTG high-speed core is switched off by clock gating.
Suspend: USB system stop	Application may decide to drastically reduce the overall power consumption by a complete shut down of all the clock sources in the system.

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Low-power modes for the High Speed core are similar to the Full Speed, but the modes concerning the PHY are not listed as in this case the PHY (or transceiver) is an external component.

Low-power modes

MCU mode	Description	USB availability
Run	MCU fully active.	Required until USB enters Suspend mode.
Sleep	Peripheral interrupts cause the device to exit Sleep mode. Peripheral registers content is kept.	Available while USB is in Suspend mode.
Stop	Peripheral interrupts cause the device to exit Stop mode. Peripheral registers content is kept.	Available while USB is in Suspend mode, offers optimal power reduction.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.	Not compatible with USB applications.

The USB peripheral is active in Run and Sleep modes. In Stop mode, the USB is not available but the contents of its registers are kept. In Standby mode, the USB peripheral is powered-down and must be reinitialized when returning to a higher power state.

Debug information

- A few dedicated bits are implemented to assist debugging of
  - USB receive data FIFO status/contents (both host and device modes)
  - Host mode: periodic queue scheduling

Debug bit	Description
OTG_FS(/HS) Receive status debug read / OTG status read and pop registers	Special read FIFO access for debug.
Top of the periodic transmit request queue	Indicates the entry in the periodic Tx request queue that is currently being processed by the MAC.

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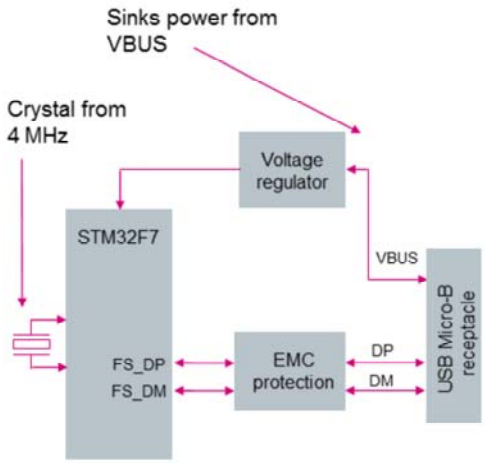
Within the USB module, certain dedicated bits are implemented to allow debug functionality in a USB application.
They relate to FIFO status and contents and the scheduling of periodic queues in Host mode.
Additional details of these debug bits are listed in this table.

Application: low-power device



- The schematic shows an example of a low-power design for a “device only” application
- In this example, the device is bus powered, drawing power only from USB VBUS
- A single 4 MHz crystal oscillator can be used

Here is an application example of a low-power device.
Power is drawn directly from the USB VBUS signal.
A single crystal oscillator (starting from 4 MHz) is needed outside.

References

- For more details, please refer to the following source pages:
  - www.usb.org : usb20_docs (hosts a ZIP file containing):
    - USB2.0 specification
    - On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification (USB2), latest version 1.1a
    - USB 2.0 ECN: Link Power Management Addendum
  - www.usb.org : devclass_docs
    - Battery Charger v1.2 specification

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For complete USB specification documents, please refer to USB.org.
USB2.0 document home page has a ZIP file containing the USB2.0 and OTG2.0 specifications and an ECN for LPM
The USB device class documents page has the battery charger specification.