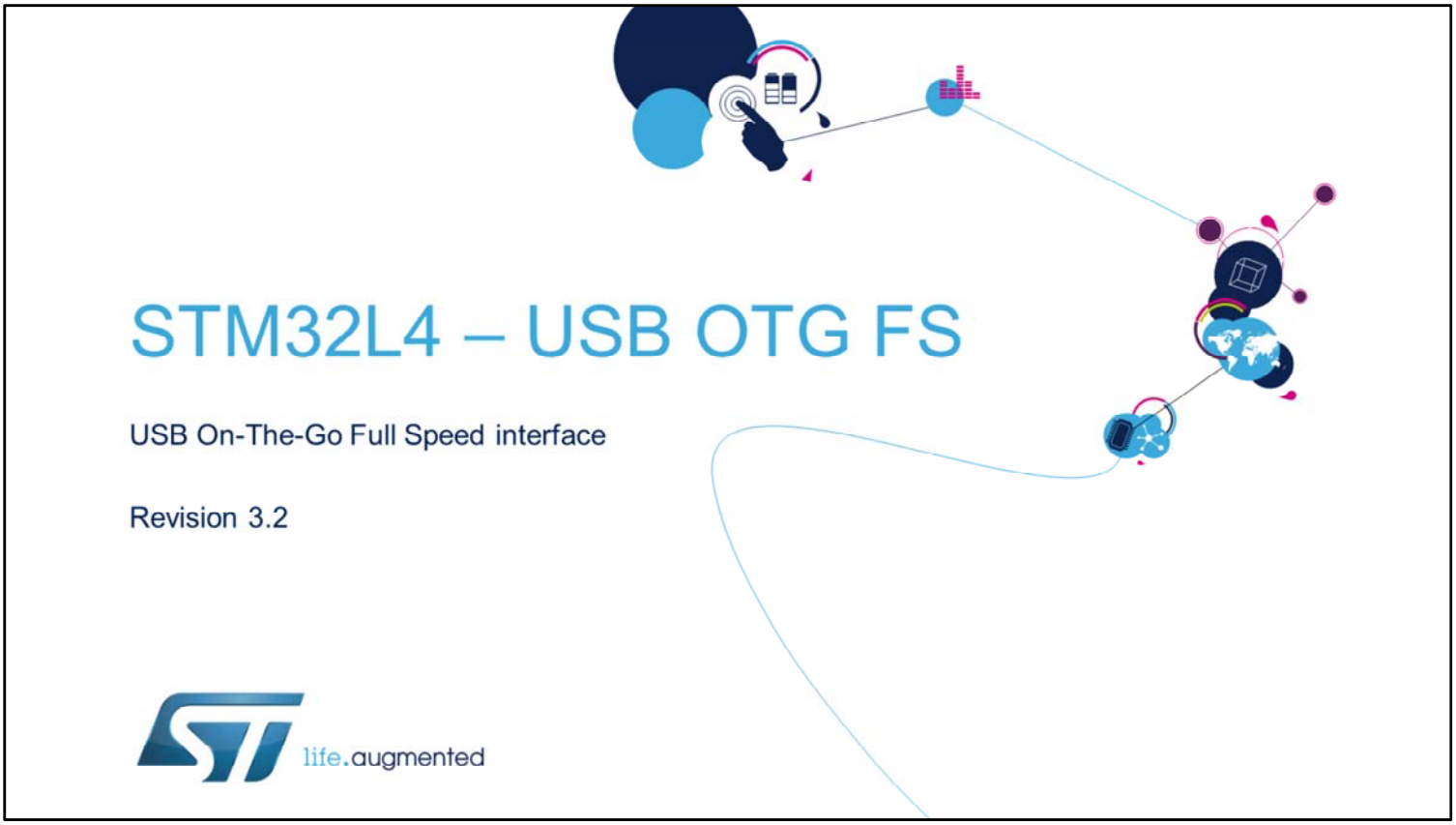

Hello, and welcome to this presentation of the STM32L4's USB interface. It covers the features of this IP, which is widely used to connect either a PC or a USB device to the microcontroller.

Scope

- In the STM32L4 family there are products offering various levels of USB functionality
- The different options are summarized in the table below, which also shows the products for which this section is relevant

Line	USB functionality	Scope
STM32L496/4A6	**OTG full speed (XTAL-less in special cases)**	**Covered now**
STM32L476/486 STM32L475	**OTG full speed**	
STM32L452/462 STM32L432/442 STM32L433/443 STM32L412/422	USB full speed device, XTAL-less	Covered in a different presentation

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This slide explains the scope of this chapter within the STM32L4 product line.
As can be seen in the table, we are now about to describe the USB full speed device interface, supported in STM32L49x/4Ax and STM32L47x/48x products.

Crystal-less device feature

3

- STM32L496/4A6, STM32L476/486, STM32L475 devices offer operation with a low-frequency crystal e.g. 32.768 kHz
- STM32L496/4A6 devices offer the possibility of working without any crystal for USB device implementations

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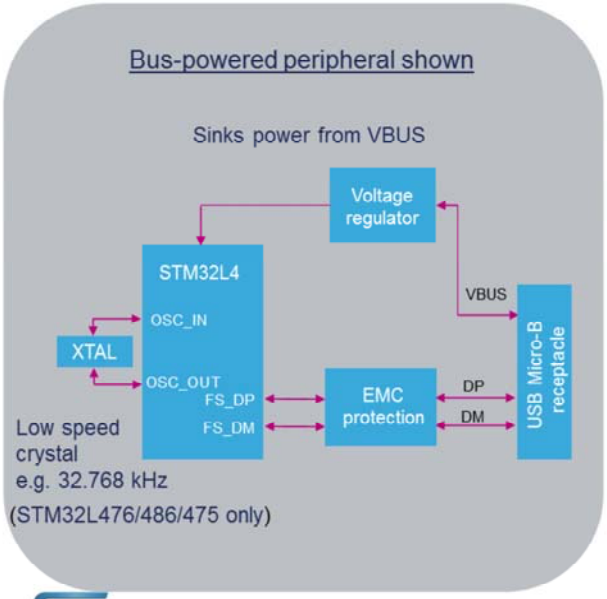
All devices with this functionality offer operation with a low frequency crystal.
STM32L496/4A6 devices also allow a USB device to be implemented without any crystal.

Overview



- Provides USB 2.0 Full Speed interface
  - Full-speed peripheral to “On-the-Go“ product

Application benefits

- Low-power implementation
- On-the-Go function
- Battery charger detection allowing more efficient charging thanks to chargers recognition

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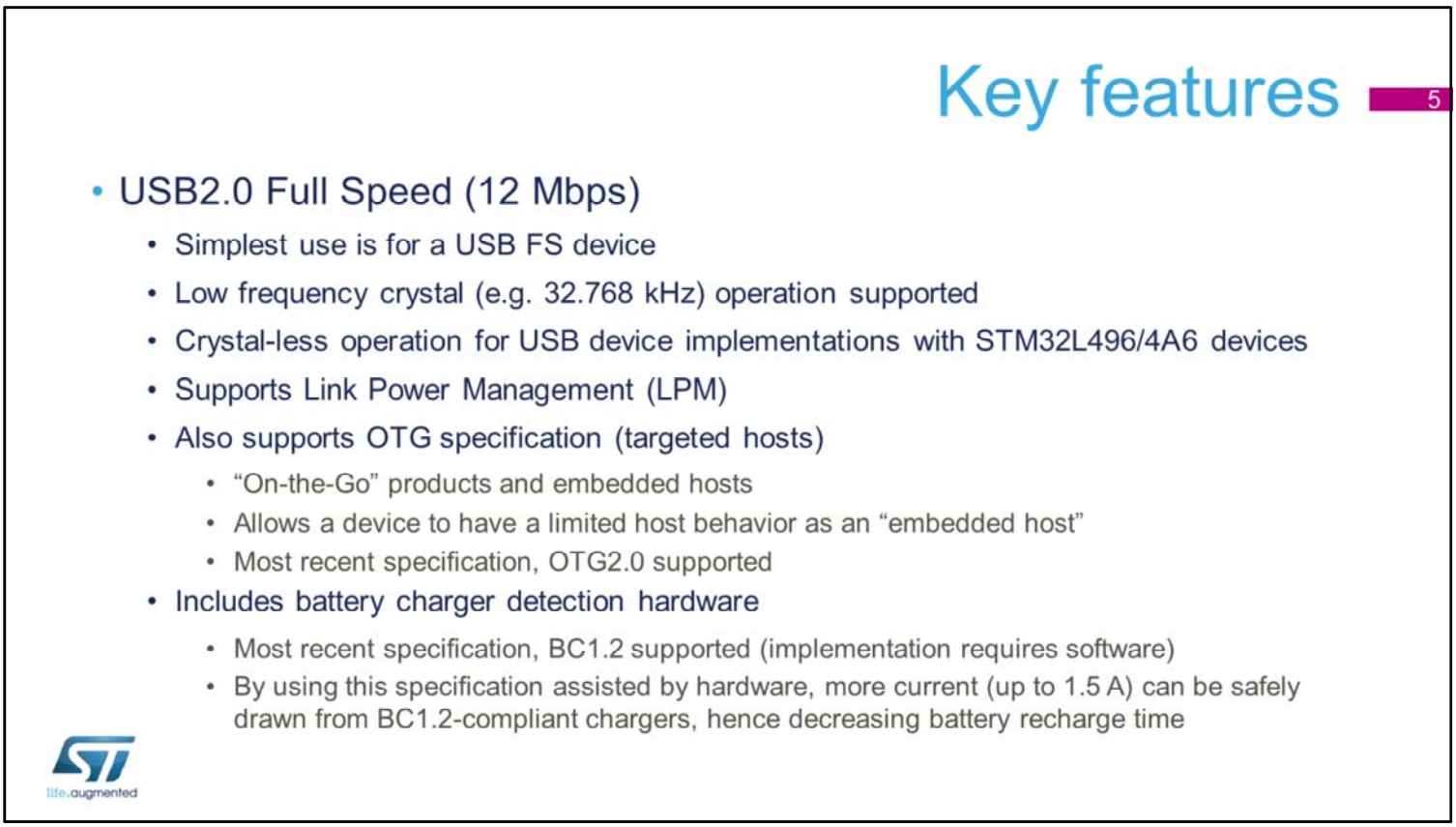
This figure shows the simplest connections between an STM32L4 microcontroller and a USB connector, in a peripheral configuration.
The STM32L4 features a Full-speed USB communication interface, allowing the microcontroller to communicate typically with a PC or a USB storage device. The simplest implementation is a USB peripheral device but the STM32L4 also supports “On-The-Go” USB functions.
The USB implementation includes low-power features allowing the use of a low-speed crystal oscillator, On-The-Go host or device functions, and a battery charger detection allowing more efficient charging possibilities.



This slide summarizes the key features of this full-speed USB interface, which is a USB specification 2.0 compliant interface operating at a 12 Megabits per second bit rate.
In the simplest form, a full-speed USB device can be implemented.
Low frequency crystal operation is possible, and STM32L496/4A6 devices can work crystal-less.
Its built-in support for Link Power Management adds enhanced power modes on top of the USB 2.0 specification.
In addition, the On-The-Go or "OTG" function enables the implementation of an OTG product or an embedded host, both of which have the capacity to behave as a targeted host.
The battery charger detection feature allows for increased current to be drawn from BC1.2 compliant

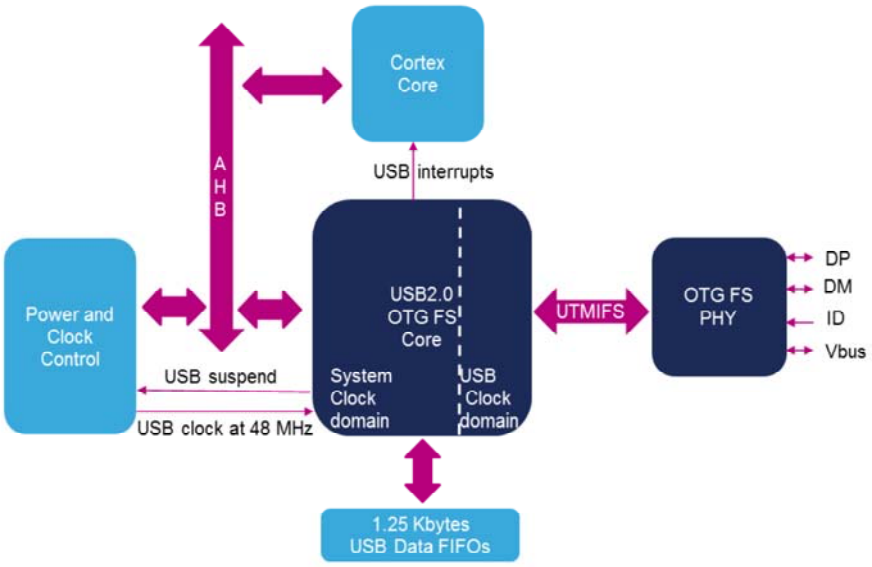
chargers up to 1.5 A.

Block diagram (OTG_FS)

External components (clock source)

Device only:
Can use only Low Speed Oscillator (32.768 kHz)

OTG device:
Uses High Speed Oscillator (4 to 48 MHz)

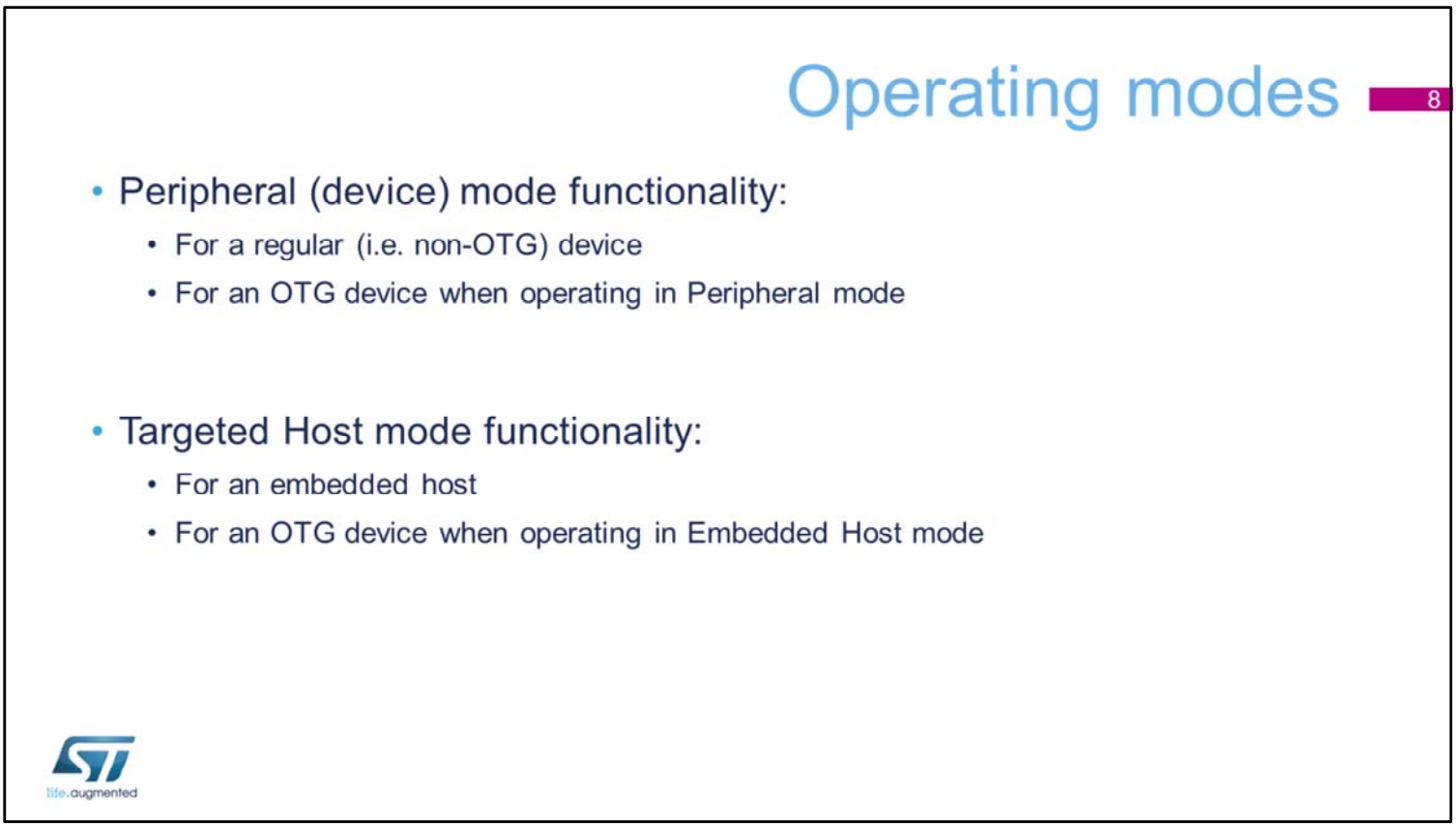


In this block diagram, the USB OTG Full Speed controller core is shown in the center with its data FIFOs below. The Physical Layer, or PHY, on its right side handles the analog signal levels including many specific level detections relating to On-The-Go and Battery Charger detection functions. The USB interrupt goes to the Cortex processor to signal various USB events. The AHB peripheral bus enables read/write access of the controller registers and the Power& Clock control block.

Related peripherals

- CRS (clock recovery system) – STM32L496/4A6 devices only
  - The remote host's start of frame (SOF) timing is extracted from the device controller and the CRS can use it to drive the internal clock generator (HSI RC 48 MHz) allowing USB timing requirements to be met without an external crystal
- NVIC (interrupts)
  - A single interrupt line is connected to the NVIC to generate events
- EXTI (events)
  - A single event line is connected to the EXTI to enable the system to be woken from STOP mode when the USB activity resumes (leaving suspend mode)

Several related peripherals work in conjunction with the USB device controller to link the USB activity to the system power mode and the requirements of the software.
The clock recovery system allows operation without an external crystal, using the integrated HSI oscillator as the main clock source.
The interrupt events are sent to the non-vectored interrupt controller via a single line.
The system events can cause the system to wakeup from STOP mode, for example at the moment we resume from USB suspend.



At any given time, one of the two operating modes will be in operation:

- Peripheral mode, used for a regular device or an OTG device.
- Targeted host mode, used for an embedded host or an OTG device.

Interrupts

Interrupt event	Description
Resume/remote wakeup	Wakeup interrupt during Suspend (L2) or LPM (L1) state.
Session request/ new session detected	Host mode: Session request is detected from the device. Device mode: VBUS in the valid range for B-peripheral device.
Disconnect detected	Asserted when a device disconnect is detected.
Connector ID status change	Change in connector ID status
LPM interrupt	Device: receives LPM transaction, responds with non-ERRORed response. Host: device responds to LPM transaction with non-ERRORed response or when host core has completed LPM transactions for programmed number of times.
Periodic Tx FIFO empty	When the periodic transmit FIFO is either half or completely empty and there is space for at least one entry to be written in the periodic request queue.
Host channels interrupt	Interrupt pending on one of the channels of the core (in Host mode)
Host port interrupt	Indicates a change in port status of one of the OTG_FS controller ports in Host mode
Reset detected	In Device mode, this interrupt is asserted when a reset is detected on the USB in partial power-down mode when the device is in Suspend mode

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Interrupts from this USB block can be triggered by a large number of events or state changes.
This slide and the following three slides show all the events that can trigger an interrupt. As can be seen, these interrupt sources are diverse; they range from events related to low power management and OTG, to events related to normal host behavior and regular USB reset and disconnect events.

Note in slide: Reset detected: In Device mode, this interrupt is asserted when a reset is detected on the USB in partial power-down mode when the device is in Suspend mode.

Interrupts (continued)

Interrupt event	Description
Incomplete periodic transfer	Host: when there are incomplete periodic transactions still pending Device: at least one isochronous OUT endpoint on which the transfer not completed
Incomplete isochronous IN transfer	At least one isochronous IN endpoint on which the transfer is not completed in the current frame
OUT endpoint interrupt	Interrupt is pending on one of the OUT endpoints of the core (in Device mode)
IN endpoint interrupt	Indicates that an interrupt is pending on one of the IN endpoints of the core (in Device mode).
End of periodic frame interrupt	Period specified in the periodic frame interval field has been reached in the current frame
Isochronous OUT packet dropped interrupt	Failed to write an isochronous OUT packet into the Rx FIFO because the Rx FIFO does not have enough space to accommodate a maximum size packet for the isochronous OUT endpoint
Enumeration done	Speed enumeration is complete
USB reset	Device mode: A reset is detected on the USB (N.B. when not in partial power-down mode)

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In this second slide showing interrupts, another diverse set of sources is described.

Interrupts (continued)

Interrupt event	Description
USB suspend	Suspend was detected on the USB
Early suspend	Idle state has been detected on the USB for 3 ms.
Global OUT NAK effective	Set global OUT NAK bit, set by the application, has taken effect in the core
Global IN non-periodic NAK effective	Set global non-periodic IN NAK bit, set by the application, has taken effect in the core
Non-periodic Tx FIFO empty	Non-periodic Tx FIFO is either half or completely empty
Rx FIFO non-empty	At least one packet pending to be read from the Rx FIFO
Start of frame	Host mode: core sets this bit to indicate that an SOF (FS), or Keep-Alive (LS) is transmitted on the USB. Device mode: core sets this bit to indicate that an SOF token has been received on the USB.
OTG interrupt	OTG protocol event
Mode mismatch interrupt	Host mode register access, when the core is operating in Device mode (and vice versa)

In this third slide describing interrupt sources, many SUSPEND, OTG functions and FIFO status events are listed as well as a general register access error.

Low-power modes

MCU mode	Description	USB availability
Run	MCU fully active.	Required until USB enters Suspend mode.
Sleep	Peripheral interrupts cause the device to exit Sleep mode. Peripheral registers content is kept.	Available while USB is in Suspend mode.
Stop 0,1	Peripheral interrupts cause the device to exit Stop mode. Peripheral registers content is kept.	Available while USB is in Suspend mode, offers optimal power reduction.
Stop 2	Peripheral interrupts cause the device to exit Stop mode. Peripheral registers content is kept.	Not compatible with USB applications.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.	Not compatible with USB applications.

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The USB peripheral is fully active in Run mode. After a SUSPEND event, Sleep mode and Stop 0 and 1 modes are available and the contents of its registers are kept. Stop 2 and Standby modes should not be used.

Debug information

- A few dedicated bits are implemented help debug:
  - USB receive data FIFO status/contents (in both Host and Device modes)
  - Host mode: periodic queue scheduling

Debug bit	Description
OTG_FS Receive status debug read / OTG status read and pop registers	Special read FIFO access for debug.
Top of the periodic transmit request queue	Indicates the entry in the periodic Tx request queue that is currently being processed by the MAC.

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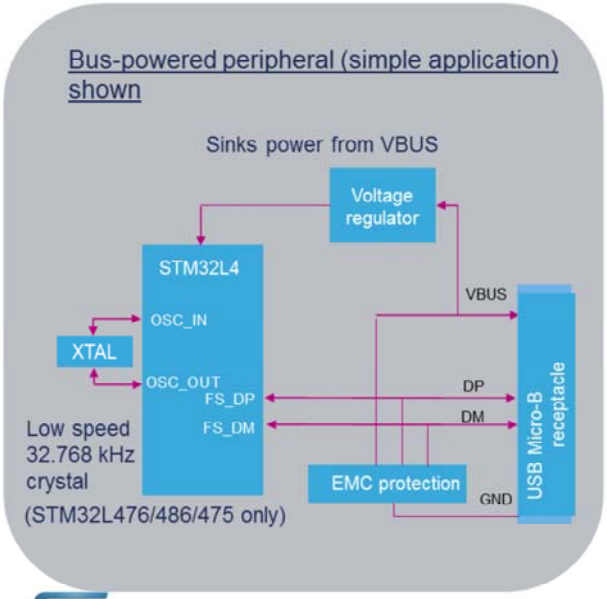
Within the USB module, dedicated bits are implemented to provide some debug functions for USB applications. They relate to FIFO status and contents and the scheduling of periodic queues in Host mode. Additional details of these debug bits are listed in this table.

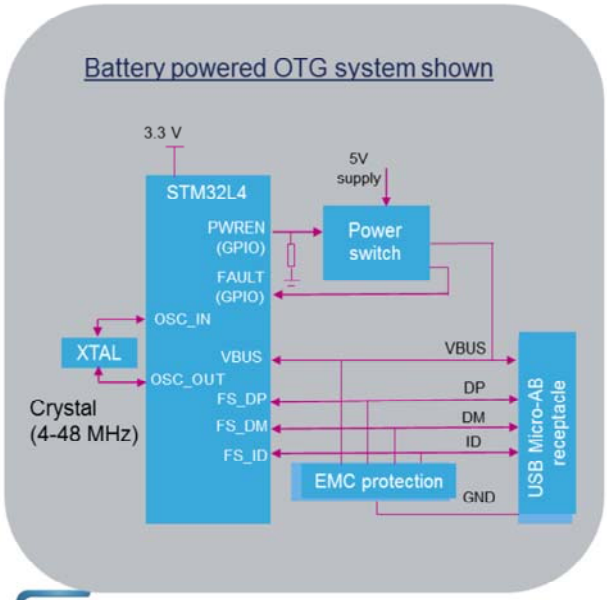
Application 1: Low-power peripheral device



- The schematic shows a low power design for a “device only” application example
- Crystal requirements:
  - STM32L476/486/475 : A single 32.768 kHz crystal oscillator
  - STM32L496/4A6 : Crystal-less operation

Here is an application example of a low-power device. Power is drawn directly from the USB VBUS signal. A single low-speed crystal oscillator at 32.768 kHz is needed outside. A scheme is implemented inside the microcontroller using this low-speed crystal oscillator to trim the internal 48 MHz oscillator, thus giving the required frequency accuracy to comply with the USB specification.

Application 2: Battery-powered OTG solution



- The schematic shows a low-power design for an OTG battery-powered application
- The STM32L4 controls the power switch in order to supply VBUS when required, and monitors for an over-current fault condition
- A regular high-speed crystal (4-48 MHz) is required
- Should dead battery support be required, VBUS should be connected to the STM32L4 via a resistor divider

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Here is a second application example showing a battery-powered OTG solution.
The STM32L4 controls a power switch supplying VBUS to the receptacle, and monitors for faults on the supply.
In this example, a regular crystal oscillator should be used.
Should dead battery support be required, VBUS should be connected to the STM32L4 via a resistor divider.

References

- For more details, please refer to following source pages
  - www.usb.org : usb20_docs (hosts a ZIP file containing):
    - USB 2.0 specification
    - On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification (USB2), latest version 1.1a
    - USB 2.0 ECN: Link Power Management Addendum
  - www.usb.org : devclass_docs
    - Battery Charger v1.2 specification
- Additional information can be found in the applications notes below:
  - Application note AN4879: USB hardware and PCB guidelines using STM32 MCUs
  - Application note AN4775: Basics and low-cost solution proposals to move from legacy USB2.0 connector to USB Type-C™ connector with STM32 devices

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For complete USB specification documents, please refer to USB.org.
USB2.0 document home page has a ZIP file containing the USB2.0 and OTG2.0 specifications and an ECN for LPM
The USB device class documents page has the battery charger specification.
Additional information can also be found in these applications notes.