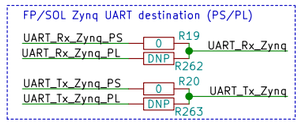
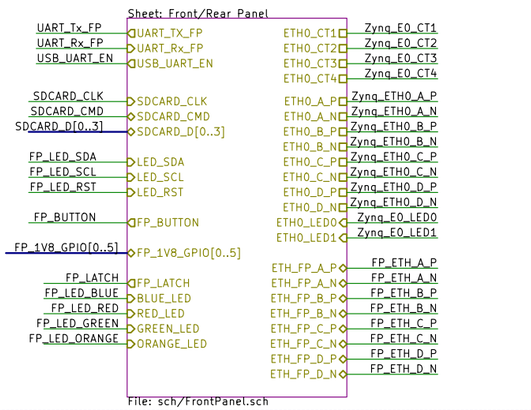
Comm & Control

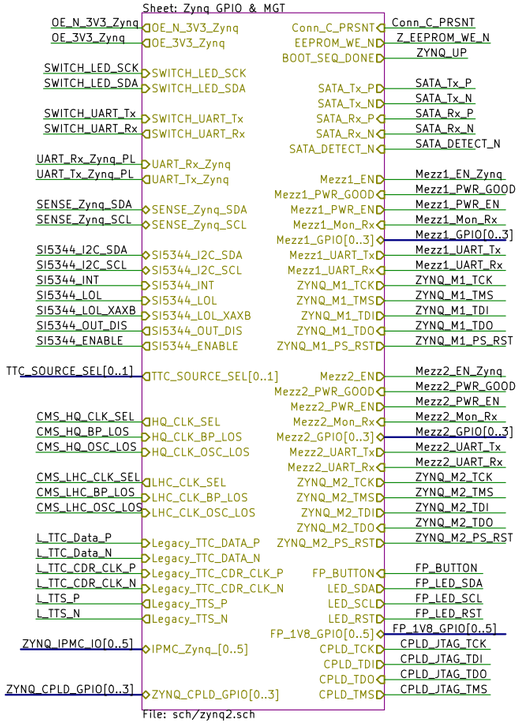
Zynq conf & PS



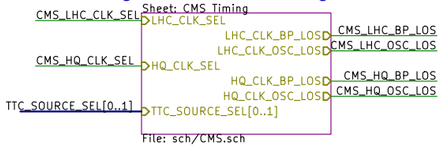
FP / RTM

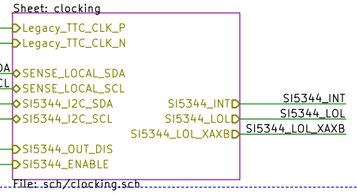


FPGA IO & MGBT

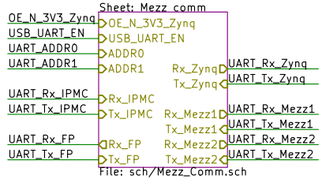


Clocking and CMS Timing

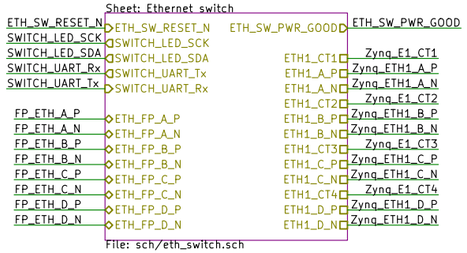




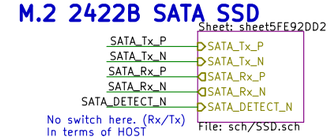
UART Comm



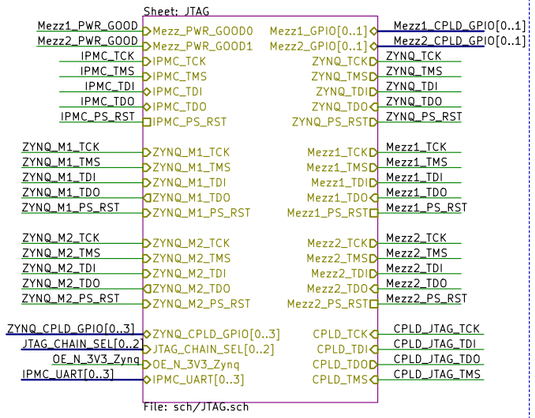
Ethernet



M.2 2422B SATA SSD

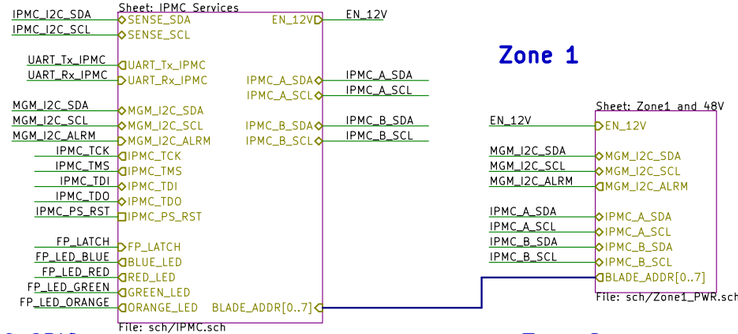


JTAG



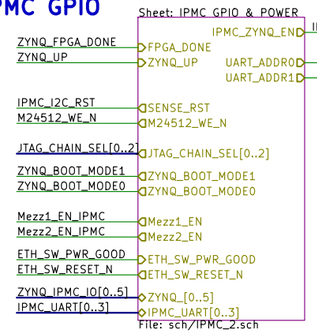
ATCA Infrastructure

IPMC Core IO

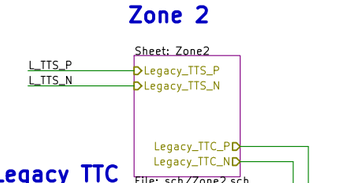


Zone 1

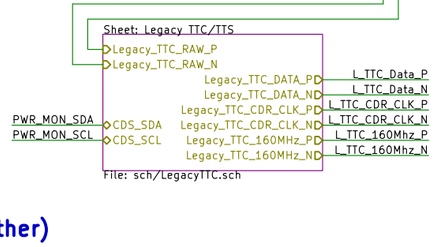
IPMC GPIO



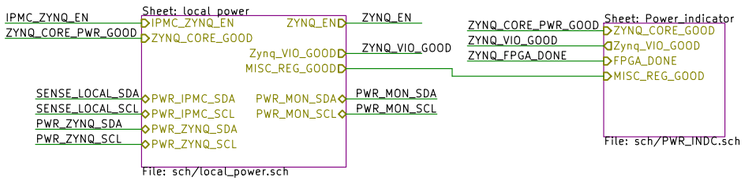
Zone 2



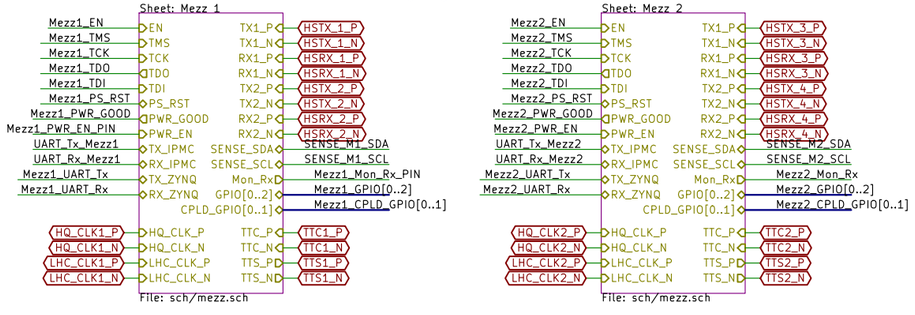
Legacy TTC



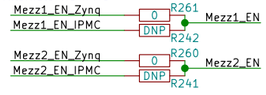
Local Power (12V->other)



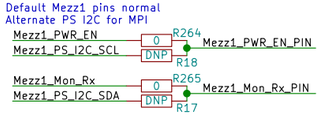
Command Module(s)



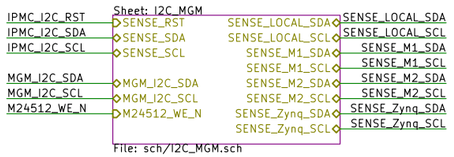
Default Mezz enable via zynq
Alternate via IPMC



Default Mezz1 pins normal
Alternate PS I2C for MPI



IPMC I2C

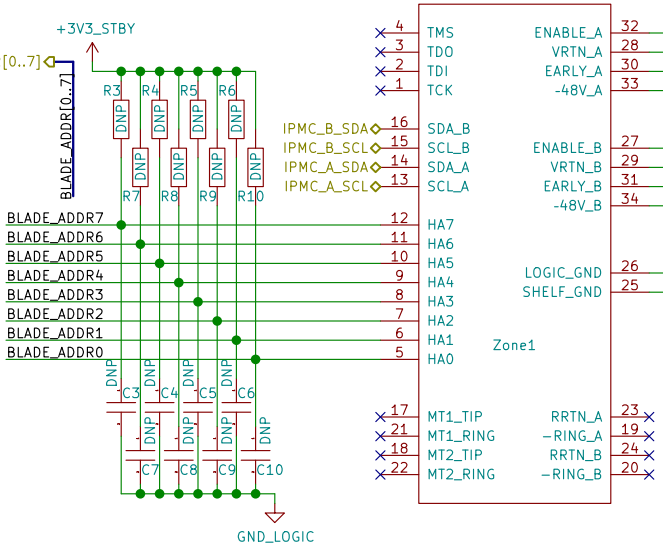


Mounting + Key HW

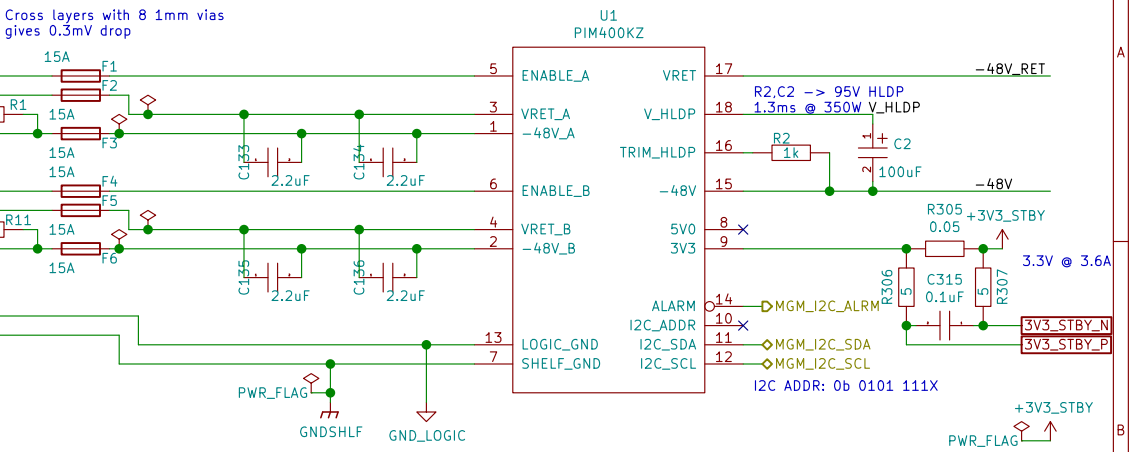
When using DRC, ignore:
Unspecified pin connected to anything
Open collector connected to unspecified
Power output to bidirectional or unspecified
Power input to unspecified

Sheet: /	
File: carrier.sch	
Title:	
Size: B	Date:
KiCad E.D.A. kicad 5.1.9+dfsg1-1	**Rev:** Id: 1/51

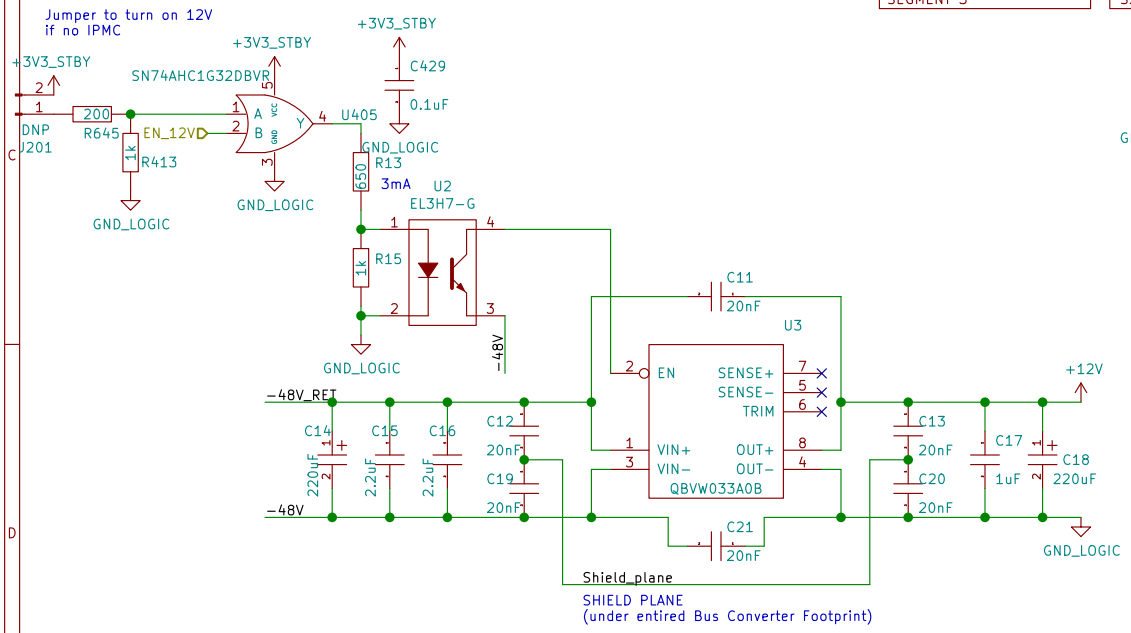
Zone 1 Connector

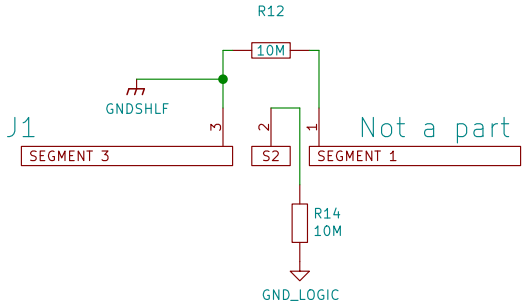


48V power



48V to 12V



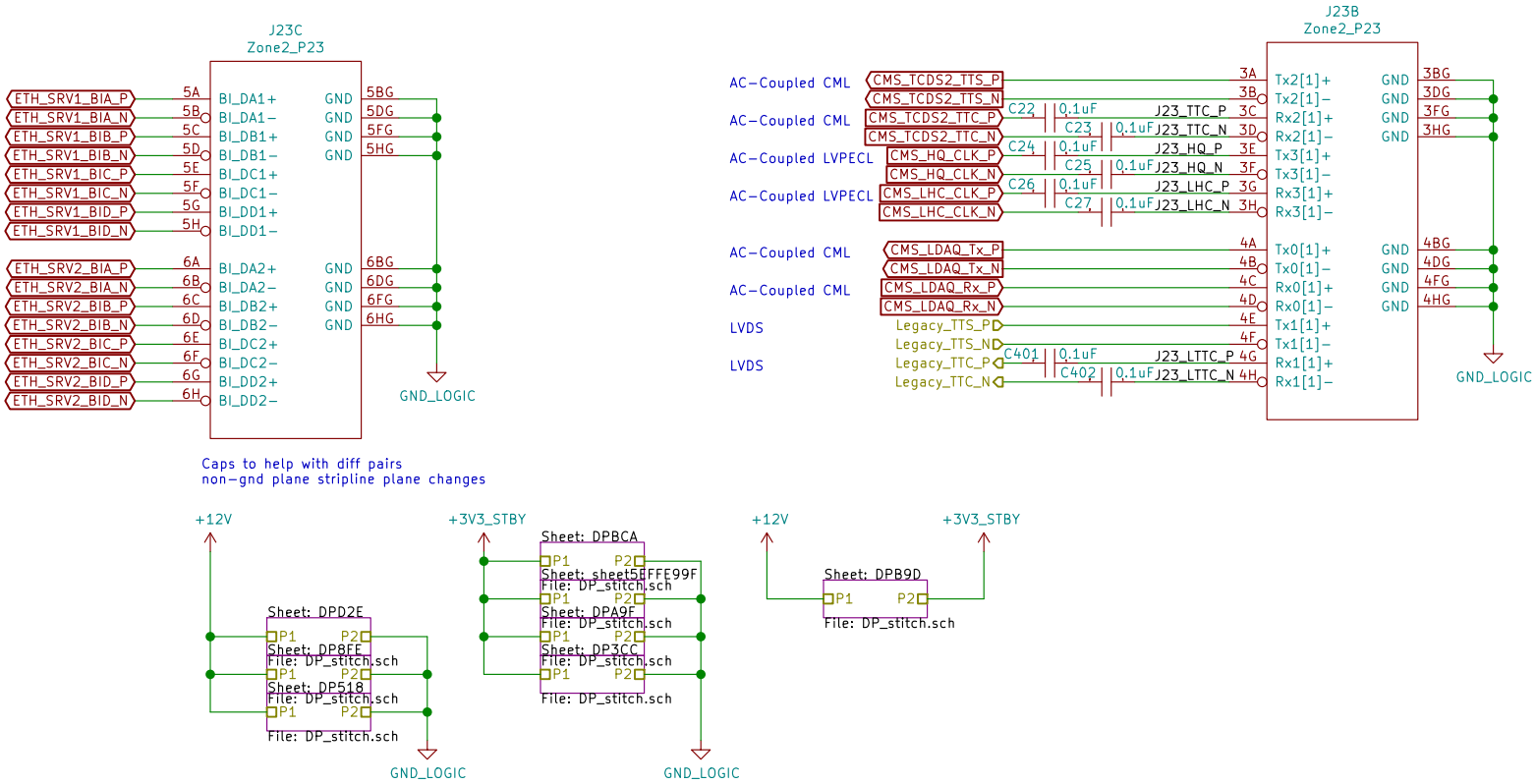


Standby 3.3V

IPMC 3.3 @ ?
Ethernet 3.3 @1.3A +50mA
JTAG 3.3 @ small
UART 3.3 @ small

Sheet: /Zone1 and 48V/	
File: Zone1_PWR.sch	
Title:	
Size: USLetter Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1	Id: 2/51

P23
Connector



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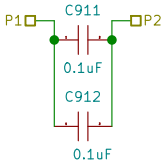
File: Zone2.sch		
Title:		
Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1−1		Id: 3/51



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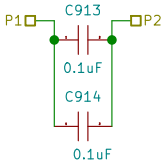
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 4/51



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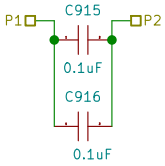

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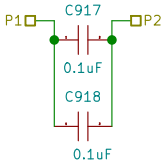

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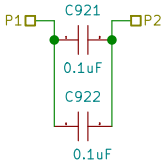

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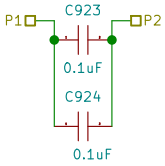

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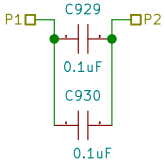
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 9/51



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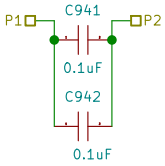

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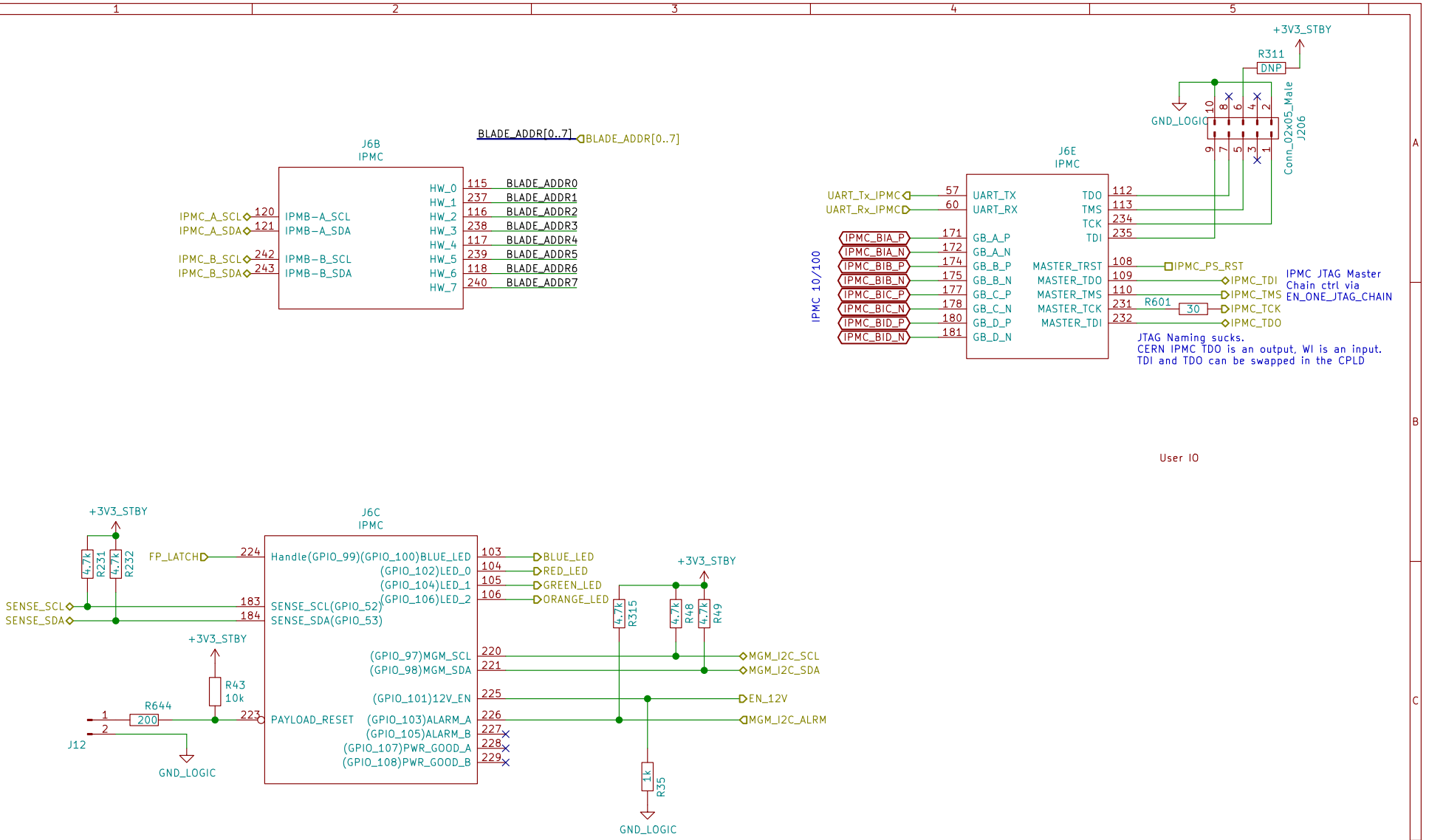
J6B
IPMC
BLADE_ADDR[0..7]
BLADE_ADDR[0..7]
IPMC_A_SCL
IPMC_A_SDA
IPMC_B_SCL
IPMC_B_SDA
120
121
242
243
IPMB-A_SCL
IPMB-A_SDA
IPMB-B_SCL
IPMB-B_SDA
HW_0
HW_1
HW_2
HW_3
HW_4
HW_5
HW_6
HW_7
115
237
116
238
117
239
118
240
BLADE_ADDR0
BLADE_ADDR1
BLADE_ADDR2
BLADE_ADDR3
BLADE_ADDR4
BLADE_ADDR5
BLADE_ADDR6
BLADE_ADDR7
+3V3_STBY
R311
DNP
GND_LOGIC
Conn_02x05_Male
J206
J6E
IPMC
IPMC 10/100
UART_Tx_IPMC
UART_Rx_IPMC
57
60
UART_TX
UART_RX
IPMC_BIA_P
IPMC_BIA_N
IPMC_BIB_P
IPMC_BIB_N
IPMC_BIC_P
IPMC_BIC_N
IPMC_BID_P
IPMC_BID_N
171
172
174
175
177
178
180
181
GB_A_P
GB_A_N
GB_B_P
GB_B_N
GB_C_P
GB_C_N
GB_D_P
GB_D_N
TDO
TMS
TCK
TDI
MASTER_TRST
MASTER_TDO
MASTER_TMS
MASTER_TCK
MASTER_TDI
112
113
234
235
108
109
110
231
232
IPMC_PS_RST
IPMC_TDI
IPMC_TMS
IPMC_TCK
IPMC_TDO
R601
30
IPMC JTAG Master
Chain ctrl via
EN_ONE_JTAG_CHAIN
JTAG Naming sucks.
CERN IPMC TDO is an output, WI is an input.
TDI and TDO can be swapped in the CPLD
User IO
+3V3_STBY
J6C
IPMC
FP_LATCH
224
Handle(GPIO_99)(GPIO_100)BLUE_LED
(GPIO_102)LED_0
(GPIO_104)LED_1
(GPIO_106)LED_2
103
104
105
106
BLUE_LED
RED_LED
GREEN_LED
ORANGE_LED
R231
R232
4.7k
SENSE_SCL
SENSE_SDA
183
184
SENSE_SCL(GPIO_52)
SENSE_SDA(GPIO_53)
R315
R48
R49
(GPIO_97)MGM_SCL
(GPIO_98)MGM_SDA
220
221
MGM_I2C_SCL
MGM_I2C_SDA
R43
10k
R644
200
J12
1
2
223
PAYLOAD_RESET
(GPIO_101)12V_EN
(GPIO_103)ALARM_A
(GPIO_105)ALARM_B
(GPIO_107)PWR_GOOD_A
(GPIO_108)PWR_GOOD_B
225
226
227
228
229
EN_12V
MGM_I2C_ALRM
R35
1k
GND_LOGIC
Sheet: /IPMC Services/
File: IPMC.sch
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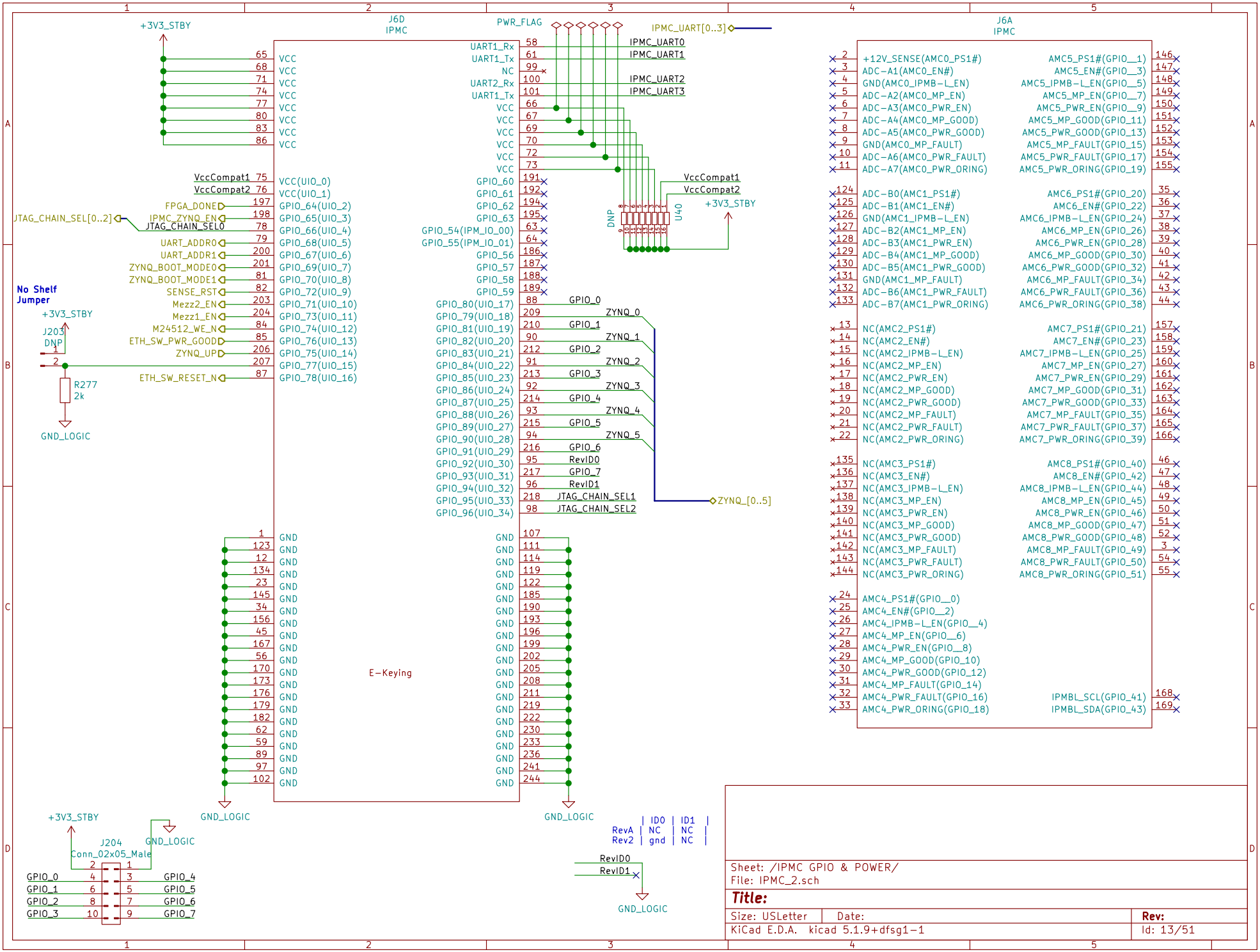
Size: USLetter
Date:
Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1
Id: 12/51

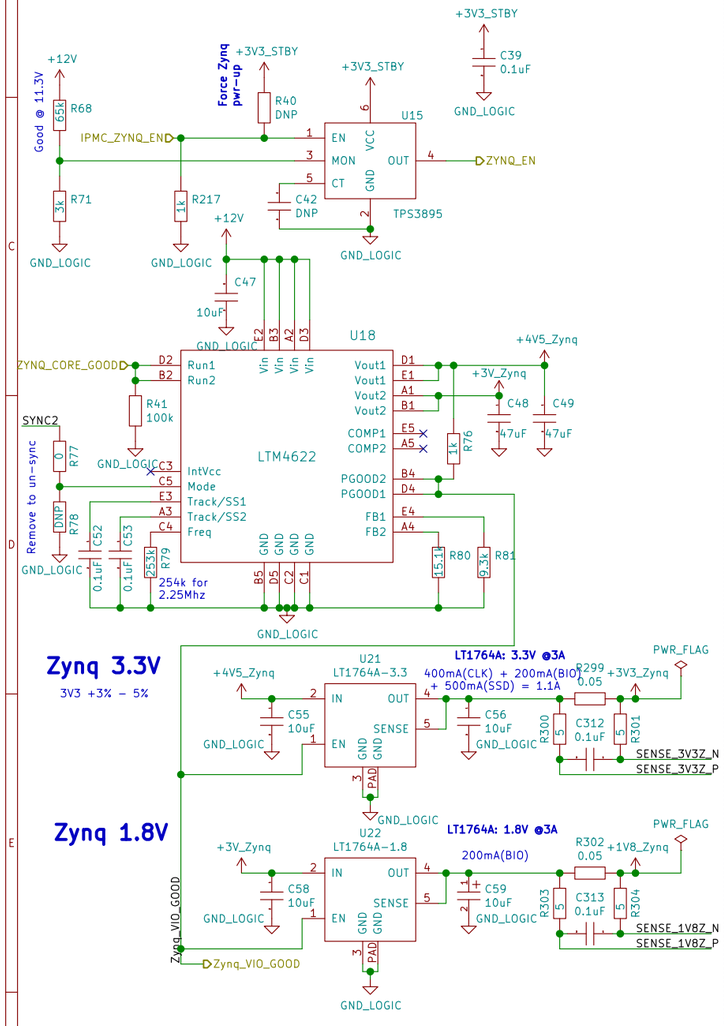

J6D
IPMC
J6A
IPMC
PWR_FLAG
IPMC_UART[0..3]
+3V3_STBY
VCC
VCC(UIO_0)
VCC(UIO_1)
GPIO_64(UIO_2)
GPIO_65(UIO_3)
GPIO_66(UIO_4)
GPIO_68(UIO_5)
GPIO_67(UIO_6)
GPIO_69(UIO_7)
GPIO_70(UIO_8)
GPIO_72(UIO_9)
GPIO_71(UIO_10)
GPIO_73(UIO_11)
GPIO_74(UIO_12)
GPIO_76(UIO_13)
GPIO_75(UIO_14)
GPIO_77(UIO_15)
GPIO_78(UIO_16)
VccCompat1
VccCompat2
FPGA_DONE
IPMC_ZYNQ_EN
JTAG_CHAIN_SEL0
JTAG_CHAIN_SEL[0..2]
UART_ADDR0
UART_ADDR1
ZYNQ_BOOT_MODE0
ZYNQ_BOOT_MODE1
SENSE_RST
Mezz2_EN
Mezz1_EN
M24512_WE_N
ETH_SW_PWR_GOOD
ZYNQ_UP
ETH_SW_RESET_N
No Shelf
Jumper
J203
DNP
R277
2k
GND_LOGIC
UART1_Rx
UART1_Tx
NC
UART2_Rx
UART1_Tx
IPMC_UART0
IPMC_UART1
IPMC_UART2
IPMC_UART3
GPIO_60
GPIO_61
GPIO_62
GPIO_63
GPIO_54(IPM_IO_00)
GPIO_55(IPM_IO_01)
GPIO_56
GPIO_57
GPIO_58
GPIO_59
GPIO_80(UIO_17)
GPIO_79(UIO_18)
GPIO_81(UIO_19)
GPIO_82(UIO_20)
GPIO_83(UIO_21)
GPIO_84(UIO_22)
GPIO_85(UIO_23)
GPIO_86(UIO_24)
GPIO_87(UIO_25)
GPIO_88(UIO_26)
GPIO_89(UIO_27)
GPIO_90(UIO_28)
GPIO_91(UIO_29)
GPIO_92(UIO_30)
GPIO_93(UIO_31)
GPIO_94(UIO_32)
GPIO_95(UIO_33)
GPIO_96(UIO_34)
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
RevID0
RevID1
JTAG_CHAIN_SEL1
JTAG_CHAIN_SEL2
ZYNQ_0
ZYNQ_1
ZYNQ_2
ZYNQ_3
ZYNQ_4
ZYNQ_5
ZYNQ_[0..5]
DNP
U40
VccCompat1
VccCompat2
+3V3_STBY
E-Keying
GND
GND_LOGIC
+12V_SENSE(AMC0_PS1#)
ADC-A1(AMC0_EN#)
GND(AMC0_IPMB-L_EN)
ADC-A2(AMC0_MP_EN)
ADC-A3(AMC0_PWR_EN)
ADC-A4(AMC0_MP_GOOD)
ADC-A5(AMC0_PWR_GOOD)
GND(AMC0_MP_FAULT)
ADC-A6(AMC0_PWR_FAULT)
ADC-A7(AMC0_PWR_ORING)
ADC-B0(AMC1_PS1#)
ADC-B1(AMC1_EN#)
GND(AMC1_IPMB-L_EN)
ADC-B2(AMC1_MP_EN)
ADC-B3(AMC1_PWR_EN)
ADC-B4(AMC1_MP_GOOD)
ADC-B5(AMC1_PWR_GOOD)
GND(AMC1_MP_FAULT)
ADC-B6(AMC1_PWR_FAULT)
ADC-B7(AMC1_PWR_ORING)
NC(AMC2_PS1#)
NC(AMC2_EN#)
NC(AMC2_IPMB-L_EN)
NC(AMC2_MP_EN)
NC(AMC2_PWR_EN)
NC(AMC2_MP_GOOD)
NC(AMC2_PWR_GOOD)
NC(AMC2_MP_FAULT)
NC(AMC2_PWR_FAULT)
NC(AMC2_PWR_ORING)
NC(AMC3_PS1#)
NC(AMC3_EN#)
NC(AMC3_IPMB-L_EN)
NC(AMC3_MP_EN)
NC(AMC3_PWR_EN)
NC(AMC3_MP_GOOD)
NC(AMC3_PWR_GOOD)
NC(AMC3_MP_FAULT)
NC(AMC3_PWR_FAULT)
NC(AMC3_PWR_ORING)
AMC4_PS1#(GPIO__0)
AMC4_EN#(GPIO__2)
AMC4_IPMB-L_EN(GPIO__4)
AMC4_MP_EN(GPIO__6)
AMC4_PWR_EN(GPIO__8)
AMC4_MP_GOOD(GPIO_10)
AMC4_PWR_GOOD(GPIO_12)
AMC4_MP_FAULT(GPIO_14)
AMC4_PWR_FAULT(GPIO_16)
AMC4_PWR_ORING(GPIO_18)
AMC5_PS1#(GPIO__1)
AMC5_EN#(GPIO__3)
AMC5_IPMB-L_EN(GPIO__5)
AMC5_MP_EN(GPIO__7)
AMC5_PWR_EN(GPIO__9)
AMC5_MP_GOOD(GPIO_11)
AMC5_PWR_GOOD(GPIO_13)
AMC5_MP_FAULT(GPIO_15)
AMC5_PWR_FAULT(GPIO_17)
AMC5_PWR_ORING(GPIO_19)
AMC6_PS1#(GPIO_20)
AMC6_EN#(GPIO_22)
AMC6_IPMB-L_EN(GPIO_24)
AMC6_MP_EN(GPIO_26)
AMC6_PWR_EN(GPIO_28)
AMC6_MP_GOOD(GPIO_30)
AMC6_PWR_GOOD(GPIO_32)
AMC6_MP_FAULT(GPIO_34)
AMC6_PWR_FAULT(GPIO_36)
AMC6_PWR_ORING(GPIO_38)
AMC7_PS1#(GPIO_21)
AMC7_EN#(GPIO_23)
AMC7_IPMB-L_EN(GPIO_25)
AMC7_MP_EN(GPIO_27)
AMC7_PWR_EN(GPIO_29)
AMC7_MP_GOOD(GPIO_31)
AMC7_PWR_GOOD(GPIO_33)
AMC7_MP_FAULT(GPIO_35)
AMC7_PWR_FAULT(GPIO_37)
AMC7_PWR_ORING(GPIO_39)
AMC8_PS1#(GPIO_40)
AMC8_EN#(GPIO_42)
AMC8_IPMB-L_EN(GPIO_44)
AMC8_MP_EN(GPIO_45)
AMC8_PWR_EN(GPIO_46)
AMC8_MP_GOOD(GPIO_47)
AMC8_PWR_GOOD(GPIO_48)
AMC8_MP_FAULT(GPIO_49)
AMC8_PWR_FAULT(GPIO_50)
AMC8_PWR_ORING(GPIO_51)
IPMBL_SCL(GPIO_41)
IPMBL_SDA(GPIO_43)
J204
Conn_02x05_Male
| | ID0 | ID1 |
RevA | NC | NC |
Rev2 | gnd | NC |
Sheet: /IPMC GPIO & POWER/
File: IPMC_2.sch
Title:
Size: USLetter
Date:
Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1
Id: 13/51

Power-up Sequence

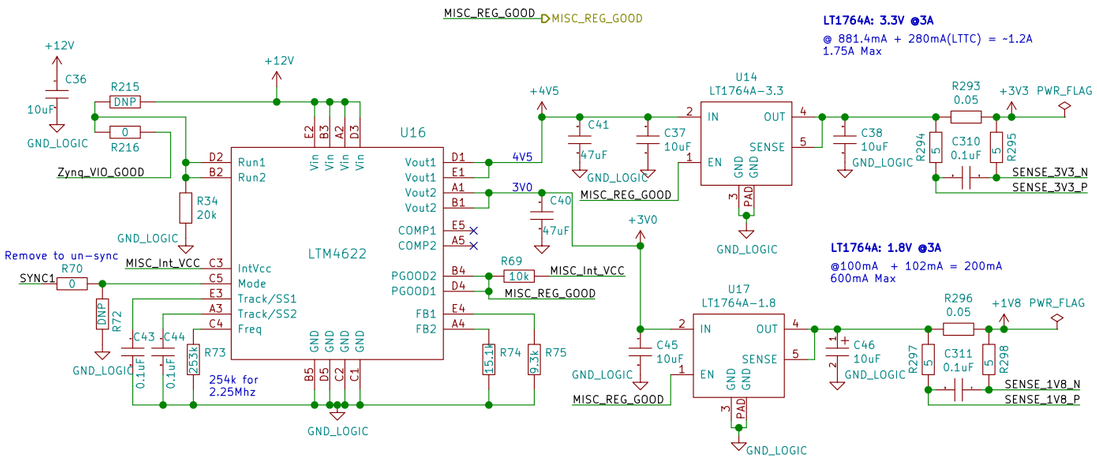
IPMC power-up on 3V3 STBY
|
|-> IPMC turn on 12V.
IPMC tells Zynq to power up.
|
|-> When 12V > 11.3V, U15 turns on Zynq Core
|
|-> When Zynq core voltages are good
ZYNQ_CORE_GOOD enables U18
|
|-> When U18's outputs are good
U21(3V3_Zynq) and U22(1V8_Zynq) are endabled
U16 is enabled
|
|-> When U16's outputs are good
U14(3V3) and U17(1V8) are endabled
|
|-> DONE

Supply	I_nom	dV
3V3_STBY	1A	50mV
3V3	1A	50mV
1V8	0.6A	30mV
3V3_Zynq	0.75A	35mV
1V8_Zynq	0.2A	10mV

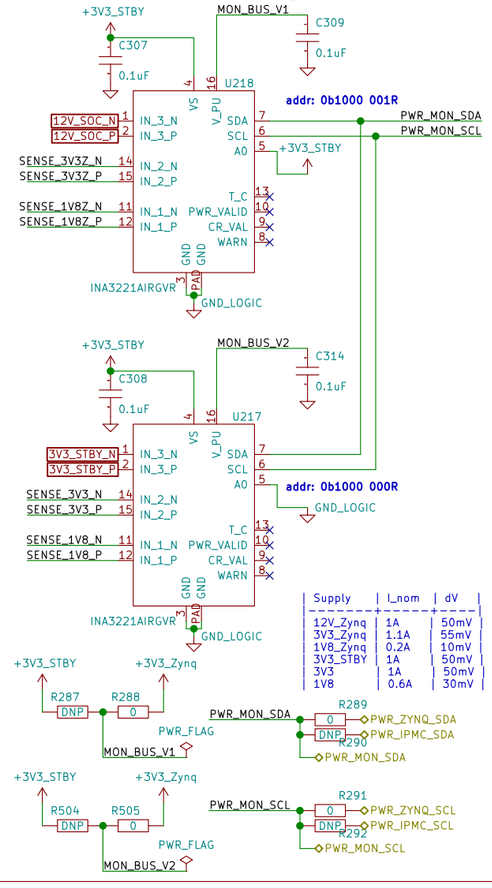
Zynq 3.3V & 1.8V



Misc Board 3.3V & 1.8V

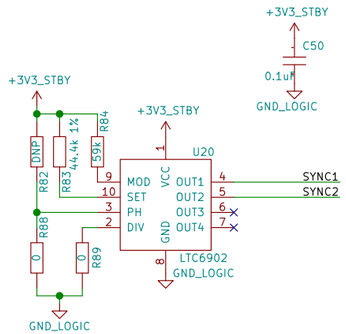


V-I Monitoring



Supply	I_nom	dV
12V_Zynq	1A	50mV
3V3_Zynq	1.1A	55mV
1V8_Zynq	0.2A	10mV
3V3_STBY	1A	50mV
3V3	1A	50mV
1V8	0.6A	30mV

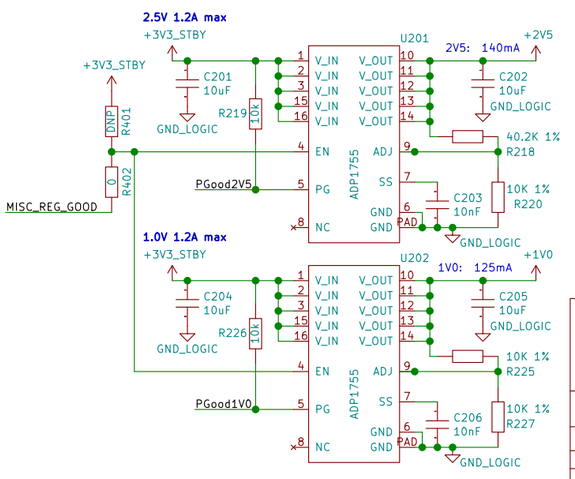
DC-DC Sync



The LTC6902 syncs the LT4622 freqs.
It's freq must be 30% of the LT4622s.
Set to 2.25Mhz with 10% SSP.
If there are problems, disconnet
syncs from LT4622s.

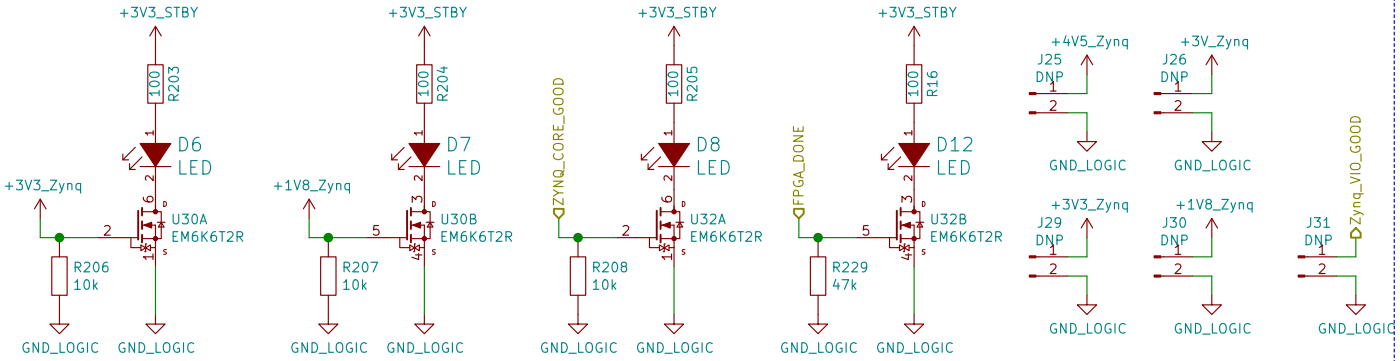
STBY 2.5V &1.0V

Power up using
MISC_REG_GOOD or
3V3_STBY

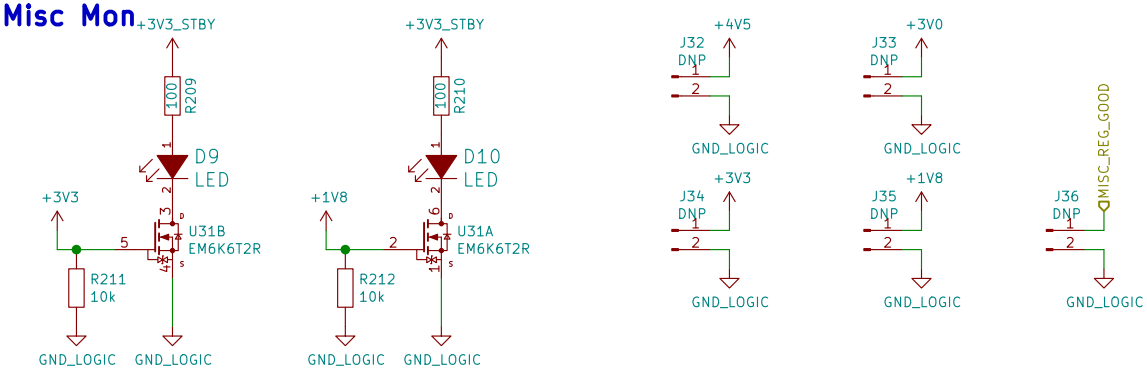


Sheet: /local power/
File: local_power.sch
Title:
Size: B | Date: | **Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1 | Id: 14/51

Zynq Mon



Misc Mon



Blade Mon

Sheet: /Power_indicator/		
File: PWR_INDC.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 15/51

ETH_SW_RESET_N

ETH_SW_RESET_N

+3V3_STBY

R236
5.76K 1%

R243
2.49K 1%

GND_LOGIC

Autoneg_Disable

+3V3_STBY

SGMII Enabled
Mirroring disabled (?)

R237
10K 1%

R244
2.49K 1%

GND_LOGIC

SGMII_EN_MIRROR_EN

Taken from UW ESM Eval board

R238
0

ETH_SW_RESET_N

SGMII_EN_MIRROR_EN

330 R240 LED_0
330 R245 LED_1
330 R246 LED_2

D201 D202 D203

GND_LOGIC

R247
11K 1%

GND_LOGIC

U203C
DP83867CSRGZT

16	MDC	JTAG_CLK	20
17	MDIO	JTAG_TDO	21
		JTAG_TMS	22
18	CLK_OUT	JTAG_TDI	23
43	RESET	INT/PWDN	44
47	LED_0	GPIO_0	39
46	LED_1	GPIO_1	40
45	LED_2		
		XO	14
12	RBias	XI	15

100 R228
2K R233
2K R234
2K R235
2K R239

GND_LOGIC
+3V3_STBY

C207 27pF
X201
C208 27pF

GND_LOGIC

U203A
DP83867CSRGZT

SGMII1_TX_N	28	TX_D0/SGMII_SER_IN_N	TD_P_A 1 A_P
SGMII1_TX_P	27	TX_D1/SGMII_SER_IN_P	TD_M_A 2 A_N
	26	TX_D2	
	25	TX_D3	TD_P_B 4 B_P
	37	TX_CTRL	TD_M_B 5 B_N
	29	GTX_CLK	
PHY_ADDR = 0b00	33		TD_P_C 7 C_P
	34	RX_D0/SGMII_CLK_OUT_P	TD_M_C 8 C_N
SGMII1_RX_P	35	RX_D1/SGMII_CLK_OUT_N	TD_P_D 10 D_P
SGMII1_RX_N	36	RX_D2/SGMII_SER_OUT_P	TD_M_D 11 D_N
Autoneg_Disable	38	RX_D3/SGMII_SER_OUT_N	
	32	RX_CTRL	
		RX_CLK	

0.1uF C217 SGMII1_TX_N
SGMII1_TX_P C218 SGMII_TX_P
0.1uF

0.1uF C227 SGMII_RX_P
SGMII1_RX_P
SGMII1_RX_N C228 SGMII_RX_N
0.1uF

U203B
DP83867CSRGZT

19	VDD_IO	VDD_1V0	6
30	VDD_IO	VDD_1V0	24
41	VDD_IO	VDD_1V0	31
		VDD_1V0	42
3	VDD_A_2V5	VDD_A_1V8	13
9	VDD_A_2V5	VDD_A_1V8	48
	GND		
	PAD		

+3V3_STBY
+2V5
+1V0

3V3_STBY : 50mA
2V5 : 140mA
1V0 : 125mA

GND_LOGIC

+3V3_STBY

C209 10uF C210 10nF C211 1uF C212 0.1uF C213 1uF C214 0.1uF C215 1uF C216 0.1uF

GND_LOGIC

+1V0

C217 1uF C220 0.1uF C221 1uF C222 0.1uF C223 1uF C224 0.1uF C225 1uF C226 0.1uF

GND_LOGIC

+2V5 +1V0

C229 10uF C230 10nF C231 1uF C232 0.1uF C233 1uF C234 0.1uF C235 10uF C236 10nF

GND_LOGIC GND_LOGIC

J5

+3V3_STBY

3.3V @ 0.85A to 1.3A

VCC

ESM

14	EN		
12	GOOD	ETH_SW_PWR_GOOD	
19	RESET	ETH_SW_RESET_N	
11	STRP0	+3V3_STBY	
13	STRP1		
17	RST		FLASH
15	CLK		
18	CS		
16	DO		
20	DI		
28	TX	SWITCH_UART_Tx	UART
30	RX	SWITCH_UART_Rx	
27	SCK	SWITCH_LED_SCK	LED
29	SDO	SWITCH_LED_SDA	
24	NC		
26	NC		

R249 DNP
GND_LOGIC

R30 DNP
R31 4.7k
R328 DNP
R329 4.7k
GND_LOGIC

SGMII1

TX_P	36	SGMII1_TX_P
TX_N	34	SGMII1_TX_N
RX_P	42	SGMII1_RX_P
RX_N	40	SGMII1_RX_N

SGMII0

TX_P	35	
TX_N	33	
RX_P	41	
RX_N	39	

P3 IPMC 10/100

X0_P	46	IPMC_BIA_P
X0_N	48	IPMC_BIA_N
X1_P	50	IPMC_BIB_P
X1_N	52	IPMC_BIB_N
X2_P	54	IPMC_BIC_P
X2_N	56	IPMC_BIC_N
X3_P	58	IPMC_BID_P
X3_N	60	IPMC_BID_N

P2 ATCA SERV B

X0_P	45	ETH_SRV2_BIA_P
X0_N	47	ETH_SRV2_BIA_N
X1_P	49	ETH_SRV2_BIB_P
X1_N	51	ETH_SRV2_BIB_N
X2_P	53	ETH_SRV2_BIC_P
X2_N	55	ETH_SRV2_BIC_N
X3_P	57	ETH_SRV2_BID_P
X3_N	59	ETH_SRV2_BID_N

P1 ATCA SERV A

X0_P	64	ETH_SRV1_BIA_P
X0_N	66	ETH_SRV1_BIA_N
X1_P	68	ETH_SRV1_BIB_P
X1_N	70	ETH_SRV1_BIB_N
X2_P	72	ETH_SRV1_BIC_P
X2_N	74	ETH_SRV1_BIC_N
X3_P	76	ETH_SRV1_BID_P
X3_N	78	ETH_SRV1_BID_N

P0 Front Panel

X0_P	63	ETH_FP_A_P
X0_N	65	ETH_FP_A_N
X1_P	67	ETH_FP_B_P
X1_N	69	ETH_FP_B_N
X2_P	71	ETH_FP_C_P
X2_N	73	ETH_FP_C_N
X3_P	75	ETH_FP_D_P
X3_N	77	ETH_FP_D_N

GND

7 8 9 10 21 22 23 25 31 32 37 38 43 44 61 62 79 80

GND_LOGIC

+12V

Sheet: DPF55
P1 P2
Sheet: DPDC8
File: DP_stitch.sch
P1 P2
File: DP_stitch.sch

GND_LOGIC

Caps for stripline plane cuts

+3V3_STBY

Sheet: DPD2A
P1 P2
Sheet: DPD8B
File: DP_stitch.sch
P1 P2
File: DP_stitch.sch

GND_LOGIC

Caps for stripline plane cuts

A,B,C,D can be direct since this phy has Auto-MDIX

U204
H5084FNLT

0.1uF 25V C237
0.1uF 25V C238
0.1uF 25V C239
0.1uF 25V C240

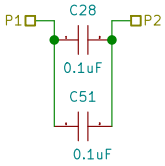
	1	D_N	24 ETH1_CT4
	2		23 ETH1_D_N
	3	D_P	22 ETH1_D_P
	4		21 ETH1_CT3
	5	C_N	20 ETH1_C_N
	6	C_P	19 ETH1_C_P
	7		18 ETH1_CT2
	8	B_N	17 ETH1_B_N
	9	B_P	16 ETH1_B_P
	10		15 ETH1_CT1
	11	A_N	14 ETH1_A_N
	12	A_P	13 ETH1_A_P

GND_LOGIC

Sheet: /Ethernet switch/
File: eth_switch.sch

Title:

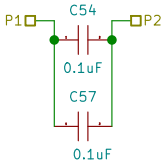
Size: B	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 16/51



Sheet: /Ethernet switch/DPD2A/
File: DP_stitch.sch

Title:

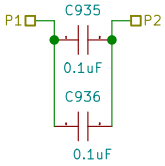
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 17/51



Sheet: /Ethernet switch/DP78B/
File: DP_stitch.sch

Title:

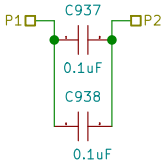
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 18/51



Sheet: /Ethernet switch/DPF55/
File: DP_stitch.sch

Title:

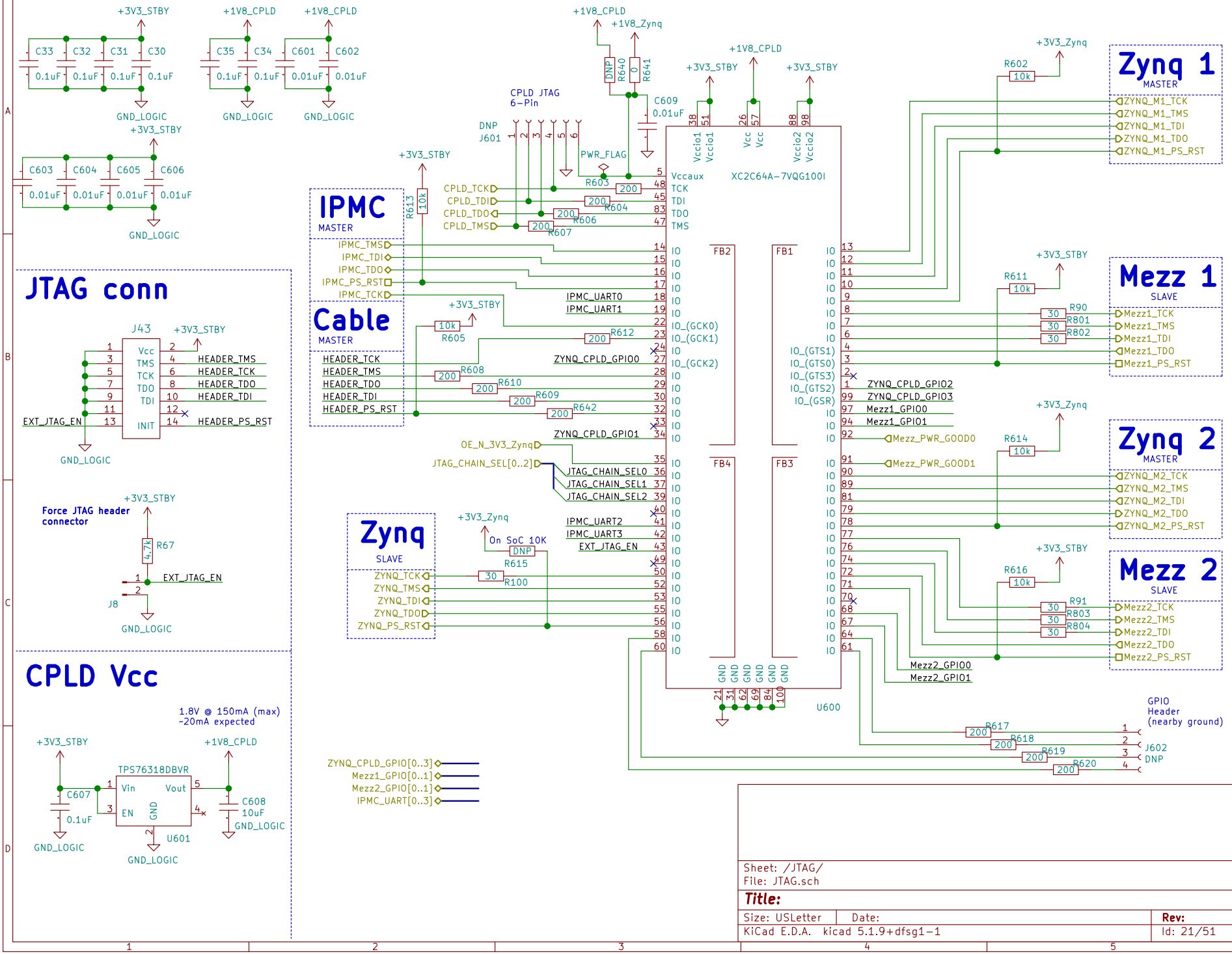
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 19/51



Sheet: /Ethernet switch/DPDC8/
File: DP_stitch.sch

Title:

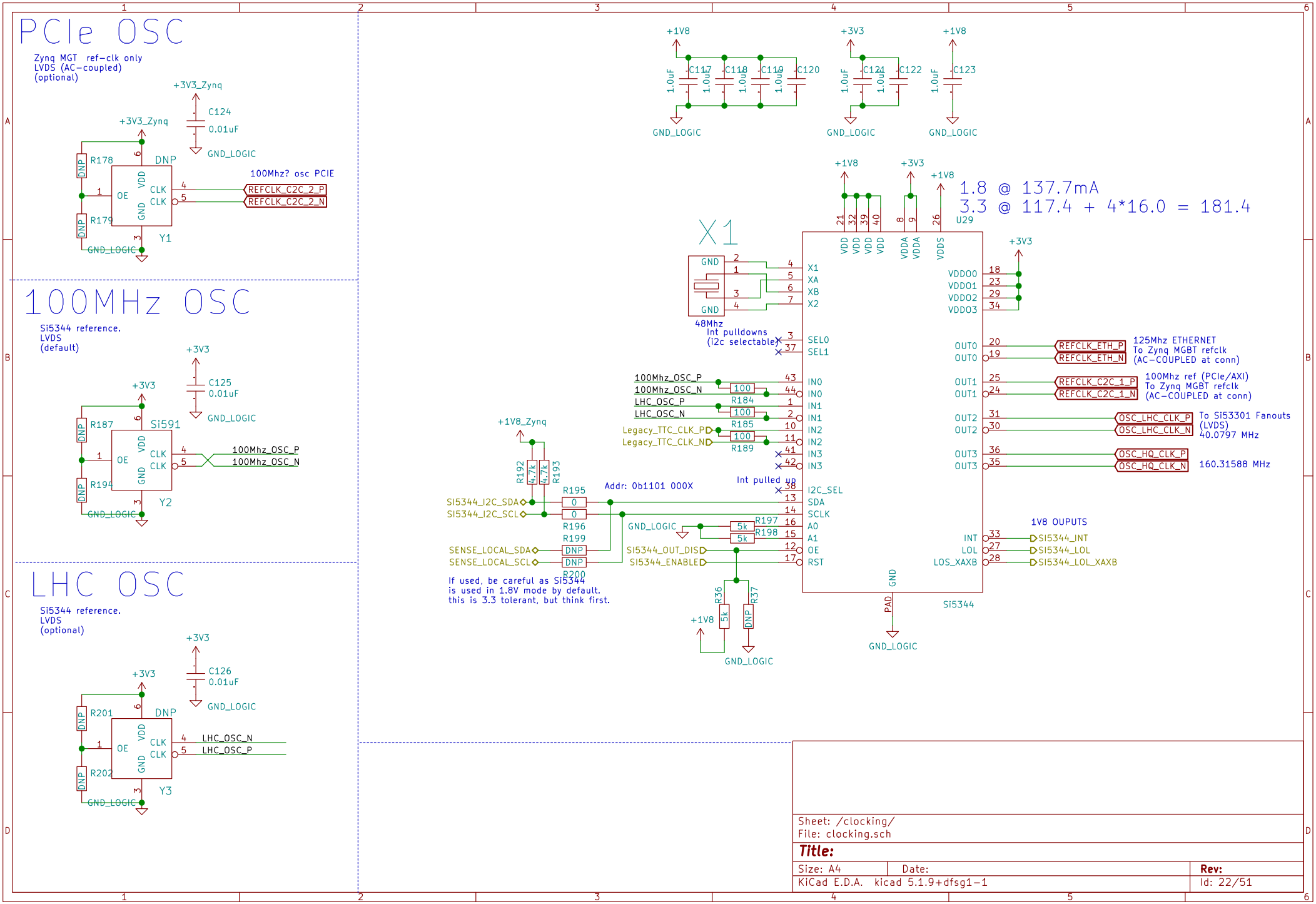
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 20/51

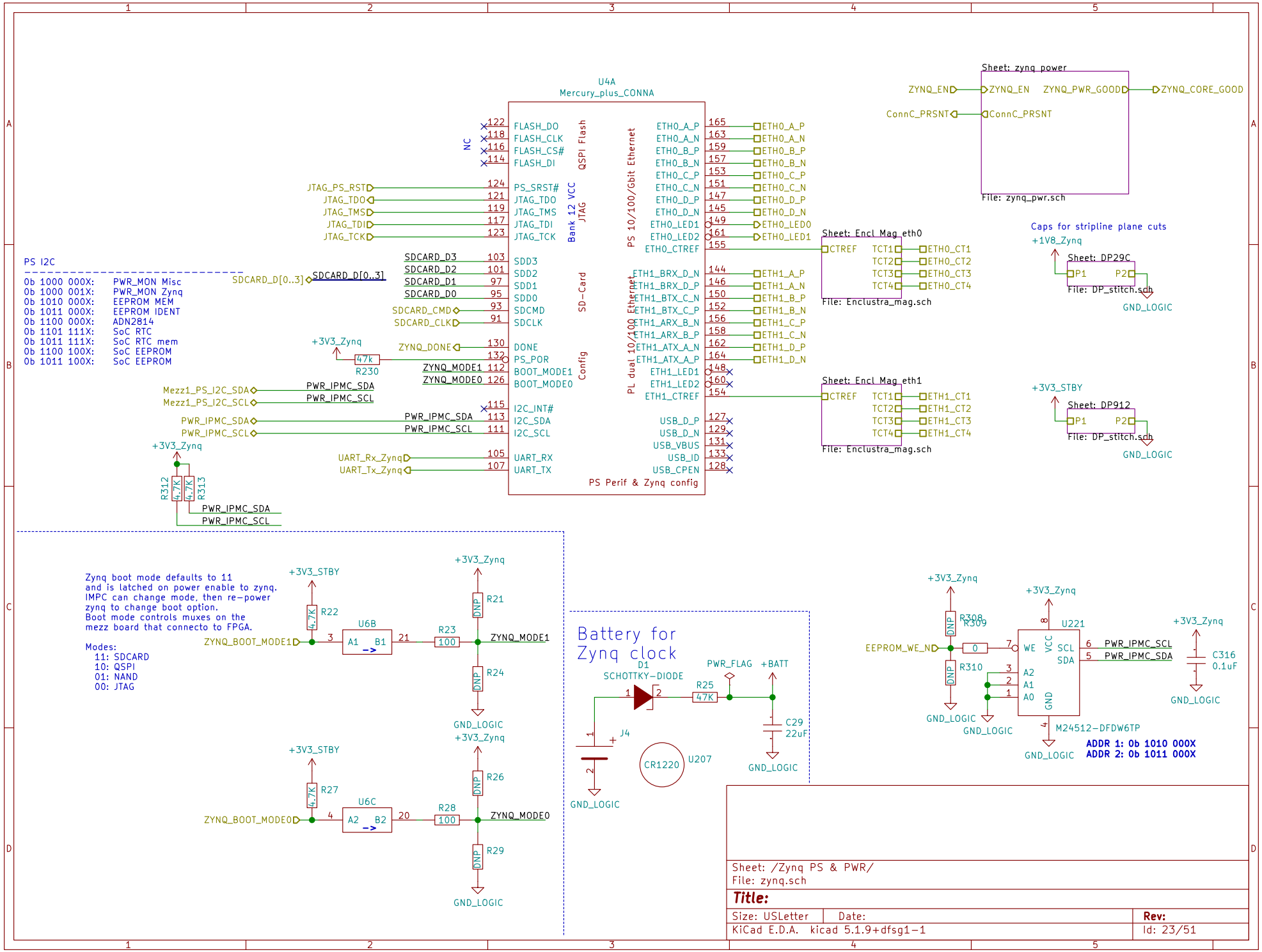


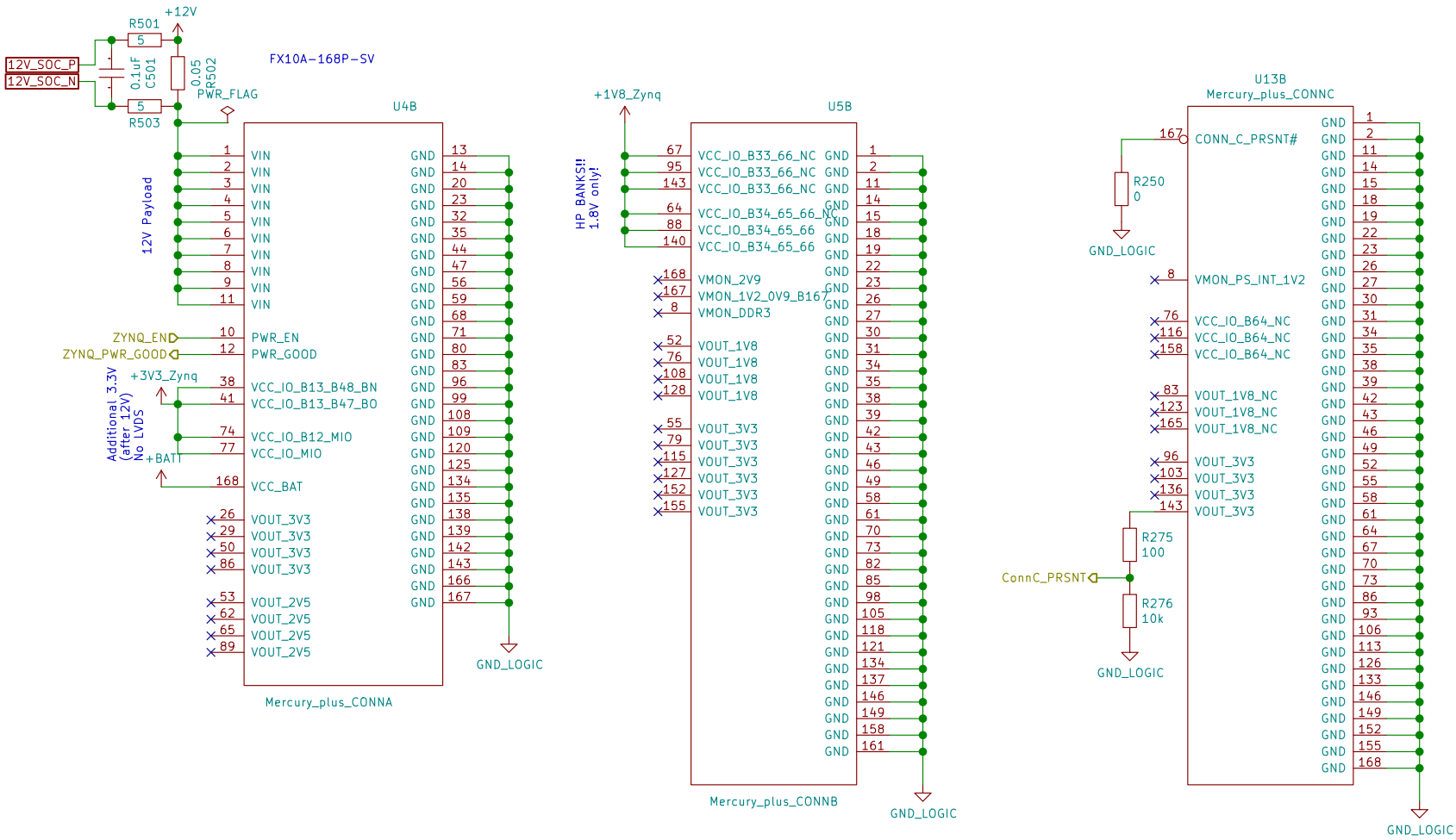
Sheet: /JTAG/
File: JTAG.sch

Title:

Size: USLetter	Date:	Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 21/51


PCIe OSC
Zynq MGT ref-clk only
LVDS (AC-coupled)
(optional)
+3V3_Zynq
C124
0.01uF
GND_LOGIC
R178
DNP
R179
OE
VDD
GND
CLK
100Mhz? osc PCIE
REFCLK_C2C_2_P
REFCLK_C2C_2_N
Y1
100MHz OSC
Si5344 reference.
LVDS
(default)
+3V3
C125
0.01uF
R187
R194
Si591
100Mhz_OSC_P
100Mhz_OSC_N
Y2
LHC OSC
Si5344 reference.
LVDS
(optional)
C126
0.01uF
R201
R202
LHC_OSC_N
LHC_OSC_P
Y3
+1V8
C117
C118
C119
C120
C121
C122
C123
1.0uF
1.8 @ 137.7mA
3.3 @ 117.4 + 4*16.0 = 181.4
U29
X1
48Mhz
Int pulldowns
(i2c selectable)
SEL0
SEL1
100Mhz_OSC_P
100Mhz_OSC_N
LHC_OSC_P
LHC_OSC_N
Legacy_TTC_CLK_P
Legacy_TTC_CLK_N
R184
R185
R189
100
IN0
IN1
IN2
IN3
+1V8_Zynq
R192
R193
4.7k
Addr: 0b1101 000X
Int pulled up
I2C_SEL
SI5344_I2C_SDA
SI5344_I2C_SCL
SDA
SCLK
R195
R196
R197
R198
5k
A0
A1
SENSE_LOCAL_SDA
SENSE_LOCAL_SCL
R199
R200
SI5344_OUT_DIS
SI5344_ENABLE
OE
RST
If used, be careful as Si5344
is used in 1.8V mode by default.
this is 3.3 tolerant, but think first.
R36
R37
PAD
Si5344
VDDO0
VDDO1
VDDO2
VDDO3
OUT0
OUT1
OUT2
OUT3
REFCLK_ETH_P
REFCLK_ETH_N
125Mhz ETHERNET
To Zynq MGBT refclk
(AC-COUPLED at conn)
REFCLK_C2C_1_P
REFCLK_C2C_1_N
100Mhz ref (PCIe/AXI)
To Zynq MGBT refclk
(AC-COUPLED at conn)
OSC_LHC_CLK_P
OSC_LHC_CLK_N
To Si53301 Fanouts
(LVDS)
40.0797 MHz
OSC_HQ_CLK_P
OSC_HQ_CLK_N
160.31588 MHz
1V8 OUPUTS
INT
LOL
LOS_XAXB
SI5344_INT
SI5344_LOL
SI5344_LOL_XAXB
Sheet: /clocking/
File: clocking.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1
Id: 22/51

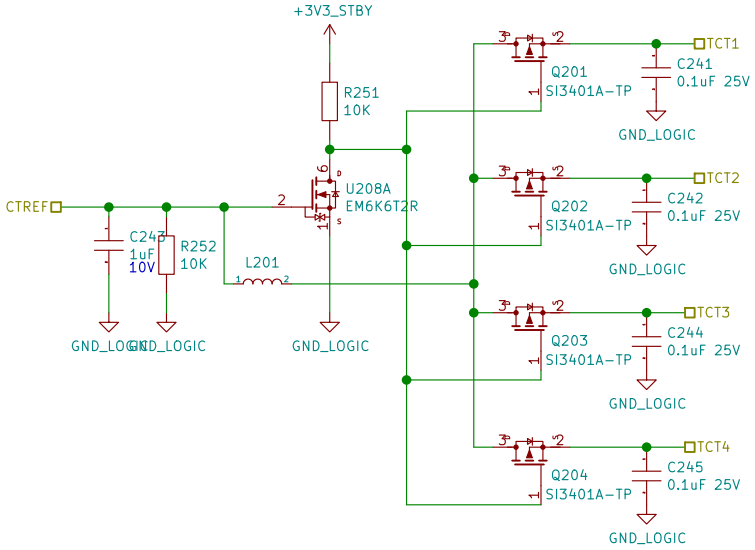

U4A
Mercury_plus_CONNA
PS I2C
0b 1000 000X: PWR_MON Misc
0b 1000 001X: PWR_MON Zynq
0b 1010 000X: EEPROM MEM
0b 1011 000X: EEPROM IDENT
0b 1100 000X: ADN2814
0b 1101 111X: SoC RTC
0b 1011 111X: SoC RTC mem
0b 1100 100X: SoC EEPROM
0b 1011 100X: SoC EEPROM
NC
QSPI Flash
JTAG
Bank 12 VCC
SD-Card
Config
PS 10/100/Gbit Ethernet
PL dual 10/100 Ethernet
PS Perif & Zynq config
FLASH_DO
FLASH_CLK
FLASH_CS#
FLASH_DI
PS_SRST#
JTAG_TDO
JTAG_TMS
JTAG_TDI
JTAG_TCK
SDD3
SDD2
SDD1
SDD0
SDCMD
SDCLK
DONE
PS_POR
BOOT_MODE1
BOOT_MODE0
I2C_INT#
I2C_SDA
I2C_SCL
UART_RX
UART_TX
ETH0_A_P
ETH0_A_N
ETH0_B_P
ETH0_B_N
ETH0_C_P
ETH0_C_N
ETH0_D_P
ETH0_D_N
ETH0_LED1
ETH0_LED2
ETH0_CTREF
ETH1_BRX_D_N
ETH1_BRX_D_P
ETH1_BTX_C_N
ETH1_BTX_C_P
ETH1_ARX_B_N
ETH1_ARX_B_P
ETH1_ATX_A_N
ETH1_ATX_A_P
ETH1_LED1
ETH1_LED2
ETH1_CTREF
USB_D_P
USB_D_N
USB_VBUS
USB_ID
USB_CPEN
JTAG_PS_RST
JTAG_TDO
JTAG_TMS
JTAG_TDI
JTAG_TCK
SDCARD_D3
SDCARD_D2
SDCARD_D1
SDCARD_D0
SDCARD_CMD
SDCARD_CLK
SDCARD_D[0..3]
SDCARD_D[0..3]
+3V3_Zynq
ZYNQ_DONE
47k
R230
ZYNQ_MODE1
ZYNQ_MODE0
Mezz1_PS_I2C_SDA
Mezz1_PS_I2C_SCL
PWR_IPMC_SDA
PWR_IPMC_SCL
UART_Rx_Zynq
UART_Tx_Zynq
R312
R313
4.7K
Sheet: zynq power
ZYNQ_EN
ZYNQ_PWR_GOOD
ZYNQ_CORE_GOOD
ConnC_PRSNT
File: zynq_pwr.sch
Sheet: Encl Mag eth0
CTREF
TCT1
TCT2
TCT3
TCT4
ETH0_CT1
ETH0_CT2
ETH0_CT3
ETH0_CT4
File: Enclustra_mag.sch
Sheet: Encl Mag eth1
ETH1_CT1
ETH1_CT2
ETH1_CT3
ETH1_CT4
Caps for stripline plane cuts
+1V8_Zynq
Sheet: DP29C
P1
P2
File: DP_stitch.sch
GND_LOGIC
+3V3_STBY
Sheet: DP912
Zynq boot mode defaults to 11
and is latched on power enable to zynq.
IMPC can change mode, then re-power
zynq to change boot option.
Boot mode controls muxes on the
mezz board that connecto to FPGA.
Modes:
11: SDCARD
10: QSPI
01: NAND
00: JTAG
+3V3_STBY
R22
U6B
ZYNQ_BOOT_MODE1
A1
B1
R23
100
R21
R24
DNP
GND_LOGIC
R27
U6C
ZYNQ_BOOT_MODE0
A2
B2
R28
R26
R29
Battery for
Zynq clock
D1
SCHOTTKY-DIODE
PWR_FLAG
+BATT
R25
47K
C29
22uF
J4
CR1220
U207
R308
R309
R310
EEPROM_WE_N
U221
WE
VCC
SCL
SDA
A2
A1
A0
GND
M24512-DFDW6TP
C316
0.1uF
ADDR 1: 0b 1010 000X
ADDR 2: 0b 1011 000X
Sheet: /Zynq PS & PWR/
File: zynq.sch
Title:
Size: USLetter
Date:
Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1
Id: 23/51



Sheet: /Zynq PS & PWR/zynq power/
File: zynq_pwr.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 24/51



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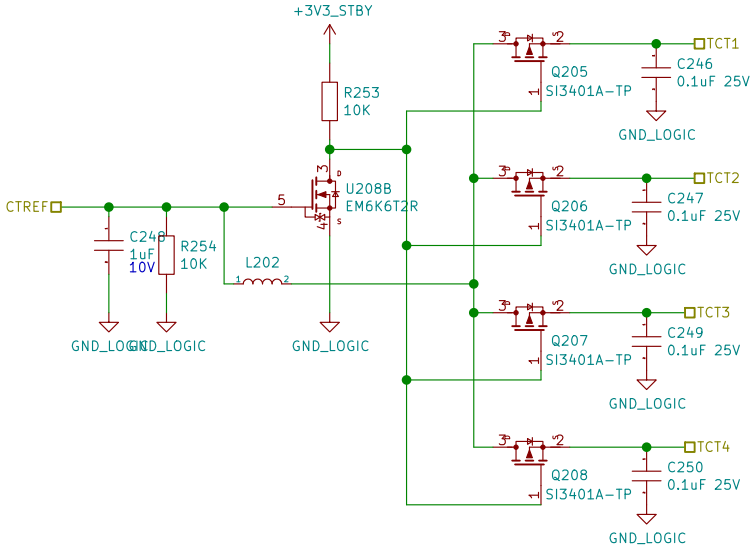
File: Enclustra_mag.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 25/51



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File: Enclustra_mag.sch

Title:

Size: A4	Date:	**Rev:**
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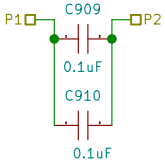
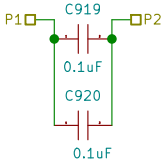


Sheet: /Zynq PS & PWR/DP29C/
File: DP_stitch.sch

Title:

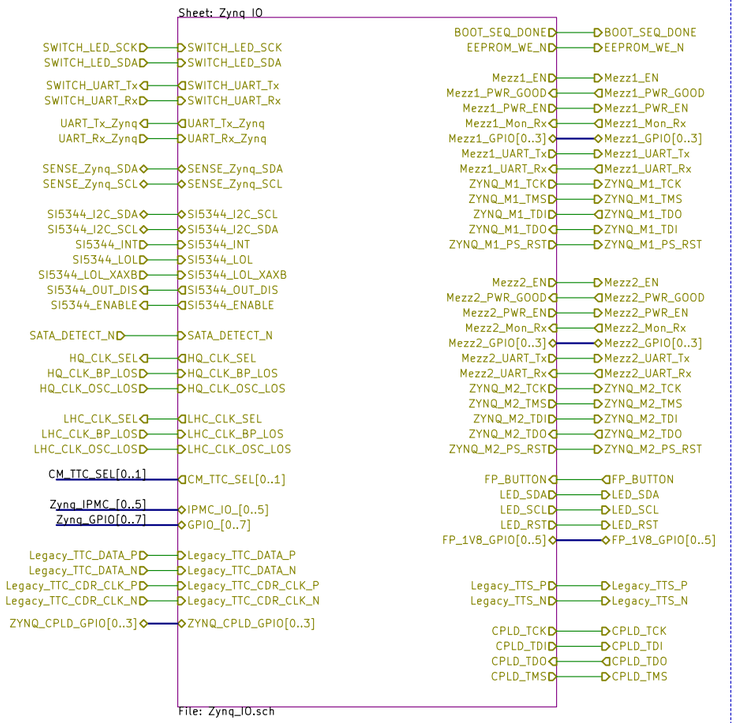
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 27/51

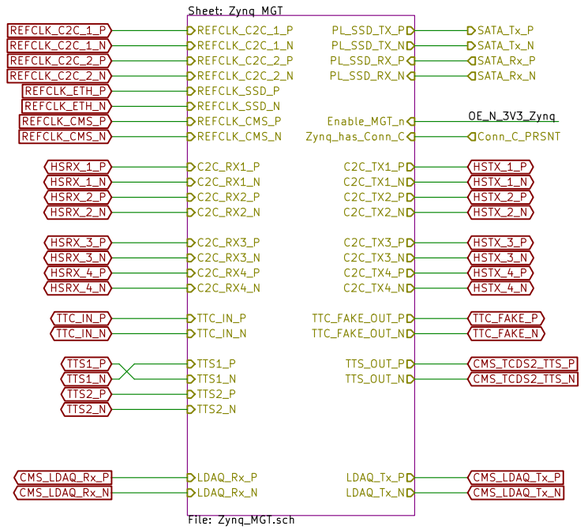


Sheet: /Zynq PS & PWR/DP912/
File: DP_stitch.sch

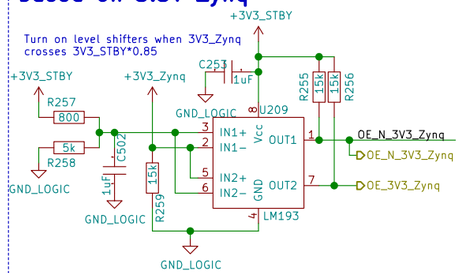
Title:

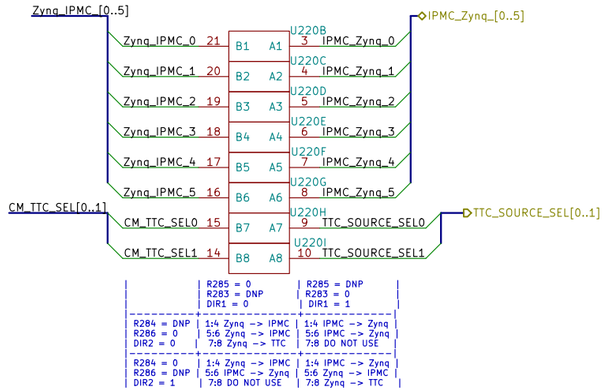
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 28/51



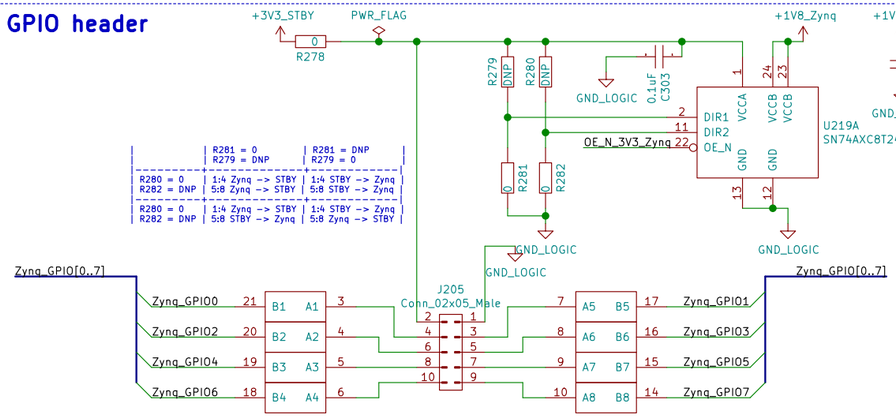


OE For Level-shifters based on 3.3V Zynq

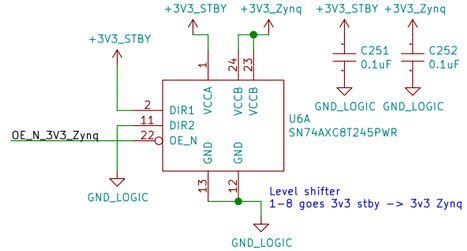




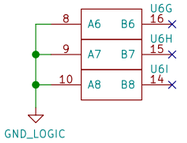
Zynq GPIO header



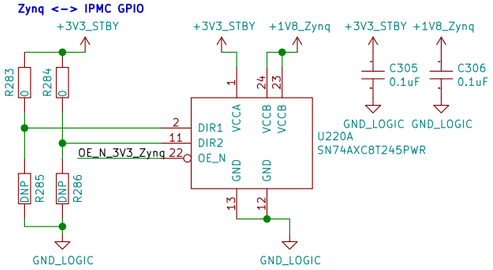
Level shifters for Zynq IOs



Un-used level shifters



Zynq <-> IPMC GPIO



Sheet: /Zynq GPIO & MGT/	
File: zynq2.sch	
Title:	
Size: B	Date:
KiCad E.D.A. kicad 5.1.9+dfsg1-1	**Rev:** Id: 29/51

Mezz1_GPIO[0..3]
Mezz2_GPIO[0..3]

U4C
Mercury_plus_CONNA

Mezz1_GPIO1	16	IO_CLK_SRCC_HDGC_P	PL Clk
Mezz1_GPIO2	18	IO_CLK_SRCC_HDGC_N	
EEPROM_WE_N	46	IO_CLK_MRCC_HDGC_P	
ZYNQ_CPLD_GPIO1	48	IO_CLK_MRCC_HDGC_N	
ZYNQ_CPLD_GPIO2	49	IO_CLK_SRCC_HDGC_P	
ZYNQ_CPLD_GPIO3	51	IO_CLK_SRCC_HDGC_N	
Mezz2_GPIO1	85	IO_CLK_MRCC_HDGC_P	
Mezz2_GPIO2	87	IO_CLK_MRCC_HDGC_N	
ZRevID0	98	IO_MIO50_MIO45	MIO
ZRevID1	100	IO_MIO51_MIO44	
ZRevID2	104	IO_MIO48_MIO42	
	106	IO_MIO49_MIO43	
Mezz1_PWR_GOOD	88	IO_L3_Y10_P	BANK 12 / LSMIO
Mezz2_PWR_GOOD	90	IO_L3_AA10_N	
ZYNQ_CPLD_GPIO0	92	IO_L1_Y12_P	
ZYNQ_M2_TDI	94	IO_L1_Y11_N	
Mezz1_UART_Tx	15	IO_P	BANK 13 / 48 / BN(O)
Mezz1_UART_Rx	17	IO_N	
Mezz2_UART_Tx	19	IO_P	
Mezz2_UART_Rx	21	IO_N	
LED_SCL	22	IO_P	
LED_RST	24	IO_N	
LED_SDA	25	IO_P	
SENSE_Zynq_SDA	27	IO_N	
SENSE_Zynq_SCL	28	IO_P	
	30	IO_N	
ZYNQ_M2_PS_RST	31	IO_P	
	33	IO_N	

BANK 13

	34	IO_P	LHC_CLK_SEL
	36	IO_N	LHC_CLK_BP_LOS
	37	IO_P	LHC_CLK_OSC_LOS
	39	IO_N	HQ_CLK_SEL
	40	IO_P	HQ_CLK_BP_LOS
	42	IO_N	HQ_CLK_OSC_LOS
	43	IO_P	Mezz2_EN
	45	IO_N	Mezz1_EN
	52	IO_P	UART_Rx_Zynq
	54	IO_N	UART_Tx_Zynq
	55	IO_P	R417 30 ZYNQ_M1_TCK
	57	IO_N	ZYNQ_M1_TMS
	58	IO_P	ZYNQ_M1_TDO
	60	IO_N	ZYNQ_M1_TDI
	61	IO_P	Mezz1_PWR_EN
	63	IO_N	Mezz1_Mon_Rx
	64	IO_P	Mezz1_GPIO0
	66	IO_N	Mezz2_PWR_EN
	67	IO_P	Mezz2_Mon_Rx
	69	IO_N	Mezz2_GPIO0
	70	IO_P	ZYNQ_M1_PS_RST
	72	IO_N	FP_BUTTON
	73	IO_P	R266 100 BOOT_SEQ_DONE
	75	IO_N	SWITCH_UART_Tx_local
	76	IO_P	SWITCH_UART_Rx_local
	78	IO_N	R418 30 ZYNQ_M2_TCK
	79	IO	ZYNQ_M2_TMS
	81	IO	ZYNQ_M2_TDO
	82	IO_P_MIO40	
	84	IO_N_MIO41	

Alternative for IPMC UART to go to PL

R267 4.6k

GND_LOGIC

3.3V

SWITCH_LED_SCK — 5 — U6D A3 B3 -> — 19
SWITCH_LED_SDA — 6 — U6E A4 B4 -> — 18
SWITCH_UART_Rx — 7 — U6F A5 B5 -> — 17 — SWITCH_UART_Rx_local
SWITCH_UART_Tx — R643 200 — SWITCH_UART_Tx_local

+3V3_STBY

Sheet: DP6C9
P1 P2
File: DP_stitch.sch

GND_LOGIC

U5C
Mercury_plus_CONNB

	130	IO_SRCC_GC_NC_P	CLK_MRCC_GC_NC_P 57
	132	IO_SRCC_GC_NC_N	CLK_MRCC_GC_NC_N 59
ZYNQ_CLK1A_P	154	IO_MRCC_GC_NC_P	CLK_MRCC_GC_NC_P 151 ZYNQ_CLK2A_P
ZYNQ_CLK1A_N	156	IO_MRCC_GC_NC_N	CLK_MRCC_GC_NC_N 153 ZYNQ_CLK2A_N
Legacy_TTC_CDR_CLK_P	78	IO_MRCC_GC_NC_P	CLK_SRCC_GC_NC_P 123
Legacy_TTC_CDR_CLK_N	80	IO_MRCC_GC_NC_N	CLK_SRCC_GC_NC_N 125
	72	IO_B34_65_66_NC_P	
	74	IO_B34_65_66_NC_N	
	84	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 75
SATA_DETECT_N	86	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 77
Legacy_TTC_DATA_P	90	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 81
Legacy_TTC_DATA_N	92	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 83
Legacy_TTS_P	94	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 87
Legacy_TTS_N	96	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 89
CPLD_TCK	100	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 91
CPLD_TDI	102	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 93
CPLD_TDO	104	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 97
CPLD_TMS	106	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 99
GPIO_7	110	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 101
GPIO_5	112	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 103
SI5344_I2C_SDA	114	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 107
SI5344_I2C_SCL	116	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 109
SI5344_INT	120	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 111
SI5344_OUT_DIS	122	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 113
SI5344_ENABLE	124	IO_B34_65_66_NC_P	IO_B33_NC_NC_P 117
SI5344_LOL	126	IO_B34_65_66_NC_N	IO_B33_NC_NC_N 119
SI5344_LOL_XAXB	136	IO_B34_65_66_NC_P	IO_B33_B66_NC_P 129 GPIO_3
	138	IO_B34_65_66_NC_N	IO_B33_B66_NC_N 131 GPIO_1
IPMC_IO_0	142	IO_B34_65_66_NC_P	IO_B33_B66_NC_P 133 GPIO_6
IPMC_IO_1	144	IO_B34_65_66_NC_N	IO_B33_B66_NC_N 135 GPIO_4
IPMC_IO_2	148	IO_B34_65_66_NC_P	IO_B33_B66_NC_P 139 GPIO_2
IPMC_IO_3	150	IO_B34_65_66_NC_N	IO_B33_B66_NC_N 141 GPIO_0
IPMC_IO_4	160	IO_B34_65_66_NC_P	IO_B33_B66_NC_P 145 FP_1V8_GPIO0
IPMC_IO_5	162	IO_B34_65_66_NC_N	IO_B33_B66_NC_N 147 FP_1V8_GPIO1
CM_TTC_SEL0	164	IO_B34_65_66_NC_P	IO_B33_B66_NC_P 157 FP_1V8_GPIO2
CM_TTC_SEL1	166	IO_B34_65_66_NC_N	IO_B33_B66_NC_N 159 FP_1V8_GPIO3
			IO_B33_B66_NC_P 163 FP_1V8_GPIO4
			IO_B33_B66_NC_N 165 FP_1V8_GPIO5

Bank34 Bank33

IPMC_IO_[0..5]
CM_TTC_SEL[0..1]
GPIO_[0..7]
FP_1V8_GPIO[0..5]

1.8V ONLY!!!

PL 1V8 I2C
0b 1101 000X: Si 5344

U13D
Mercury_plus_CONNC

Conflicting Use

	72	IO_P_B65_REFCLK0_228_A	IO_P_B66_REFCLK1_B228_A 69
	74	IO_N_B65_REFCLK0_228_A	IO_N_B66_REFCLK1_B228_A 71
	78	IO_B65_RX0_228_A_P	IO_B66_TX0_B228_A_P 75
	80	IO_B65_RX0_228_A_N	IO_B66_TX0_B228_A_N 77
	82	IO_B65_RX1_228_A_P	IO_B66_TX1_B228_A_P 79
	84	IO_B65_RX1_228_A_N	IO_B66_TX1_B228_A_N 81
	88	IO_B65_RX2_228_A_P	IO_B66_TX2_B228_A_P 85
	90	IO_B65_RX2_228_A_N	IO_B66_TX2_B228_A_N 87
	92	IO_B65_RX3_228_A_P	IO_B66_TX3_B228_A_P 89
	94	IO_B65_RX3_228_A_N	IO_B66_TX3_B228_A_N 91
	98	IO_B65_P	IO_B66_NC_P 95
	100	IO_B65_N	IO_B66_NC_N 97
	102	IO_B65_P	IO_B66_NC_P 99
	104	IO_B65_N	IO_B66_NC_N 101
	108	IO_B64_NC_P	IO_B64_NC_P 105
	110	IO_B64_NC_N	IO_B64_NC_N 107
	112	IO_B64_NC_P	IO_B64_NC_P 109
	114	IO_B64_NC_N	IO_B64_NC_N 111
	118	IO_B64_NC_P	IO_B64_NC_P 115
	120	IO_B64_NC_N	IO_B64_NC_N 117
	122	IO_B64_NC_P	IO_B64_NC_P 119
	124	IO_B64_NC_N	IO_B64_NC_N 121
	128	IO_B64_NC_P	IO_B64_NC_P 125
	130	IO_B64_NC_N	IO_B64_NC_N 127
	132	IO_B64_NC_P	IO_B64_NC_P 129
	134	IO_B64_NC_N	IO_B64_NC_N 131
	138	IO_B64_NC_P	IO_B64_NC_P 135
	140	IO_B64_NC_N	IO_B64_NC_N 137

	Z_ID0	Z_ID1	Z_ID2
RevA	NC	NC	NC
Rev2	gnd	NC	NC

ZRevID0
ZRevID1
ZRevID2
GND_LOGIC

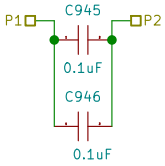
U13C
Mercury_plus_CONNC

	148	GC_B64_65_P	GC_B64_65_P 151
	150	GC_B64_65_N	GC_B64_65_N 153
	142	IO_B64_65_P	IO_B64_65_P 139
	144	IO_B64_65_N	IO_B64_65_N 141
	154	IO_B64_65_P	IO_B64_65_P 145
	156	IO_B64_65_N	IO_B64_65_N 147
	160	IO_B64_65_P	IO_B64_65_P 157
	162	IO_B64_65_N	IO_B64_65_N 159
	164	IO_B64_65_P	IO_B64_65_P 161
	166	IO_B64_65_N	IO_B64_65_N 163

1.8V ONLY!!!

STBY -> Zynq 3.3: Zynq 3.3 -> STBY
ZYNQ_M1_PS_RST
ZYNQ_M2_PS_RST

Sheet: /Zynq GPIO & MGT/Zynq IO/
File: Zynq_IO.sch
Title:
Size: B | Date: | Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1 | Id: 30/51



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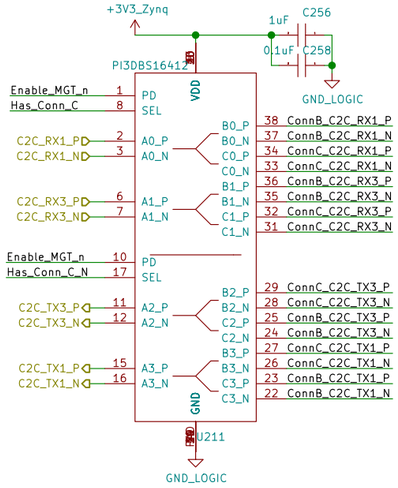
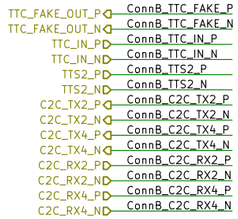
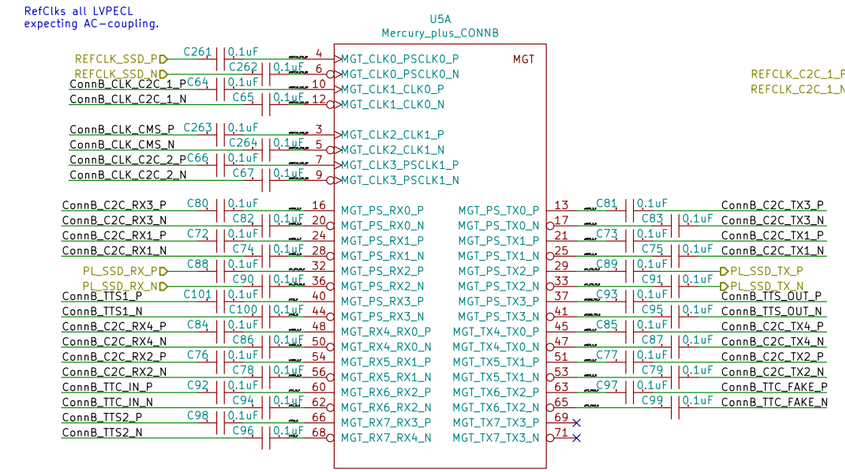
File: DP_stitch.sch

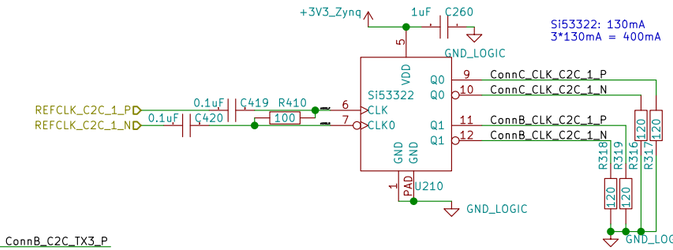
Title:

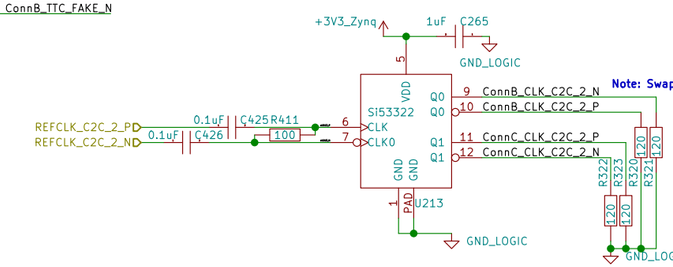
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 31/51

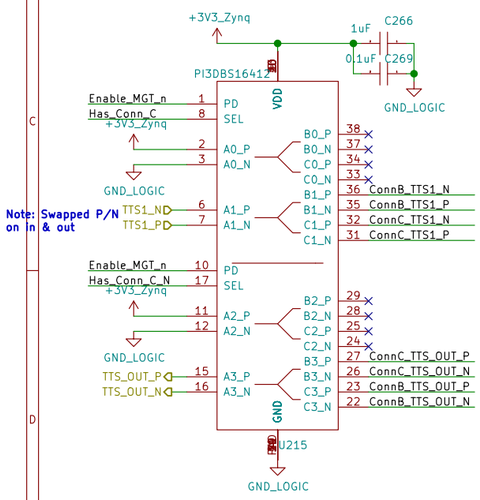


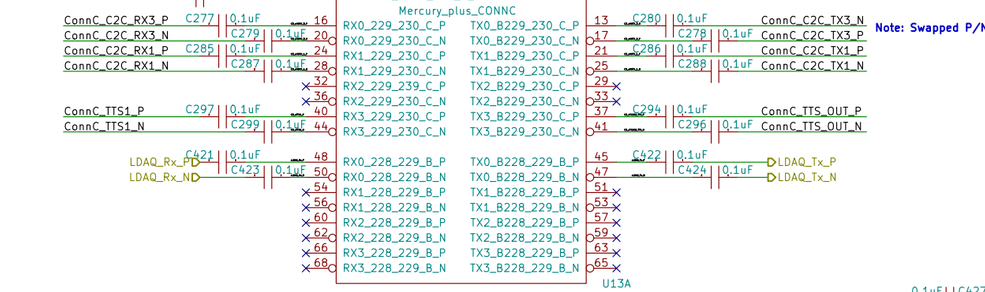


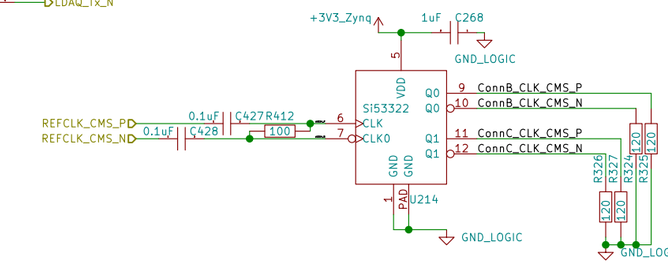


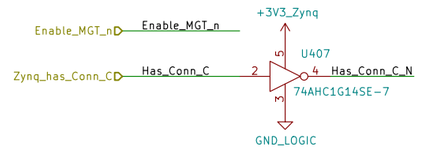








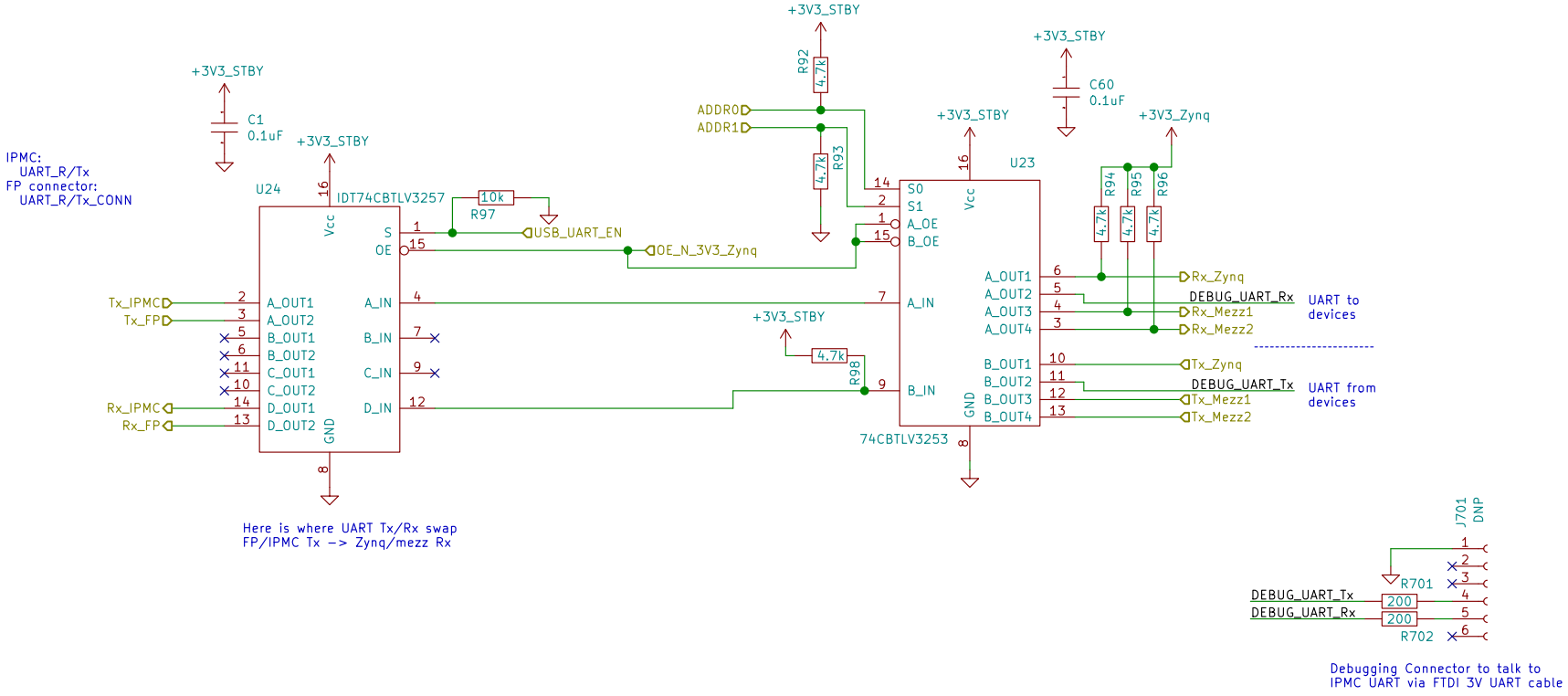




Sheet: /Zynq GPIO & MGT/Zynq MGT/
File: Zynq_MGT.sch

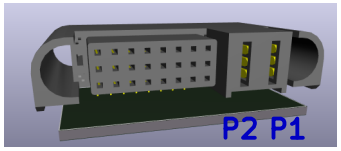
Title:

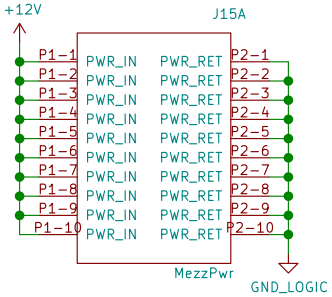
Size: B	Date:	Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 32/51

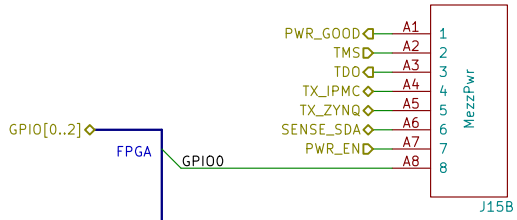


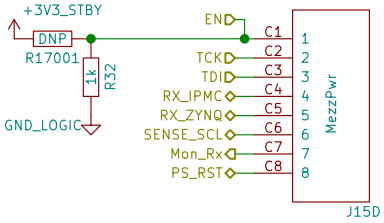
Sheet: /Mezz comm/ File: Mezz_Comm.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 33/51

Power & single-ended connector

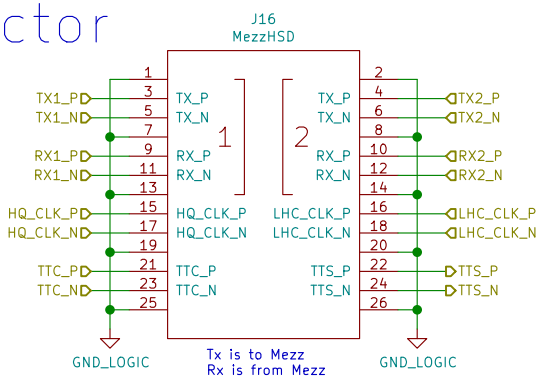


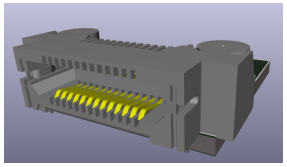






High-speed connector



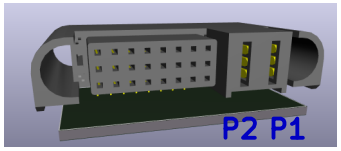


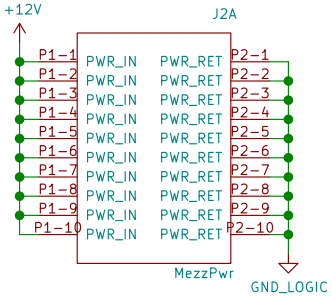
Sheet: /Mezz 1/
File: mezz.sch

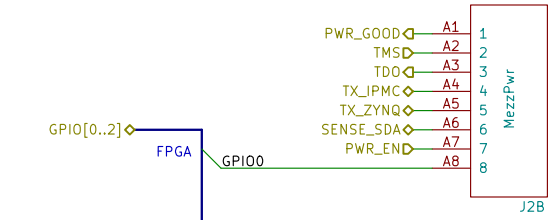
Title:

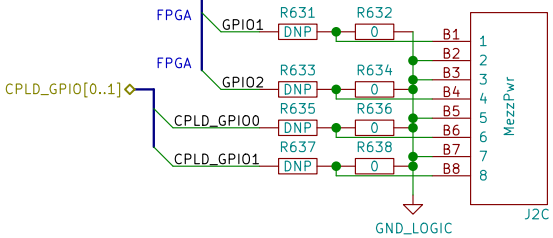
Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 34/51

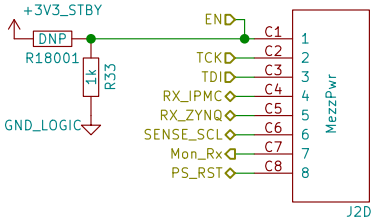
Power & single-ended connector



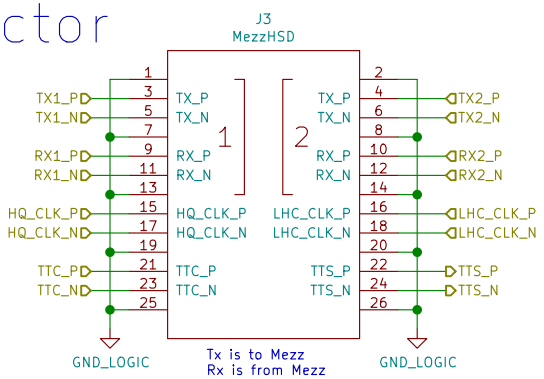


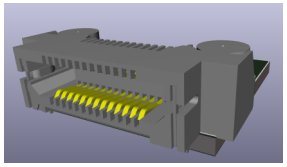






High-speed connector



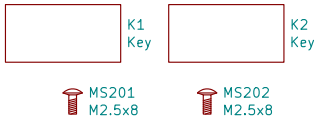


Sheet: /Mezz 2/
File: mezz.sch

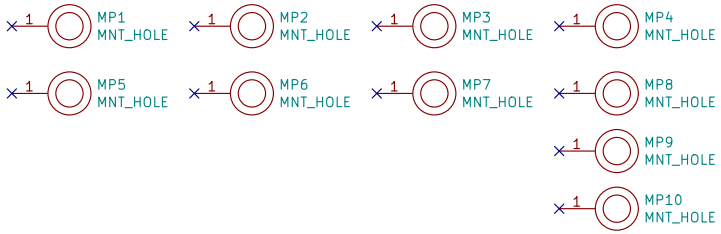
Title:

Size: USLetter	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 35/51

ATCA Keying connectors



Cover mounting

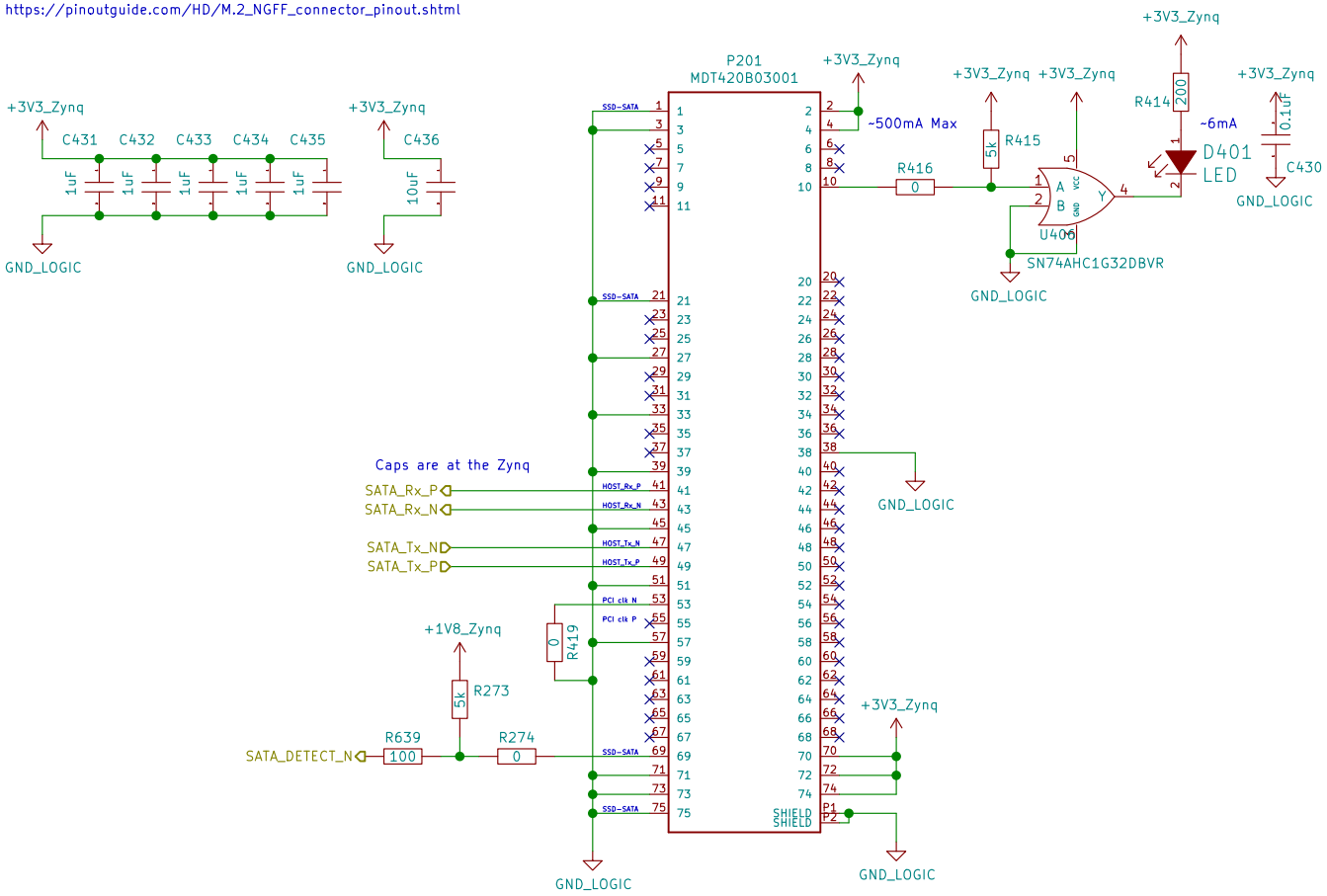


Mezz mounting

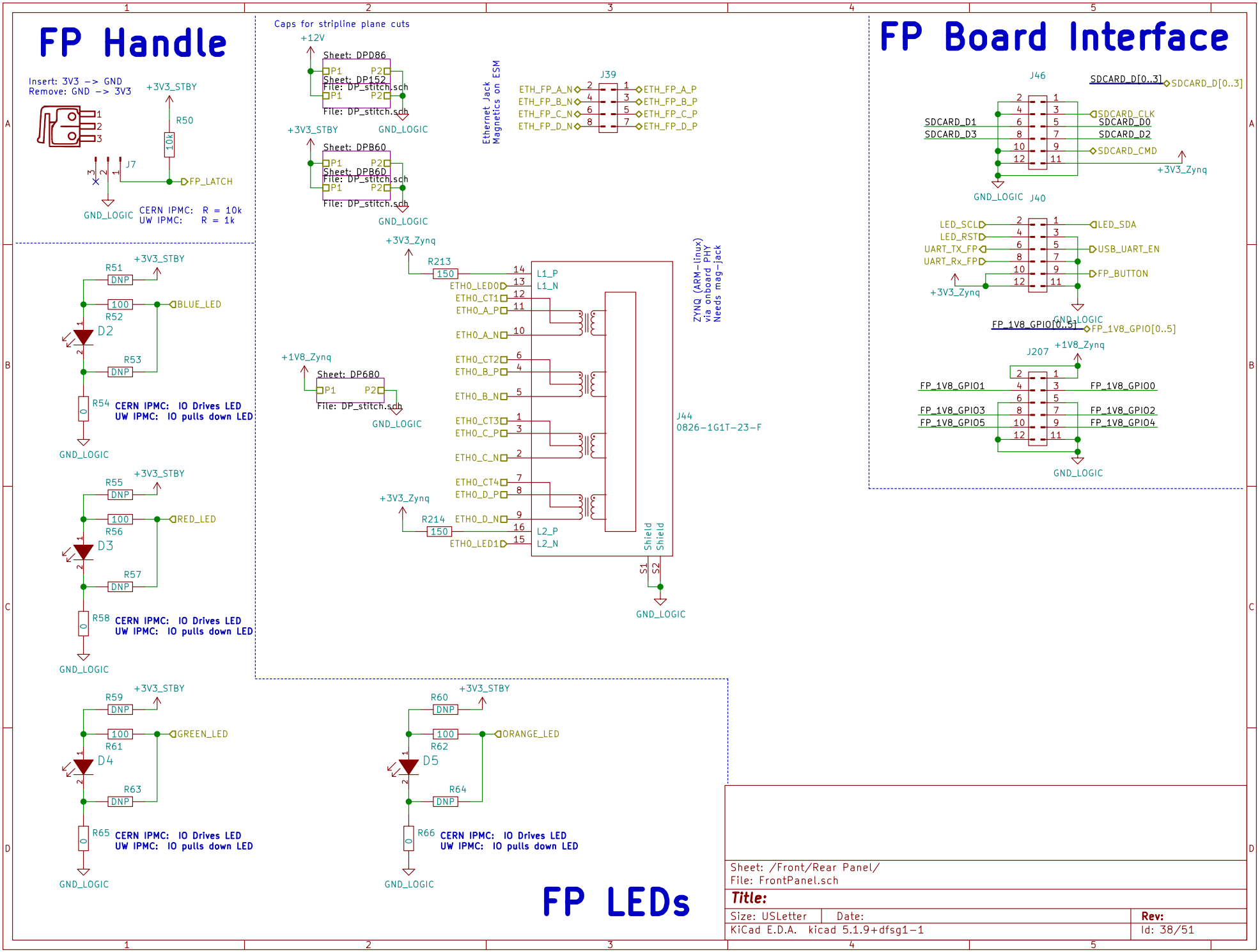
Front panel

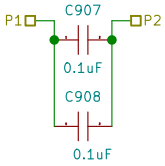
Sheet: /HW/ File: hw.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 36/51

Design from: ZCU104 eval board
M.2 2242 B
https://pinoutguide.com/HD/M.2_NGFF_connector_pinout.shtml



Sheet: /sheet5FE92DD2/		
File: SSD.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 37/51

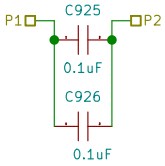

FP Handle
Insert: 3V3 -> GND
Remove: GND -> 3V3
+3V3_STBY
R50
10k
J7
FP_LATCH
GND_LOGIC
CERN IPMC: R = 10k
UW IPMC: R = 1k
Caps for stripline plane cuts
+12V
Sheet: DPD86
Sheet: DP152
File: DP_stitch.sch
GND_LOGIC
+3V3_STBY
Sheet: DPB60
Sheet: DPB6D
File: DP_stitch.sch
GND_LOGIC
Ethernet Jack
Magnetics on ESM
J39
ETH_FP_A_N
ETH_FP_B_N
ETH_FP_C_N
ETH_FP_D_N
ETH_FP_A_P
ETH_FP_B_P
ETH_FP_C_P
ETH_FP_D_P
+3V3_Zynq
R213
150
ETH0_LED0
ETH0_CT1
ETH0_A_P
ETH0_A_N
ETH0_CT2
ETH0_B_P
ETH0_B_N
ETH0_CT3
ETH0_C_P
ETH0_C_N
ETH0_CT4
ETH0_D_P
ETH0_D_N
ETH0_LED1
L1_P
L1_N
L2_P
L2_N
+1V8_Zynq
Sheet: DP680
File: DP_stitch.sch
GND_LOGIC
ZYNQ (ARM-linux)
via onboard PHY
Needs mag-jack
J44
0826-1G1T-23-F
Shield
Shield
S1
S2
GND_LOGIC
+3V3_STBY
R51
DNP
100
BLUE_LED
R52
D2
R53
DNP
R54
CERN IPMC: IO Drives LED
UW IPMC: IO pulls down LED
GND_LOGIC
+3V3_STBY
R55
DNP
100
RED_LED
R56
D3
R57
DNP
R58
CERN IPMC: IO Drives LED
UW IPMC: IO pulls down LED
GND_LOGIC
+3V3_STBY
R59
DNP
100
GREEN_LED
R61
D4
R63
DNP
R65
CERN IPMC: IO Drives LED
UW IPMC: IO pulls down LED
GND_LOGIC
+3V3_STBY
R60
DNP
100
ORANGE_LED
R62
D5
R64
DNP
R66
CERN IPMC: IO Drives LED
UW IPMC: IO pulls down LED
GND_LOGIC
FP Board Interface
J46
SDCARD_D[0..3]
SDCARD_D[0..3]
SDCARD_CLK
SDCARD_D1
SDCARD_D0
SDCARD_D3
SDCARD_D2
SDCARD_CMD
+3V3_Zynq
GND_LOGIC
J40
LED_SCL
LED_SDA
LED_RST
UART_TX_FP
USB_UART_EN
UART_Rx_FP
FP_BUTTON
+3V3_Zynq
GND_LOGIC
FP_1V8_GPIO[0..5]
FP_1V8_GPIO[0..5]
J207
+1V8_Zynq
FP_1V8_GPIO1
FP_1V8_GPIO0
FP_1V8_GPIO3
FP_1V8_GPIO2
FP_1V8_GPIO5
FP_1V8_GPIO4
GND_LOGIC
FP LEDs
Sheet: /Front/Rear Panel/
File: FrontPanel.sch
Title:
Size: USLetter
Date:
Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1
Id: 38/51



Sheet: /Front/Rear Panel/DP680/
File: DP_stitch.sch

Title:

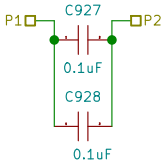
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 39/51



Sheet: /Front/Rear Panel/DPD86/
File: DP_stitch.sch

Title:

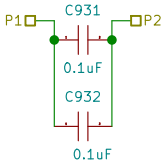
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 40/51



Sheet: /Front/Rear Panel/DP152/
File: DP_stitch.sch

Title:

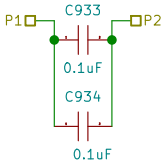
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 41/51



Sheet: /Front/Rear Panel/DPB60/
File: DP_stitch.sch

Title:

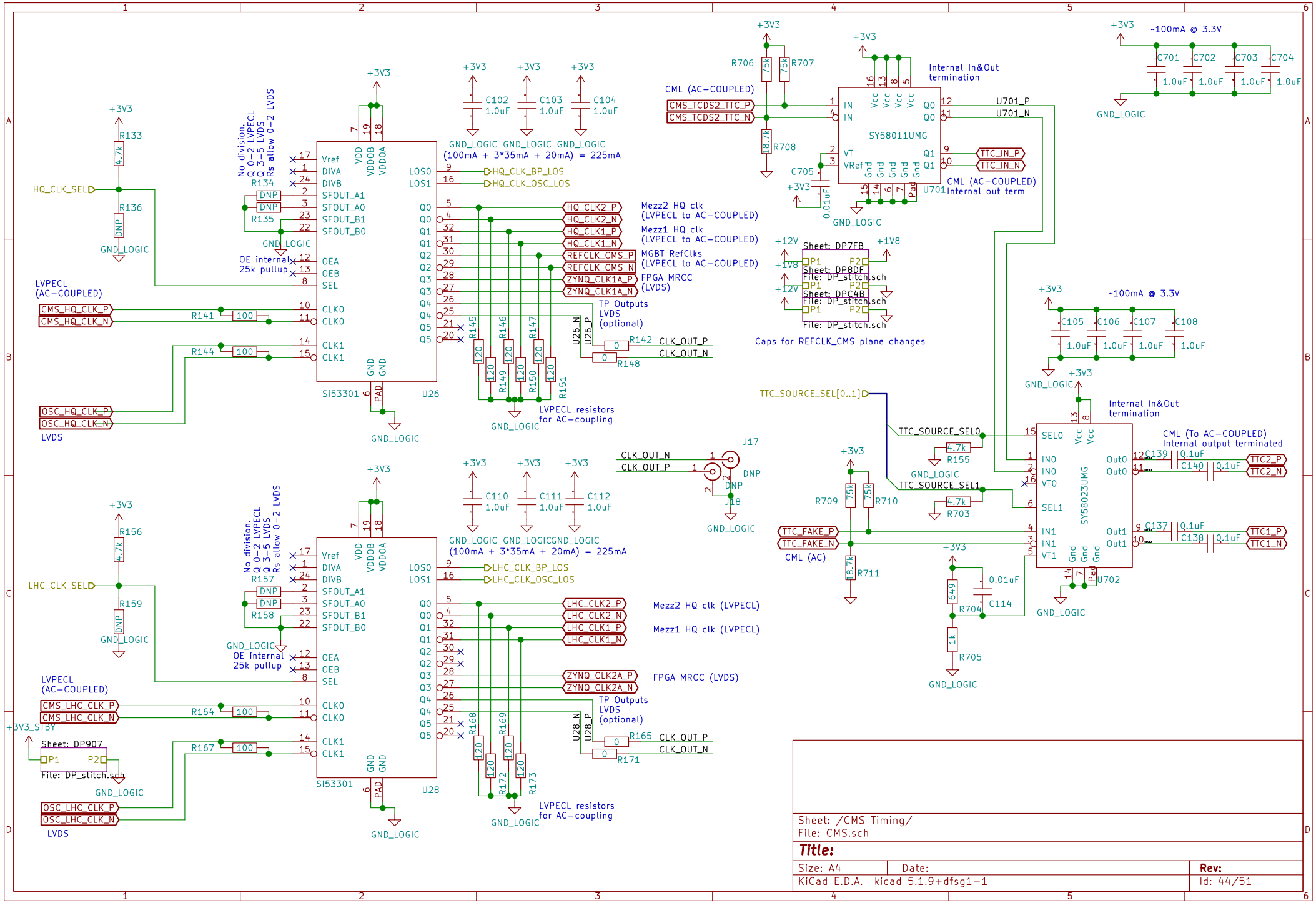
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 42/51

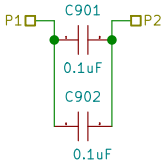


Sheet: /Front/Rear Panel/DPB6D/
File: DP_stitch.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 43/51

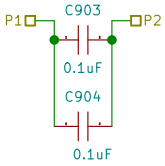

+3V3
HQ_CLK_SEL
R133
4.7k
R136
DNP
GND_LOGIC
LVPECL
(AC-COUPLED)
CMS_HQ_CLK_P
CMS_HQ_CLK_N
R141
100
R144
100
OSC_HQ_CLK_P
OSC_HQ_CLK_N
LVDS
No division.
Q 0-2 LVPECL
Q 3-5 LVDS
Rs allow 0-2 LVDS
R134
R135
DNP
OE internal
25k pullup
Vref
DIVA
DIVB
SFOUT_A1
SFOUT_A0
SFOUT_B1
SFOUT_B0
OEA
OEB
SEL
CLK0
CLK1
VDD
VDDOB
VDDOA
GND
PAD
Si53301
U26
C102
C103
C104
1.0uF
GND_LOGIC (100mA + 3*35mA + 20mA) = 225mA
LOS0
LOS1
HQ_CLK_BP_LOS
HQ_CLK_OSC_LOS
Q0
Q1
Q2
Q3
Q4
Q5
HQ_CLK2_P
HQ_CLK2_N
HQ_CLK1_P
HQ_CLK1_N
REFCLK_CMS_P
REFCLK_CMS_N
ZYNQ_CLK1A_P
ZYNQ_CLK1A_N
Mezz2 HQ clk
(LVPECL to AC-COUPLED)
Mezz1 HQ clk
(LVPECL to AC-COUPLED)
MGBT RefClks
(LVPECL to AC-COUPLED)
FPGA MRCC
(LVDS)
TP Outputs
LVDS
(optional)
R145
R146
R147
120
U26_N
U26_P
R142
R148
0
CLK_OUT_P
CLK_OUT_N
LVPECL resistors
for AC-coupling
LHC_CLK_SEL
R156
R159
R157
R158
LHC_CLK2_P
LHC_CLK2_N
LHC_CLK1_P
LHC_CLK1_N
ZYNQ_CLK2A_P
ZYNQ_CLK2A_N
Mezz2 HQ clk (LVPECL)
Mezz1 HQ clk (LVPECL)
FPGA MRCC (LVDS)
C110
C111
C112
LHC_CLK_BP_LOS
LHC_CLK_OSC_LOS
CMS_LHC_CLK_P
CMS_LHC_CLK_N
OSC_LHC_CLK_P
OSC_LHC_CLK_N
R164
R167
R165
R171
R168
R169
R172
R173
U28_N
U28_P
U28
J17
J18
CLK_OUT_N
CLK_OUT_P
DNP
+3V3_STBY
Sheet: DP907
File: DP_stitch.sch
P1
P2
R706
R707
75K
R708
18.7k
CML (AC-COUPLED)
CMS_TCDS2_TTC_P
CMS_TCDS2_TTC_N
SY58011UMG
U701
IN
VT
VRef
Q0
Q1
Vcc
Gnd
Pad
C705
0.01uF
Internal In&Out
termination
U701_P
U701_N
TTC_IN_P
TTC_IN_N
CML (AC-COUPLED)
Internal out term
~100mA @ 3.3V
C701
C702
C703
C704
C105
C106
C107
C108
Sheet: DP7FB
Sheet: DP8DF
Sheet: DPC4B
File: DP_stitch.sch
+12V
+1V8
Caps for REFCLK_CMS plane changes
TTC_SOURCE_SEL[0..1]
TTC_SOURCE_SEL0
TTC_SOURCE_SEL1
R155
R703
SY58023UMG
U702
SEL0
SEL1
IN0
IN1
VT0
VT1
Out0
Out1
C139
C140
C137
C138
0.1uF
TTC2_P
TTC2_N
TTC1_P
TTC1_N
CML (To AC-COUPLED)
Internal output terminated
TTC_FAKE_P
TTC_FAKE_N
CML (AC)
R709
R710
R711
R704
R705
649
1k
C114
0.01uF
GND_LOGIC
Sheet: /CMS Timing/
File: CMS.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1
Id: 44/51



Sheet: /CMS Timing/DP7FB/
File: DP_stitch.sch

Title:

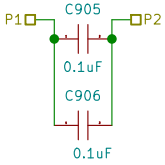
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 45/51



Sheet: /CMS Timing/DP8DF/
File: DP_stitch.sch

Title:

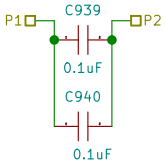
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 46/51



Sheet: /CMS Timing/DPC4B/
File: DP_stitch.sch

Title:

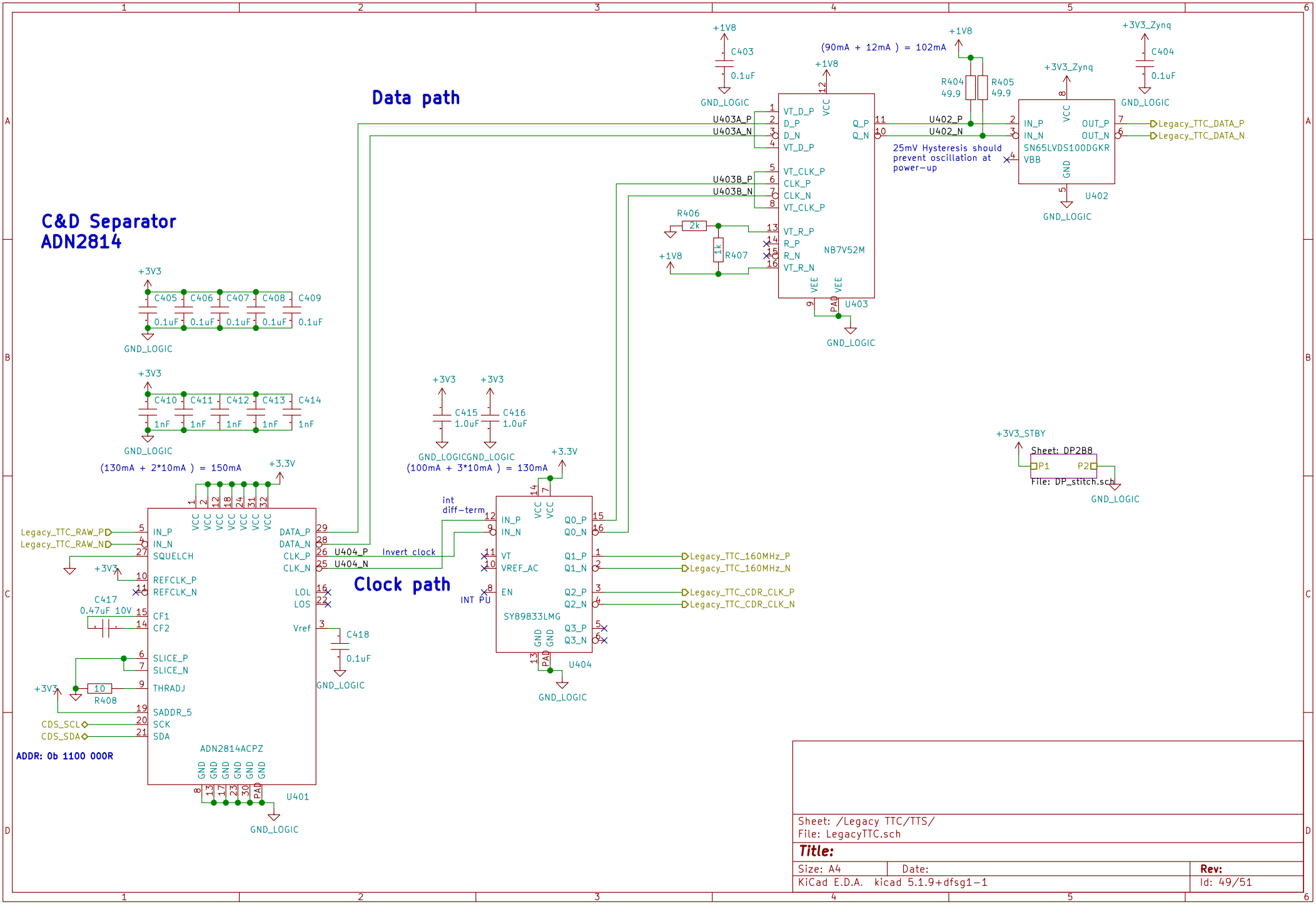
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 47/51

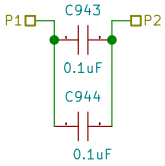


Sheet: /CMS Timing/DP907/
File: DP_stitch.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 48/51

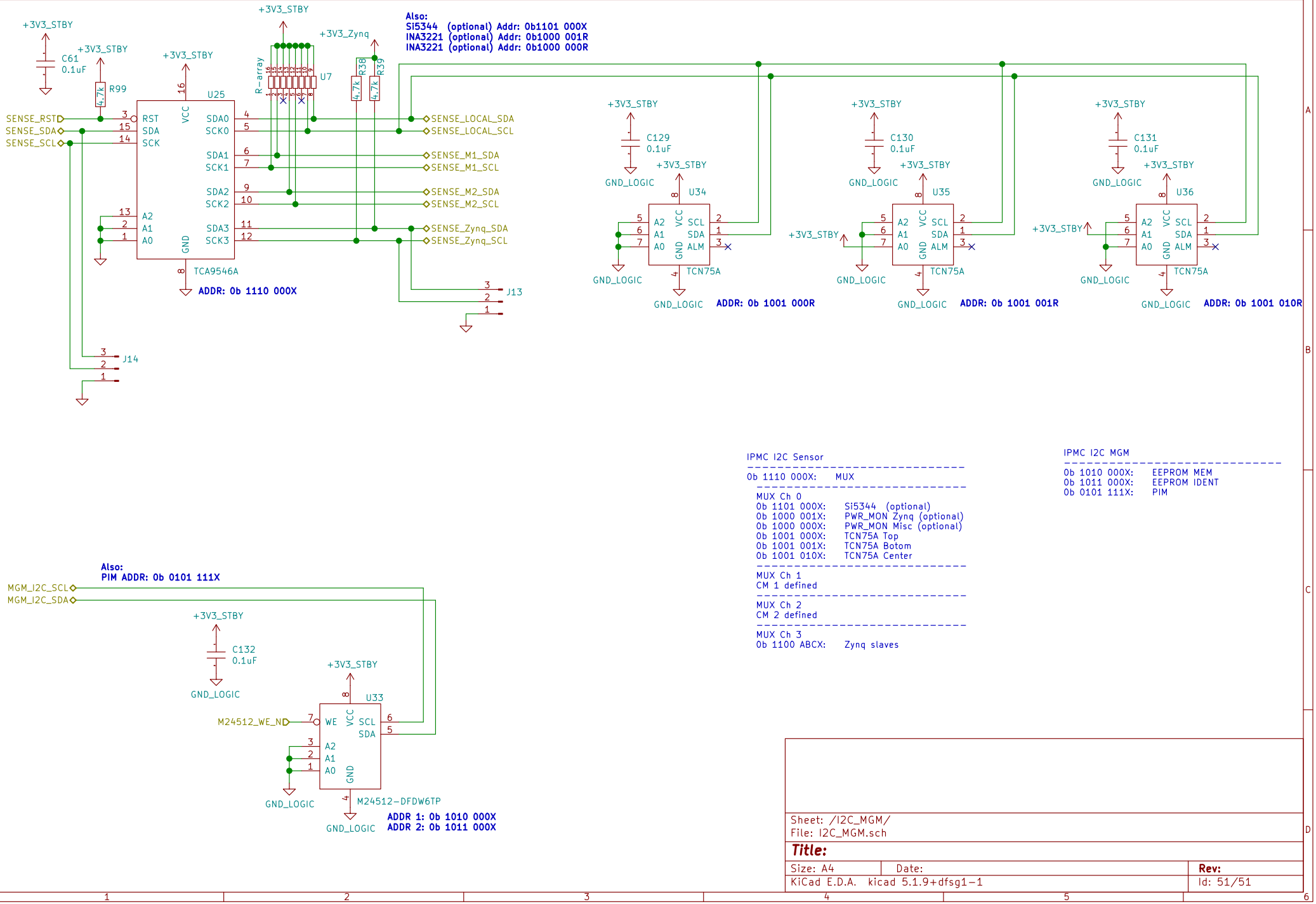

C&D Separator
ADN2814
Data path
Clock path
+1V8
C403
0.1uF
GND_LOGIC
(90mA + 12mA) = 102mA
R404
49.9
R405
49.9
+3V3_Zynq
C404
0.1uF
U403A_P
U403A_N
U403B_P
U403B_N
VT_D_P
D_P
D_N
VT_CLK_P
CLK_P
CLK_N
VT_R_P
R_P
R_N
VT_R_N
Q_P
Q_N
NB7V52M
U403
R406
2k
R407
1k
25mV Hysteresis should prevent oscillation at power-up
IN_P
IN_N
SN65LVDS100DGKR
VBB
OUT_P
OUT_N
U402
U402_P
U402_N
Legacy_TTC_DATA_P
Legacy_TTC_DATA_N
+3V3
C405
C406
C407
C408
C409
0.1uF
C410
C411
C412
C413
C414
1nF
(130mA + 2*10mA) = 150mA
+3.3V
C415
C416
1.0uF
GND_LOGICGND_LOGIC
(100mA + 3*10mA) = 130mA
+3V3_STBY
Sheet: DP2B8
P1
P2
File: DP_stitch.sch
Legacy_TTC_RAW_P
Legacy_TTC_RAW_N
IN_P
IN_N
SQUELCH
REFCLK_P
REFCLK_N
C417
0.47uF 10V
CF1
CF2
SLICE_P
SLICE_N
THRADJ
R408
10
SADDR_5
SCK
SDA
CDS_SCL
CDS_SDA
ADDR: 0b 1100 000R
ADN2814ACPZ
DATA_P
DATA_N
CLK_P
CLK_N
U404_P
U404_N
Invert clock
LOL
LOS
Vref
C418
0.1uF
U401
int
diff-term
VT
VREF_AC
EN
INT PU
SY89833LMG
Q0_P
Q0_N
Q1_P
Q1_N
Q2_P
Q2_N
Q3_P
Q3_N
U404
Legacy_TTC_160MHz_P
Legacy_TTC_160MHz_N
Legacy_TTC_CDR_CLK_P
Legacy_TTC_CDR_CLK_N
Sheet: /Legacy TTC/TTS/
File: LegacyTTC.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1
Id: 49/51



Sheet: /Legacy TTC/TTS/DP2B8/
File: DP_stitch.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.9+dfsg1-1		Id: 50/51


Also:
Si5344 (optional) Addr: 0b1101 000X
INA3221 (optional) Addr: 0b1000 001R
INA3221 (optional) Addr: 0b1000 000R
+3V3_STBY
+3V3_Zynq
C61
0.1uF
R99
4.7k
U25
TCA9546A
R-array
U7
R38
R39
SENSE_RST
SENSE_SDA
SENSE_SCL
SENSE_LOCAL_SDA
SENSE_LOCAL_SCL
SENSE_M1_SDA
SENSE_M1_SCL
SENSE_M2_SDA
SENSE_M2_SCL
SENSE_Zynq_SDA
SENSE_Zynq_SCL
J13
J14
ADDR: 0b 1110 000X
C129
U34
TCN75A
GND_LOGIC
ADDR: 0b 1001 000R
C130
U35
ADDR: 0b 1001 001R
C131
U36
ADDR: 0b 1001 010R
IPMC I2C Sensor
0b 1110 000X: MUX
MUX Ch 0
0b 1101 000X: Si5344 (optional)
0b 1000 001X: PWR_MON Zynq (optional)
0b 1000 000X: PWR_MON Misc (optional)
0b 1001 000X: TCN75A Top
0b 1001 001X: TCN75A Botom
0b 1001 010X: TCN75A Center
MUX Ch 1
CM 1 defined
MUX Ch 2
CM 2 defined
MUX Ch 3
0b 1100 ABCX: Zynq slaves
IPMC I2C MGM
0b 1010 000X: EEPROM MEM
0b 1011 000X: EEPROM IDENT
0b 0101 111X: PIM
Also:
PIM ADDR: 0b 0101 111X
MGM_I2C_SCL
MGM_I2C_SDA
C132
U33
M24512_WE_N
M24512-DFDW6TP
ADDR 1: 0b 1010 000X
ADDR 2: 0b 1011 000X
Sheet: /I2C_MGM/
File: I2C_MGM.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.9+dfsg1-1
Id: 51/51