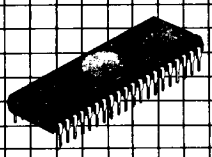
October 1986
Edition 1.0

MB89321A, MB89322A
CMOS Programmable CRT Controller

Description

The MB89321A/MB89322A Programmable CRT Controllers are single chip CMOS devices used to interface CRT raster scan displays with microcomputer systems. Both devices operate on a single +5 V power supply and have TTL-compatible I/O. The MB89321A interfaces to 6800 family microprocessors; the MB89322A to the 8080.

The MB89321A/MB89322A refresh the display by buffering information from main memory using thirty-three internal registers and keeping track of the display position of the screen. Both devices are designed to allow simple interfacing to most raster scan CRTs with a minimum of external hardware and software overhead.

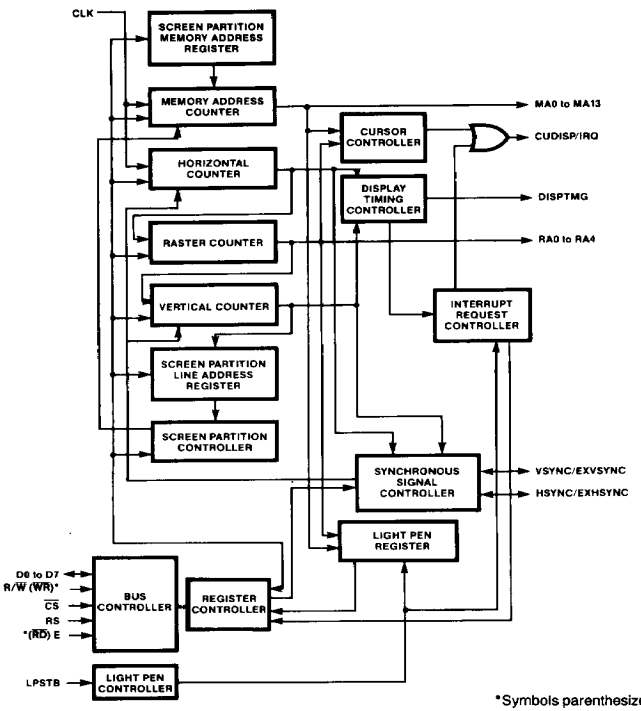


40-Lead Plastic DIP
(DIP-40P-M01)

Features

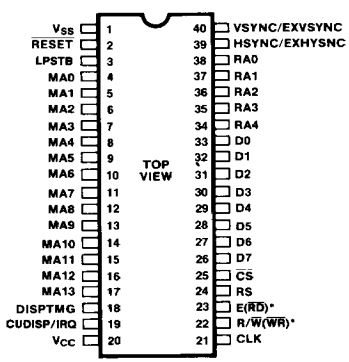
- Programmable Screen and Character Formats
- Cursor Control (3 types)
- Selectable Scan Modes (3 types)
- Light Pen Detection
- Refresh Memory Address Function
- Screen Partitioning (up to 4 partitions)
- Independent Paging/Scrolling for Each Screen Partition
- Smooth Scrolling (up to 4 screens simultaneously)
- Status Generation and Processor Interrupt Generation by Vertical Blanking or Light Pen
- External Sync for TV Superimposition (synchronous mode) or Interface to Other CRT Controllers (master-slave mode)
- Double-Size Vertical Display using Raster Interpolation
- 4.0 MHz Clock Rate
- Single +5 V Power Supply
- CMOS Process
- 40-pin Plastic DIP

Functional Block Diagram



*Symbols parenthesized are applied to MB89322A.

Pin Assignment



*Symbols parenthesized are applied to MB89322A.

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Pin Descriptions
MB89321A(MB89322A)

Pin Number	Symbol	Pin Name	Function
1	V_{SS}	Ground	Ground
2	$\overline{RESET}$	Reset	Input used for device reset. When $\overline{RESET}$ goes low: • Internal counters are cleared and stopped; • All outputs go low, and; • Control registers and status register are cleared, other internal registers unaffected. Enabled only when LPSTB is low. $\overline{RESET}$ goes high, display is initiated immediately. Control registers R30 and R31 must be initialized by software after reset is released.
3	LPSTB	Light Pen Strobe	Character detection input. When high, the memory address is loaded in the light pen register, the raster address in the light pen raster register, and the status bit set.
4 to 17	MA0 to MA13	Memory Address	Refresh memory address output
18	DISPTMG	Display Timing	Display timing output. Set to high during display.
19	CUDISP/ IRQ	Cursor Display Timing/ Interrupt Request	Cursor display timing output/interrupt request output. Set to high during display. Setting the control register enables a high-level interrupt request signal to be output while the display timing signal is low.
20	V_{CC}	Power Supply	+5 V power supply.
21	CLK	Clock	Clock input. Goes low during EXHSYNC in TV sync mode.
22	R/$\overline{W}$ ($\overline{WR}$)*	Read/Write (Write)	MPU read/write input. (MPU write input)
23	E ($\overline{RD}$)*	Enable (Read)	MPU enable input. (MPU read input)
24	RS	Register select	Internal register select input. Normally connected to the least significant bit (A0) of the address bus. When high, selects internal registers; when low, the address register.
25	$\overline{CS}$	Chip select	Chip select input. Goes low when the MPU accesses the CRTC.
26 to 33	D7 to D0	Data Bus	MPU data bus pins
34 to 38	RA4 to RA0	Raster Address	Raster address output
39	HSYNC/ EXHSYNC	Hsync Output/ Hsync Input	Horizontal sync output/external horizontal sync input. When reset, becomes the horizontal sync output.
40	VSYNC/ EXVSYNC	Vsync Output/ Vsync Input	Vertical sync output/external vertical sync input. When reset, becomes the vertical sync output.

*Symbols parenthesized are applied to MB89322A.

Internal Registers and Functions

CS	RS	Address 4	3	2	1	0	Register Number	Register Name	Read Write	Data Bit 7	6	5	4	3	2	1	0
1	x	x	x	x	x	x	—	Invalid	—								
0	0	x	x	x	x	x	AR	Address Register	W								
0	1	0	0	0	0	0	R0	Total Number of Characters in Line (*)	W								
0	1	0	0	0	0	1	R1	Number of Characters Displayed in Line	W								
0	1	0	0	0	1	0	R2	Horizontal Sync Position (*)	W								
0	1	0	0	0	1	1	R3	Sync Signal Pulse Width	W	V3	V2	V1	V0	H3	H2	H1	H0
0	1	0	0	1	0	0	R4	Total Number of Lines (*)	W								
0	1	0	0	1	0	1	R5	Total Raster Adjust	W								
0	1	0	0	1	1	0	R6	Number of Lines Displayed	W								
0	1	0	0	1	1	1	R7	Vertical Sync Position (*)	W								
0	1	0	1	0	0	0	R8	Scan Mode/Skew	W	C1	C0	D1	D0			I1	I0
0	1	0	1	0	0	1	R9	Maximum Raster Address	W								
0	1	0	1	0	1	0	R10	Cursor Start Raster	W		B1	B0					
0	1	0	1	0	1	1	R11	Cursor End Raster	W								
0	1	0	1	1	0	0	R12	Start Address 1	R/W								
0	1	0	1	1	0	1	R13										
0	1	0	1	1	1	0	R14	Cursor	R/W								
0	1	0	1	1	1	1	R15										
0	1	1	0	0	0	0	R16	Light Pen	R								
0	1	1	0	0	0	1	R17										
0	1	1	0	0	1	0	R18	Screen 2 Display Start Position (*)	R/W								
0	1	1	0	0	1	1	R19	Start Address 2	R/W								
0	1	1	0	1	0	0	R20										
0	1	1	0	1	0	1	R21	Screen 3 Display Start Position (*)	R/W								
0	1	1	0	1	1	0	R22	Start Address 3	R/W								
0	1	1	0	1	1	1	R23										
0	1	1	1	0	0	0	R24	Screen 4 Display Start Position (*)	R/W								
0	1	1	1	0	0	1	R25	Start Address 4	R/W								
0	1	1	1	0	1	0	R26										
0	1	1	1	0	1	1	R27	Vertical Sync Position Fine Adjust	W								
0	1	1	1	1	0	0	R28	Light Pen Raster	R	DP							
0	1	1	1	1	0	1	R29	Smooth Scroll	R/W								
0	1	1	1	1	1	0	R30	Control	W	VE	VS	IB	IL	SY	TV	P1	P0
0	1	1	1	1	1	1	R31	Control/Status	R/W	SS3	SS2	SS1	SS0	RI*	E	SB	SL

***Note:** Values written to these registers are one (1) less than the set values; refer to Notes on operation

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Register Description

Address Register (AR)

Sets the number of the internal register. Unchanged until a new value is written.

Total Number of Characters in Line Register (RO)

Sets horizontal scan sync. Settings indicate number of characters, and are determined by the formula:

Total Number of Characters in Line x Character Period = Horizontal Scan Period

Values written to the register are 1 less than the set values.

Number of Characters Displayed in Line Register (R1)

Sets the horizontal display period. Settings indicate number of characters.

Horizontal Sync Position Register (R2)

Sets the horizontal sync signal position. Settings indicate number of characters. Values written to the register are 1 less than the set values.

Sync Signal Pulse Width Register (R3)

MSB							LSB
V3	V2	V1	V0	H3	H2	H1	H0

Sets the sync signal pulse width. The 4 high-order bits are used for the vertical sync signal, the 4 low-order bits for the horizontal sync signal. the TV sync mode, the 4 low-order bits are used as the horizontal back porch.

Total Number of Lines Register (R4)

Used the the total raster adjust register to set vertical sync (field sync is set by number of rasters). Setting is in number of lines. Values written to the register are 1 less than the set value.

Total Raster Adjust Register (R5)

Used to fine tune the vertical sync. Settings indicate number of rasters, and must be less than the maximum raster address. Vertical sync is determined by the formula:

Vertical Sync = Total Number of Lines x Maximum Raster Address + Total Raster Adjust

Number of Lines Displayed Register (R6)

Sets the vertical display period. Settings indicate number of lines.

Vertical Sync Position Register (R7)

Used with the vertical sync position fine adjust register (R27) to set vertical sync position using raster count. Settings indicate number of lines. Values written to the register are 1 less than the set values.

Scan Mode/Skew Register (R8)

MSB						LSB
C1	C0	D1	D0		I1	I0

Sets cursor display signal and display timing signal skew, and the scan mode. Bit functions are as shown below:

C1	C0	CUDISP Output
0	0	Output without skew
0	1	Skewed by 1 character
1	0	Skewed by 2 characters
1	1	No CUDISP output

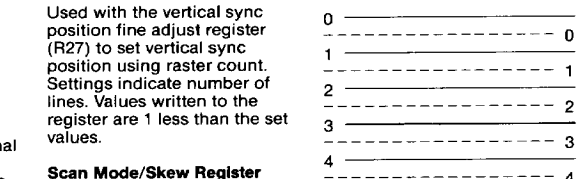
D1	D0	DISPTMG Output
0	0	Output without skew
0	1	Skewed by 1 character
1	0	Skewed by 2 characters
1	1	No DISPTMG output

I1	I0	Scan Mode
0	0	Non-interlace mode
0	1	Interlace mode
1	0	Non-interlace mode
1	1	Interlace and video mode

Maximum Raster Address Register (R9)

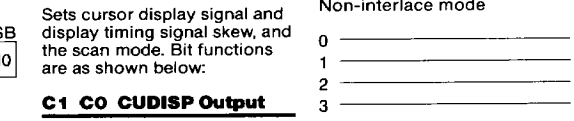
Sets the number of rasters in a line. In interlace and non-interlace modes, the value written is 1 less than the set value; in interlace and video mode, 2 less. Examples of settings in each mode are as follows:

Interlace mode



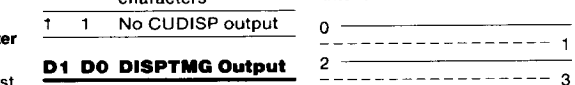
Raster count - 5
Value written - 4

Non-interlace mode



Raster count - 5
Value written - 4

Interlace & video modes

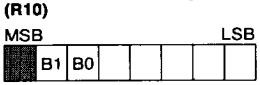


Raster count - 5
Value written - 3

Non-interlace mode and Interlace mode:
Written value = Setting value − 1
Interlace mode & video mode:
Written value = Setting value − 2

Register Description
(Continued)

Cursor Start Raster Register (R10)



Sets the cursor display mode and the display start raster. Settings indicate number of rasters. Cursor display mode bit function is as follows:

B1	B0	Cursor Display Mode
0	0	Displays without blinking
0	1	No display
1	0	Blinks in 16-field sync
1	1	Blinks in 32-field sync

Cursor End Raster Register (R11)

Sets the cursor display end raster. Settings indicate number of rasters.

Start Address Registers (R12, R13, R19, R20, R22, R23, R25, R26)

Four sets of 14-bit paired registers used to set the starting memory address for screen display that enable independent paging/scrolling when screen is partitioned. Registers are for Start Address 1 (R12, R13), Start Address 2 (R19, R20), Start Address 3 (R22, R23) and Start Address 4 (R25, R26).

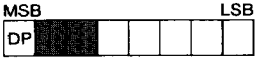
Cursor Registers (R14, R15)

14-bit paired registers used to set the cursor display memory address.

Light Pen Registers (R16, R17)

14-bit paired registers to which the memory address is written when the light pen strobe signal goes high. Memory address value must be compensated in software for delay in the light pen detection circuit.

Light Pen Raster Register (R28)

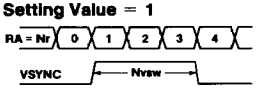


Register to which the raster address and display status bit are written when the light pen strobe signal goes high. When the light pen register or light pen raster register are written to during the display period, the display status bit is set to 1; during blank period, reset to 0.

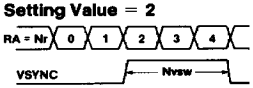
Vertical Sync Position Fine Adjust Register (R27)

Used to fine-tune the vertical sync signal within the line set by the vertical sync position register. Settings indicate number of rasters. Examples of settings are shown below:

Setting Value = 1



Setting Value = 2



Setting 0 must not be written as it will cause the control register to disable the vertical sync position adjust register, resulting in a vertical sync signal output of RA = 0. The set value must be less than the maximum raster address.

Display Start Position Registers (R18, R21, R24)

Sets the starting line numbers for display start addresses 2, 3, and 4 when screen is partitioned. See following figure. Values written to the register are 1 less than the line number; 0 must not be written. Examples of settings are shown below:

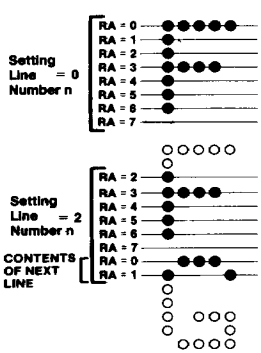
Line Number	Display Screen
0 1 2	Screen 1 (Start address 1)
3	Screen 2 (Start address 2, Register 18)
4 5 6 7	Screen 3 (Start address 3, Register 21)
8 9	Screen 4 (Start address 4, Register 24)

Value written for start position 2 = 2
Value written for start position 3 = 3
Value written for start position 4 = 7

Smooth Scroll Register (R29)

Sets the starting raster address within a line. Setting indicates number of rasters. Smooth scrolling can be used in interlace and non-interlace modes only.

Settings are valid for screens specified by SS3 to SS0 of the control/status register. Settings must be less than the maximum raster address. Examples of settings are shown below:



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Register Description
(Continued)

Control Register (R30)

MSB							LSB
VE	VS	IB	IL	SY	TV	P1	P0

Controls the external sync function, interrupt function, vertical sync position fine adjust function and screen partition function. This register must be initialized by software after reset is released. Bit functions are as shown below:

VE	VS	TV	External Sync Function
0	0	0	Both VSYNC and HSYNC are in output mode. DISPTMG is active. External sync operation is disabled.
0	1	0	Outputs VSYNC for odd-numbered fields only in interlace mode. No VSYNC output when the programmed values of max. raster address and vertical sync position are odd numbers in interlace & video mode.
1	0	0	EXVSYNC is in input mode but external sync signal ignored. DISPTMG is active.
1	1	0	EXVSYNC is in input mode and external sync signal is accepted. DISPTMG goes low (disabled).
0	0	1	Disallowed
0	1	1	Disallowed
1	0	1	Both EXVSYNC and EXHSYNC are in input mode and external sync signal is accepted. DISPTMG output is active.
1	1	1	Both EXVSYNC and EXHSYNC are in input mode and external sync signal is accepted. DISPTMG goes low (disabled).

Notes:
1. When VS = 1, DISPTMG goes low.
2. When TV = 0, indicates master-slave mode. When TV = 1, indicates TV sync mode.
3. In TV sync mode, the horizontal back porch must be set using the horizontal sync pulse width register.
4. In TV sync mode, the internal control is in non-interlace mode.

IB	IL	Interrupt Function
0	0	None
0	1	With light pen strobe
1	0	With vertical blanking
1	1	With light pen or vertical blanking

Note: Interrupt signal is output for CUDISP while DISPTMG is low.

SY	Vertical Sync Position Fine Adjust Function
0	Vertical sync position fine adjust register disabled
1	Vertical sync position fine adjust register enabled

P1	P0	Screen Partition Function
0	0	Start Address 1 enabled
0	1	Start addresses 1 and 2 enabled; screen partitioned into two sections
1	0	Start addresses 1, 2, and 3 enabled; screen partitioned into three sections
1	1	Start addresses 1, 2, 3, and 4 enabled; screen partitioned into four sections

Note: Screen address 1 is always displayed starting from line number 0.

Register Description
(Continued)

Control/Status Register (R31)

Controls the smooth scrolling and raster interpolation functions, and performs read/write of the status register. This register must be initialized by software after reset is released. Control bit functions are as follows:

Control Bits	Function
SS3 to SS0	Smooth scrolling control bits; when set to 1 the smooth scrolling register is enabled. Bits correspond to the screens as follows: SS3 = screen 4 SS2 = screen 3 SS1 = screen 2 SS0 = screen 1
RI	Raster interpolation bit. Set to 1, raster interpolation is performed. The raster counter is incremented every two rasters, doubling the vertical sync rate. Therefore, in this case, registers related to vertical sync control must be reprogrammed. The raster interpolation function can't be used in external sync mode and interlace & video mode.

Notes:
1. "0s" must be written to lower 3 bits of the control register.
2. Refer to diagram of "Double-Size Vertical Display" and item 6 of Notes on Operation.

Status Bits

The functions of status bits are as follows:

E	Display Field Status
0	Odd-numbered screen display, or in non-interlace mode
1	Even-numbered screen display

SB	Vertical Blanking Status
0	During screen display
1	During vertical blanking

SL	Light Pen Strobe Status
0	Light pen strobe ignored
1	Light pen strobe accepted

Notes:
1. Light pen strobe status is cleared by reset or by read of the status register.
2. Vertical blanking status and light pen strobe status are set regardless of the setting of the control register interrupt function.
3. E bit is controlled by the vertical blank. Therefore, E bit status is different from normal field image, and it's update timing changes depending on number of lines displayed. To get correct status, E bit must be read immediately after the display period.

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Restrictions on Values Written to Registers

Values which may be written to internal registers are as follows:

(1) $0 < \text{number of characters displayed in line } (R1) < \text{total number of characters in line } (R0) + 1 \leq 256$

(2) $0 <$ number of lines displayed (R6) $<$ total number of lines (R4) $+ 1 \leq 128$

(3) $0 \leq$ horizontal sync position (R2) $\leq$ total number of characters in line (R0)

(4) $0 \leq$ vertical sync position (R7) $\leq$ total number of lines (R4)

(5) $0 \leq$ cursor start raster (R10) $\leq$ cursor end raster (R11) $\leq$ maximum raster address (R9)
(interlace mode and non-interlace modes)
$0 \leq$ cursor start raster (R10) $\leq$ cursor end raster (R11) $\leq$ maximum raster address (R9) $+ 1$
(interlace & video mode)

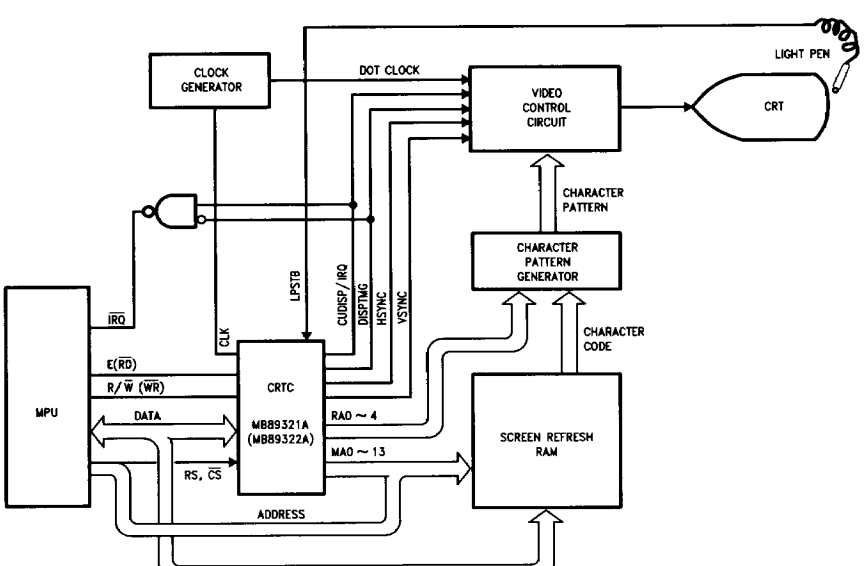
(6) $2 \leq$ maximum raster address (R9) ≤ 30
(interlace & video mode only)

(7) $3 \leq$ total number of characters in line (R0)
(except in non-interlace mode)
$5 \leq$ total number of characters in line (R0)
(non-interlace mode only)

(8) Vertical sync position fine adjust (R27) $<$ maximum raster address (R9)

(9) Smooth scroll (R29) $\leq$ maximum raster address (R9)

System Block Diagram



Programmable Values

Programmable values which can be written to registers and their respective symbols are as shown below:

Register Number	Register Name	Programmable Value	Symbol
R0	Total Number of Characters in Line	Characters	Nht
R1	Number of Characters Displayed in Line	Characters	Nhd
R2	Horizontal Sync Position	Characters	Nhsp
R3	Sync Signal Pulse Width	Rasters/Characters	Nvsw/Nhsw
R4	Total Number of Lines	Lines	Nvt
R5	Total Raster Adjust	Rasters	Nadj
R6	Number of Lines Displayed	Lines	Nvd
R7	Vertical Sync Position	Lines	Nvsp
R8	Scan Mode/Skew		
R9	Maximum Raster Address	Rasters	Nr
R10	Cursor Start Raster	Rasters	N_{CSTART}
R11	Cursor End Raster	Rasters	N_{CEND}
R12 R13	Start Address 1		N_{S1}
R14 R15	Cursor		
R16 R17	Light Pen		
R18	Screen 2 Display Start Position	Lines	N_{L2}
R19 R20	Start Address 2		N_{S2}
R21	Screen 3 Display Start Position	Lines	N_{L3}
R22 R23	Start Address 3		N_{S3}
R24	Screen 4 Display Start Position	Lines	N_{L4}
R25 R26	Start Address 4		N_{S4}
R27	Vertical Sync Position Fine Adjust	Rasters	Nspadj
R28	Light Pen Raster		
R29	Smooth Scroll	Rasters	Nradj
R30	Control		
R31	Control/Status		

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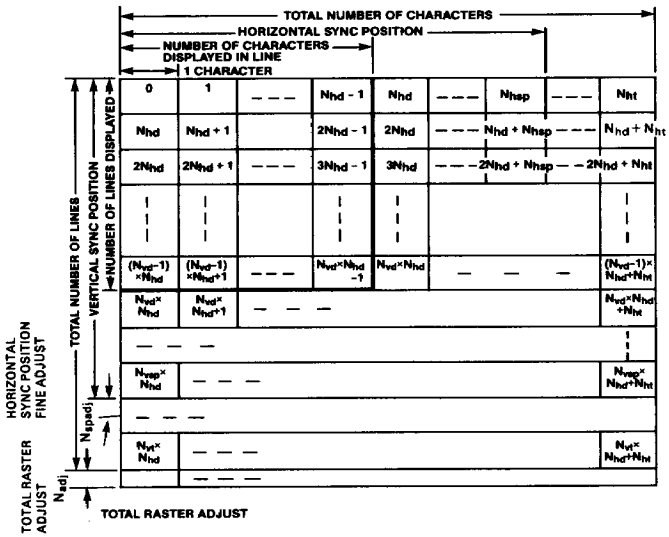
Screen Format



Line numbers are counted starting at the following addresses:

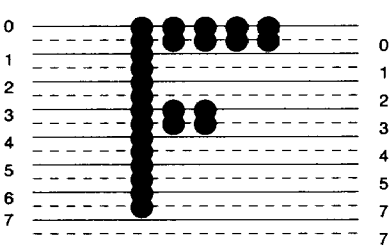
Line number 0 = starts from memory address 0
Line number 1 = starts from memory address Nhd
Line number 2 = starts from memory address 2Nhd

Line number n = starts from memory address (Nvd–1)Nhd

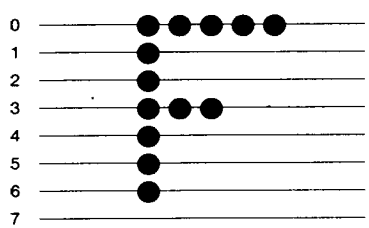
Scan Mode

Examples of format during scan mode:

Interlace Mode



Non-Interlace Mode

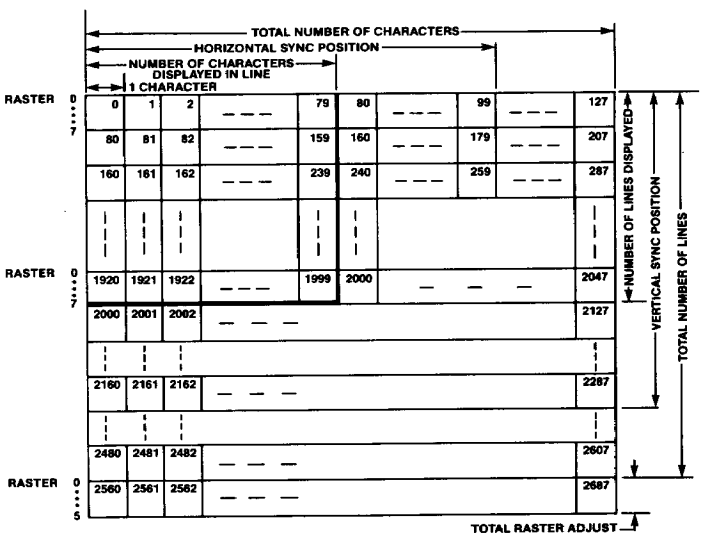


Example of Screen Format

Dot clock rate	16.128 MHz
Horizontal frequency	15.75 kHz
Vertical frequency	60.1145 Hz

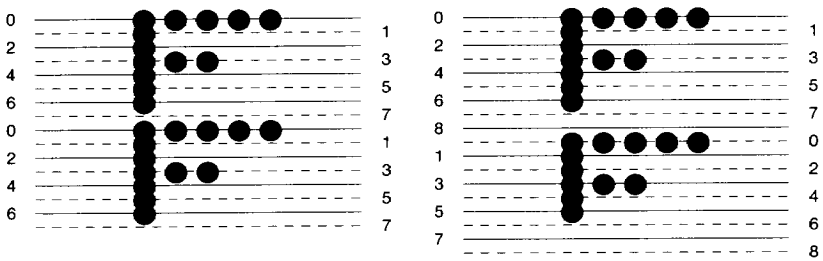
At the following clock rates and register settings, the screen format is as shown in the diagrams below:

Total number of characters in line, Register 0:	127
Number of characters displayed in line, Register 1:	80
Horizontal sync position, Register 2:	99
Sync signal pulse width, Register 3:	8
Total number of lines, Register 4:	31
Total raster adjust, Register 5:	6
Number of lines displayed, Register 6:	25
Vertical sync position, Register 7:	27
Maximum raster address, Register 9:	8



Scan Mode
(Continued)

Interlace & Video Modes

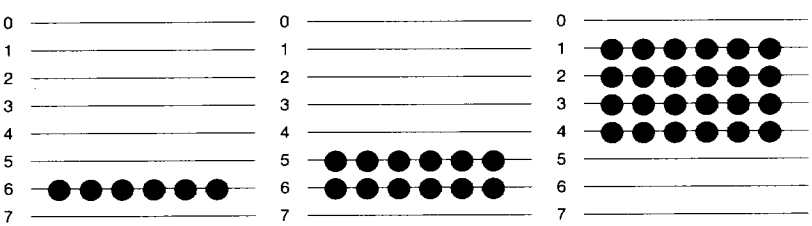


Even number of rasters in a line

Odd number of rasters in a line

Cursor Control

Examples of settings for the cursor start and end raster registers:



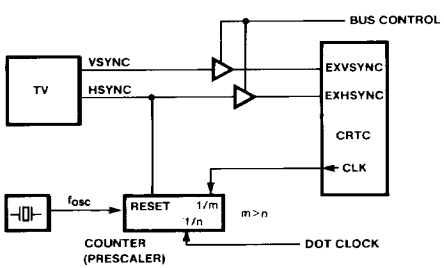
Start address = 6
End address = 6

Start address = 5
End address = 6

Start address = 1
End address = 4

TV Sync Mode

Example of a TV Sync mode circuit:

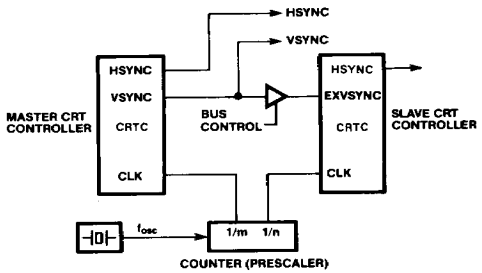


TV sync mode is used to superimpose displays on TV or video signals. In the above example a 1/n f_{OSC} dot shift will occur. Accordingly, an appropriate prescaler should be designed to avoid image resolution problems.

During HSYNC, CLK must be low (stopped).

Master-Slave Mode

Example of a master-slave mode circuit:

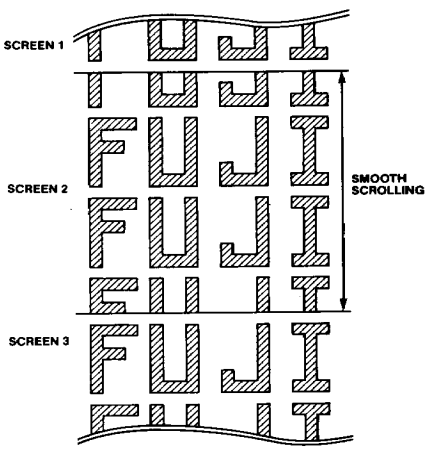


Master-slavemode is used to synchronize master and slave CRT controllers. The screen formats and clock phases of the two CRTCs must match.

Since HSYNC is output, PLL can be used.

Smooth Scroll

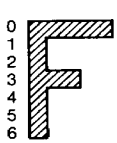
Example of smooth scrolling display:



In the example, screen 2 is being smooth scrolled.

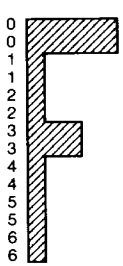
Double-Size Vertical Display

Raster Address



Without raster interpolation function

Raster Address



With raster interpolation function

The vertical size of the display can be doubled using the raster interpolation function as shown in the example.

In raster interpolation, the raster address is updated every second raster.

Refer to item 6 of Notes on Operation.

4

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Input Voltage	V_{IN}	−0.3 to +7.0	V
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{STG}	−55 to +150	°C
Power Dissipation	P_D	600	mW

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter		Symbol	Value Min.	Typ.	Max.	Unit
Supply Voltage		V_{CC}	4.5	5.0	5.5	V
		V_{SS}		0.0		V
Input High Voltage	LPSTB, CLK	V_{IH1}	2.2		V_{CC}	V
	Other Inputs	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	LPSTB, CLK	V_{IL1}	−0.3		0.6	V
	Other Inputs	V_{IL}	−0.3		0.8	V
Ambient Temperature		T_A	−20	25	+75	°C

DC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter		Symbol	Test Conditions	Value Min	Typ	Max	Unit
Input High Voltage	LPSTB, CLK	V_{IH1}		2.2		V_{CC}	V
	Other Inputs	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	LPSTB,CLK	V_{IL1}		−0.3		0.6	V
	Other Inputs	V_{IL}		−0.3		0.8	V
Input Leakage Current	D0 to D7, EXHSYNC, EXVSYNC	I_{IL}	V_{IN} = 0.4 V to 2.4 V, V_{CC} = 5.5 V	−10		10	μA
	Other Inputs	I_{IL_1}	V_{IN} = 0 V to 5.5 V	−2.5		2.5	μA
Output High Voltage	D0 to D7	V_{OH}	I_{OH} = −205 μA	2.4			V
	Other Outputs	V_{OH1}	I_{OH} = −100 μA	2.4			V
Output Low	Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input Capacitance	D0 to D7, EXHSYNC, EXVSYNC	C_{IN}	V_{IN} = 0 V			12.5	pF
	Other Outputs	C_{IN_1}	f = 1.0 MHz			10.0	pF
Ouput Capacitance		C_{OUT}				10.0	pF
Power Dissipation		P_D	V_{CC} = V_{max} f = 1.0 MHz		10	30	mW

AC Characteristics

Recommended operating conditions unless otherwise noted.

Parameter		Symbol	Conditions	Value Min.	Typ.	Max.	Unit
CRT Controller	Clock Period	t_{CLK}	(1)	250			ns
	Clock High	t_{PWCH}		100			ns
	Clock Low	t_{PWCL}		100			ns
	Clock Rise	t_{CR}				20	ns
	Clock Fall	t_{CF}				20	ns
	Memory Address Delay	t_{MAD}				80	ns
	Raster Address Delay	t_{RAD}				100	ns
	Display Timing Delay	t_{DTD}				120	ns
	Cursor Timing Delay	t_{CDD}				120	ns
	Horizontal Synchronous Delay	t_{HSD}				100	ns
	Vertical Synchronous Delay	t_{VSD}				120	ns
External Synchronization	Clock Stop	t_{CLKST}	(2)	100			ns
	External Horizontal Synchronous Signal Width	t_{PWHS}		1000			ns
	External Horizontal Synchronous Rise	t_{HR}				20	ns
	External Horizontal Synchronous Fall	t_{HF}				20	ns
	External Vertical Synchronous Signal Width *1	t_{PWVS}/ t_{PWVSS}		1220/ 1750			ns
	External Vertical Synchronous Rise	t_{VR}				20	ns
	External Vertical Synchronous Fall	t_{VF}				20	ns
	External Synchronous Setup (Master-slave mode)	t_{VSS}		50			ns
Light Pen	Light Pen Strobe Width	t_{PWLP}	(3)	60			ns
	Light Pen Strobe Maximum Period	t_{LPDR}				0	ns
		t_{LPDF}				70	ns
CRT Interface 1	Enable Period	t_E	[(4) MB89321A only]	0.5			μs
	Enable High	t_{PWEH}		0.22			μs
	Enable Low	t_{PWEL}		0.21			μs
	Enable Rise	t_{ER}				20	ns
	Enable Fall	t_{EF}				20	ns
	Address Setup	t_{AS}		40			ns
	Data Delay	t_{DDR}				120	ns
	Data Access	t_{ACC}				160	ns
	Address Hold	t_{AH}		10			ns
	Data Hold	t_H		10			ns
	Data Setup	t_{DSW}		60			ns

4

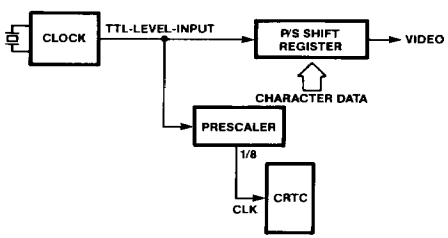
AC Characteristics
(Continued)

Parameter		Symbol	Conditions	Value Min	Typ	Max	Unit
CPU Interface 2	Read Address Setup	t_{AR}	[(5)MB89322A only]	0			ns
	Read Low	t_{RR}		160			ns
	Read Address Hold	t_{RA}		0			ns
	Write Address Setup	t_{AW}		0			ns
	Write Low	t_{WW}		190			ns
	Write Address Hold	t_{WA}		0			ns
	Data Delay	t_{RD}				120	ns
	Data Hold	t_{DF}		10			ns
	Data Setup	t_{DW}		60			ns
	Data Hold	t_{WD}		0			ns
	Access Inhibit	t_{DIS}		210			ns
IRQ	Interrupt Delay	t_{IRDF}	(6)			150	ns
	Interrupt Delay *2	t_{IRDR}				$1/2t_{clk}$ +150	ns

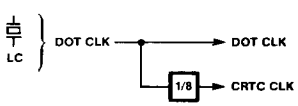
Note: *1. External vertical synchronous signal width t_{PWVS} = 1000 ns + t_{CLK} (TV sync mode)
t_{PWVSS} = 1000 ns + 3 t_{CLK} (Master slave mode)
*2. Rising delay time when light pen strobe input in non display time

Clock

A TTL-level input from DC to 4.5 MHz character clock should be used. An example of the clock circuit is shown below.

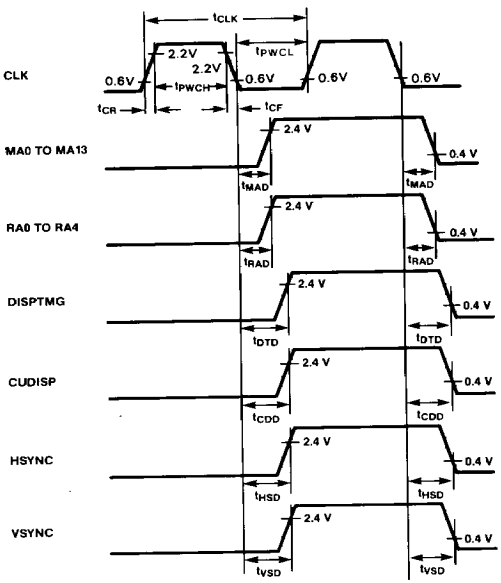


A circuit example for horizontal 8-dot character mode is as follows:

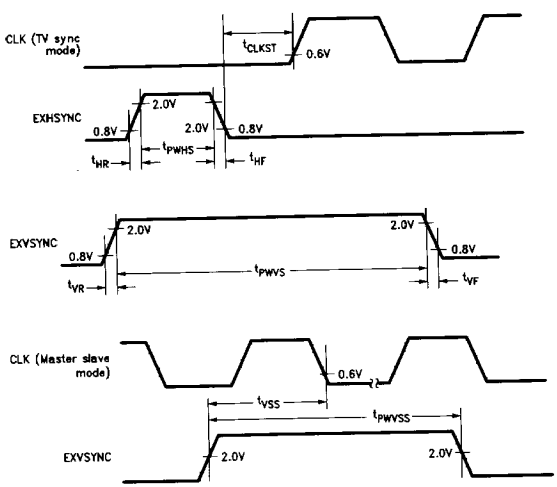


Timing Diagrams

(1) CRT Controller



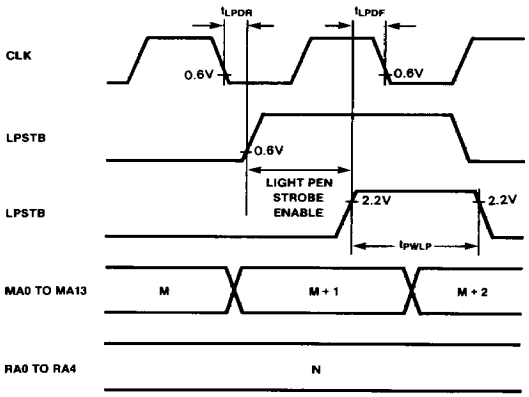
(2) External synchronization



4

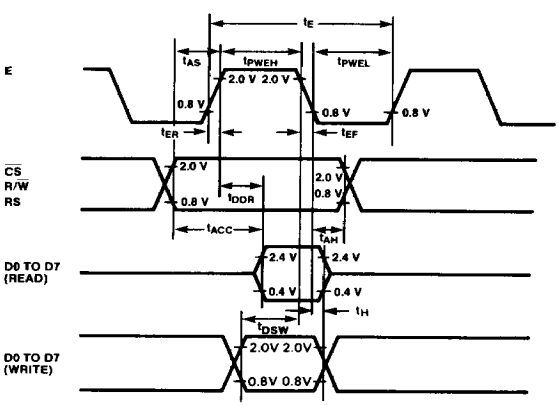
Timing Diagrams
(Continued)

(3) Light Pen



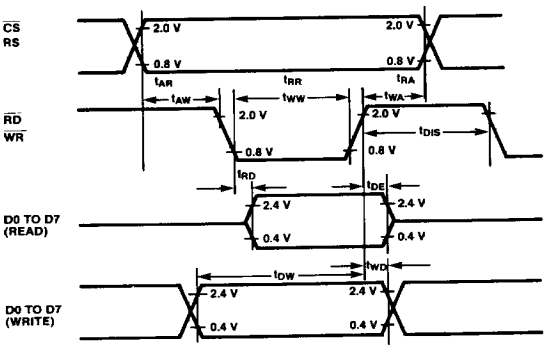
When the light pen strobe is enabled, LPSTB goes high, M+2 is loaded into the light pen register, N into the light pen raster register, and the display status bit is set.

(4) CPU Interface 1 (MB89321A only)

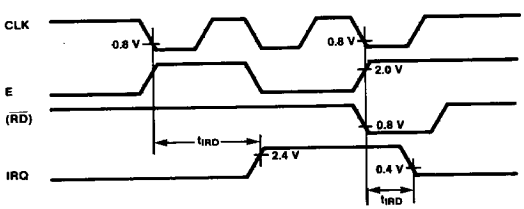


Timing Diagrams
(Continued)

(5) CPU Interface 2 (MB89322A only)

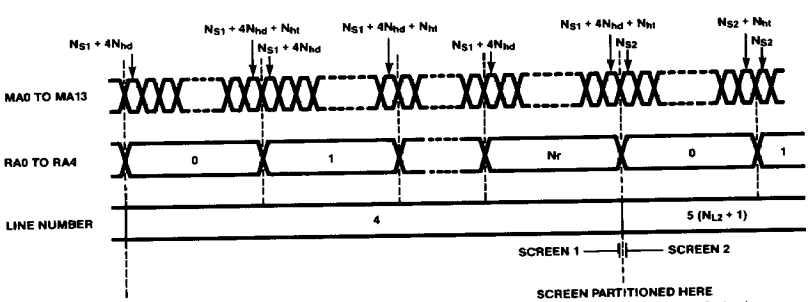


(6) IRQ Timing



Notes on Operation

(1) Screen Partition Timing



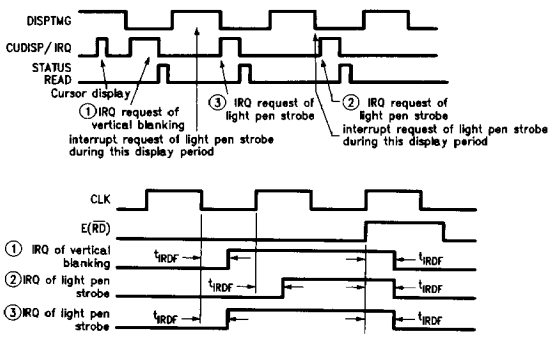
This example shows typical memory addresses and raster addresses of screens 1 and 2 during screen partitioning.

Nht: Total Number of Characters in Line (R0)
Nhd: Number of Characters Displayed in Line (R1)
Nr : Maximum Raster Address (R9)
Ns1: Start Address 1 (R12, R13)
NL2: Screen 2 Display Start Position (R18)
NS2: Start Address 2 (R19, R20)

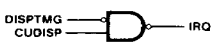
4

Notes on Operation
(Continued)

(2) Interrupt Signal Generator Timing

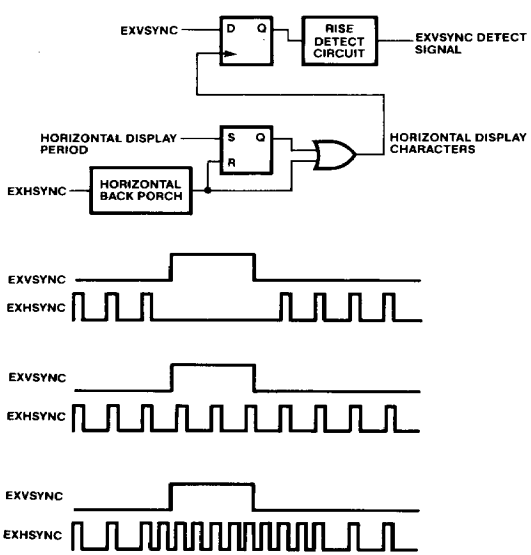


The interrupt signal is output to the CUDISP pin during display blanking. The interrupt signal can be generated as shown in the diagram below.



When the cursor is not enabled, the CUDISP pin functions as IRQ.

(3) TV Sync Timing



In TV sync mode, EXHSYNC is enabled when a pulse of 1,000 ns or more is applied. Also, during vertical blanking, EXVSYNC is enabled to sync the controller's internal horizontal display period signal. In order to use the TV sync function, a horizontal display period should be set. The basic circuit required to do this is shown to the left.

Note: Low (enabled) during the horizontal display period.

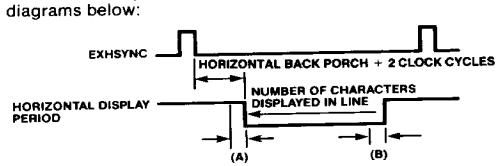
The TV sync function may not operate under the timing shown here at the immediate left.

The TV sync function is activated using the timing as shown here.

Notes on Operation
(Continued)

(4) Horizontal Display Period Setting (TV Sync Mode)

The horizontal display period is determined by the timing diagrams below:



(A) and (B) indicate points where EXVSYNC is detected.

EXVSYNC is normally detected at (B). However, when EXHSYNC is generated during the horizontal display period by an equivalent pulse, detection is at (A).

(A) and (B) require at least 1,000 ns + 1 clock cycle, during which period EXVSYNC must be maintained.

(5) Screen Partitioning

The display order of partitioned screens can be changed by programming the start position registers (R18, R21, and R24) for each partitioned screen, except screen 1, which is always displayed from line 0 on the screen. (See Figure A below.)

But, when the same values are programmed to the start position registers, the partitioned screens for those start position registers aren't displayed, even if those partitioned screens are enabled by P0 and P1 bits.

Figure A

Line No.	Display Screen	Example of Register Setting
0	Screen 1	Screen 3 Start Position (R21) ≤ Screen 2 Start Position (R18) ≤ Screen 4 Start Position (R24)
1		
2		
3	Screen 3	• Screen 2 Start Position Reg. (R18) = 5
4		• Screen 3 Start Position Reg. (R21) = 2
5		• Screen 4 Start Position Reg. (R24) = 8
6	Screen 2	
7		
8		
9	Screen 4	
10		
11		

4

Notes on Operation
(Continued)

(6) Raster Interpolation

At present, two versions of MB89321A/89322A are provided: One has the raster interpolation function, and another has no raster interpolation function. On MB89321A/89322A without the raster interpolation function, "0" must always be written to RI bit of the control/status register (R31).

Figure B

Line No.	Display Screen	Example of Register Setting
0	Screen 1	Screen 2 Start Position (R18) = Screen 3 Start Position (R21) ≤ Screen 4 Start Position (R24)
1		
2		
3		
4		• Screen 4 Start Position Reg. (R24) = 8
5		
6		
7		• Screens 2 and 3 aren't displayed because the start position registers for these screens have the same value. In the display areas for Screens 2 and 3, Screen 1, which is displayed above those screens, is displayed.
8		
9		
10	Screen 4	
11		

Package Dimensions
Dimensions in inches (millimeters)

40-Lead Plastic Dual In-Line Package (Case No.: DIP-40P-M01)