256 x 18 Video Color Palette

FEATURES

- RGB analog outputs, 6-bit DAC per channel with composite blank.
- Combines high speed Color Palette RAM and Triple Video DAC.
- Displays 256 colors simultaneously from a palette of 256K colors.
- Supports pixel rates up to 50 MHz.
- Direct replacement for INMOS G171 and G176.
- Up to 6-bit per pixel resolution.
- Directly drives singly or doubly terminated 75Ω transmission lines.
- Pixel word mask for single cycle color updates.
- Asynchronous microprocessor compatible interface.
- TTL compatible inputs, single 5V ± 10% power supply.
- Packaged in JEDEC standard 28 pin 600 mil DIP and 44 pin PLCC packages.

DESCRIPTION

The MOSEL MS176 is a high speed RAMDAC designed for video graphics applications. It combines a 256 x 18 color look-up table, triple 6-bit video digital to analog converters and an asynchronous bidirectional microprocessor interface into a single device.

The MS176 can display 256 colors selected from a total of 256K colors. The on-chip pixel word mask allows displayed colors to be changed in a single write cycle rather than by modifying the color look-up table. Each of the RED, GREEN and BLUE analog output signals can drive a single or doubly terminated 75Ω transmission line directly.

Intended for high-resolution graphics applications, the MOSEL MS176 is available with pixel rates ranging from 40 MHz to 50 MHz. It is a direct pin and function replacement for the Inmos G-171 and G-176, and is fully compatible with VGA industry standards. The MS176 is offered in a JEDEC standard 28-pin, 600 mil plastic DIP and 44 pin PLCC packages.

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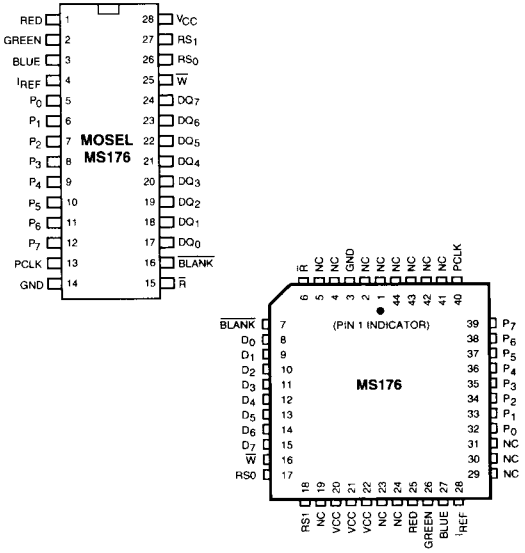
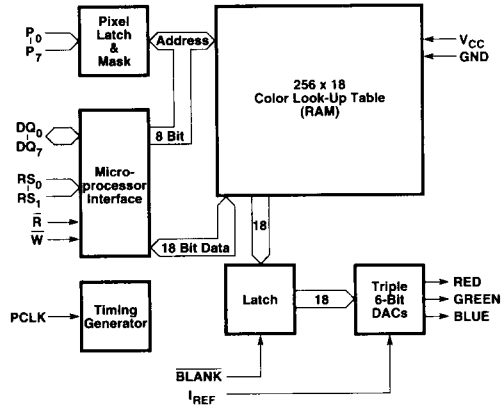
PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

ANALOG INTERFACE

RED, GREEN, BLUE Color Signal Outputs

These three signals are the outputs of the three 6 bit video DACs. These signals drive a singly or doubly terminated (75Ω) transmission line. Each DAC is composed of a number of current sources whose outputs are summed. The number of active current sources is controlled by the applied binary value. A compatible monitor or video amplifier can be directly driven by these color signals.

I_{REF} Reference Current

I_{REF} provides a reference for the internal video DACs. I_{REF} must be driven by an external current sink providing a regulated current. The reference current drawn from V_{CC} through the I_{REF} pin determines the current sourced by each of the DACs current sources.

PIXEL INTERACE

PCLK Pixel Clock Input

The Pixel Clock is a positive edge triggered signal. It is used to latch the pixel addresses and the blanking signal. This clock also controls the three-stage pipeline of the color palette and DAC to the outputs. Each Pixel Clock period corresponds to one pixel displayed on the monitor.

P_0–P_7 Pixel Address Inputs

These 8 inputs are latched on the rising edge of PCLK. The value of these 8 inputs are ANDed with the corresponding bits of the Pixel Mask Register. The resulting address is used to specify the desired RAM word in the color look-up table. This 18 bit wide color value is then output to the DACs.

$\overline{BLANK}$ Blanking Control Input

The blanking control input is active LOW, and is latched on the rising edge of PCLK. The $\overline{BLANK}$ signal is used for blanking the display during retrace. When $\overline{BLANK}$ is LOW the color value from the look-up table is ignored and the DAC outputs are forced to the blanking level. $\overline{BLANK}$ has the same pipeline delay as P_0–P_7.

DIGITAL INTERFACE

$\overline{R}$ Read Enable Input

The read enable input is active LOW. When active, output data will be present at the DQ pins. The values of the register select inputs are latched on the falling edge of $\overline{R}$ and are decoded to determine the source of the output data. When $\overline{R}$ is HIGH, the DQ pins will be in the high-impedance state.

$\overline{W}$ Write Enable Input

The write enable input is active LOW. When active, data present at the DQ pins will be written into the device. The values of the register select inputs are latched on the falling edge of $\overline{W}$ and are decoded to determine the destination of the write data.

RS_0–RS_1 Register Select Inputs

The value of these inputs specifies which of the internal registers is to be read or written. The values of these inputs are latched at the beginning of a read or write cycle. The cycle begins on the falling edge of either the $\overline{R}$ or $\overline{W}$ input.

DQ_0–DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data to the device internal registers. The Pixel Address Register and the Pixel Mask Register use all 8 bits, the Color Value Register uses only the lower six bits (DQ_0–DQ_5).

V_{CC} Positive Power Supply

GND Ground

TABLE 1. REGISTER SELECT TRUTH TABLE

RS_1	RS_0	REGISTER ASSIGNMENT
0	0	Pixel Address Register (RAM Write)
1	1	Pixel Address Register (RAM Read)
0	1	Color Value Register
1	0	Pixel Mask Register

FUNCTIONAL DESCRIPTION

The MOSEL MS176 is designed for use as the output stage of a raster scan video system. This high speed video color palette combines a 256 x 18 color look-up table, triple 6-bit video digital to analog converters and an asynchronous bidirectional microprocessor interface into a single compact package.

The MS176 consists of three distinct sections. The first section includes the pixel address, timing and $\overline{\text{BLANK}}$ information. The second section contains the color look-up table and the three video DACs, while the third section is the digital microprocessor interface.

Video Path

The pixel address inputs P_0–P_7 are latched on the rising edge of PCLK. The value of these 8 inputs are ANDed with the corresponding bits of the pixel mask register before being passed as an address to the color look-up table. The contents of the specified location are then transferred to the video DACs.

The $\overline{\text{BLANK}}$ signal is used to blank the display during retrace. The $\overline{\text{BLANK}}$ input is latched at the same time as P_0–P_7, and is delayed internally so that it arrives at the analog outputs synchronized with the pixel stream. When $\overline{\text{BLANK}}$ is LOW the color value from the look-up table is ignored and the video DAC outputs are forced to the blanking level.

Microprocessor Interface

The microprocessor interface is used to read to and write from the color look-up table as well as the pixel mask register. The microprocessor interface is internally synchronized so that operations may occur at any time without waiting for retrace. Table 1 shows the microprocessor interface registers and how they are addressed.

Writing to the Color Look-Up Table

In order to define a new color value, the desired address in the color look-up table must first be written to the Pixel Address Register (RAM write). The appropriate values are set on the register select pins (RS_0–RS_1). This is latched on the falling edge of $\overline{W}$. The desired address is set on pins DQ_0–DQ_7 and is loaded into the Pixel Address Register. Following this, the values for the red, green and blue intensities are then written into the Color Value Register. This is accomplished by three additional write cycles (with the Color Value Register selected by the register select inputs). The Color Value Register loads only the values on DQ_0–DQ_5.

After the blue value is loaded on the third write cycle, the contents of the Color Value Register are written to the selected address in the color look-up table, and the Pixel Address Register is automatically incremented. This allows color values to be defined for sequential locations with no need to rewrite the Pixel Address Register.

Reading from the Color Look-Up Table

To read a color value contained in the look-up table the desired address must first be written to the Pixel Address Register (RAM read). The appropriate values are set on the register select pins (RS_0–RS_1). This is latched on the falling edge of $\overline{W}$. The desired address is set on pins DQ_0–DQ_7 and is loaded into the Pixel Address Register. The contents of the specified location are written into the Color Value Register and the Pixel Address Register is automatically incremented.

The red, green and blue values are then read by a sequence of three read cycles (with the Color Value Register Selected by the register select inputs). The values are output on DQ_0–DQ_5. After the blue value is read on the third cycle, the contents of the location specified by the Pixel Address Register (which has already been incremented) are written into the Color Value Register. This allows color values to be read for sequential locations with no need to rewrite the Pixel Address Register.

Reading and Writing the Pixel Mask Register

The Pixel Mask Register is written to in a similar fashion as the Pixel Address Register. The appropriate values for selecting the Pixel Mask Register are set on the register select pins, the desired contents are placed on DQ_0–DQ_7, and a single write cycle is executed. The contents of the Pixel Mask Register may be read by placing the appropriate values on the register select pins and executing a single read cycle. The contents of the Pixel Mask Register can then be read on DQ_0–DQ_7.

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	VALUE	UNITS
V_{CC}	V_{CC} Supply Voltage	7.0	V
V_{TERM}	Voltage on All Other Pins	−1.0 to V_{CC} +0.5	V
t_{BIAS}	Temperature Under Bias	−40 to +85	°C
t_{STG}	Storage Temperature	−60 to +150	°C
I_{REF}	Reference Current	−15	mA
I_O	Analog Output Current (2)	45	mA
I_{OUT}	DC Digital Output Current (3)	25	mA
P_D	Power Dissipation	1	W

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Per output
3. One output at a time, maximum one second duration.

OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to 70°C	5V ± 10%

CAPACITANCE (1, 2)

SYMBOL	PARAMETER	CONDITIONS	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN}=0V	7	pF
C_{DQ}	Digital Input/Output Capacitance	V_{DQ}=0V $\overline{R}$=V_{IH}	7	pF
C_{OA}	Analog Output Capacitance	V_{OA}=0V $\overline{BLANK}$=V_{IL}	10	pF

1. This parameter is guaranteed and not tested.
2. T_A = 25°C, f = 1.0 MHz.

DC ELECTRICAL CHARACTERISTICS (over the operating range)

DIGITAL INTERFACE

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input LOW Voltage (2)(3)		−0.5	—	+0.8	V
V_{IH}	Guaranteed Input HIGH Voltage (2)		2.0	—	V_{CC}+0.5	V
I_{REF}	Reference Current		−7.0	−8.88	−10	mA
V_{REF}	Voltage I_{REF} Input (pin 4)		V_{CC}−3	—	V_{CC}	V
V_{OL}	Output LOW Voltage	V_{CC}=Min, I_{OL}=5mA	—	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC}=Min, I_{OH}=−5mA	2.4	—	—	V
I_{IN}	Input Leakage Current	V_{CC}=Max, V_{SS}≤V_{IN}≤V_{CC}	—	—	±10	µA
I_{OLK}	Output Leakage Current	V_{CC} = Max, V_{SS}≤V_{IN}≤V_{CC}, $\overline{R}$≥V_{IH}	—	—	±50	µA
I_{CC}	Operating Power Supply Current	V_{CC}=Min, I_O=Max, I_{DQ}=0mA, F=F_{MAX} (4)	—	120	180	mA

ANALOG INTERFACE

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_O (max)	Analog Output Voltage	I_O≤10mA	—	—	1.5	V
I_O (max)	Analog Output Current	V_O≤1V	21	—	—	mA
	Full Scale Error	(5, 6)	—	—	±5	%
	DAC to DAC Correlation	(6, 7, 11)	—	—	±2	%
	Integral Non-Linearity	(8, 11)	±0.5	—	—	LSB
	Full Scale Settling Time	MS176-50 (9, 10, 11)	—	—	20	ns
		MS176-40 (9, 10, 11)	—	—	28	ns
	Rise Time (10% to 90%)	(10, 11)	—	—	6	ns
	Glitch Energy	(10, 11)	—	—	200	pV_{SEC}

NOTES:

1. Typical characteristics are at V_{CC} = 5.0V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (min) = −1.0V for pulse width < 10ns.
4. F_{MAX} = $1/t_{CHCH}$
5. Full scale error is measured from the value derived from the design equation.
6. R_L = 37.5Ω, I_{REF} = −8.88 mA.
7. About the mid-point of the distribution of the three DACs measured at full scale deflection.
8. Measured from least squares best fit line. Monotonicity is guaranteed.
9. Measured from a 2% change in the output voltage until settling to within 2% of the final value.
10. I_{REF} = −8.88 mA, R_L = 37.5Ω, C_L = 30pF as shown in Figure 2a.
11. This parameter is sampled but not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times (10% to 90%)	3ns
Digital Input Timing Reference Level	1.5V
Digital Output Timing Reference Level	0.8V and 2.4V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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AC TEST LOADS AND WAVEFORMS

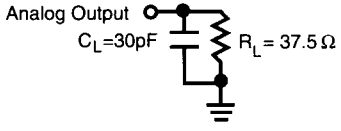


Figure 1a

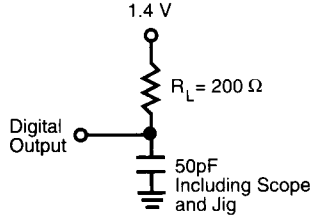


Figure 1b

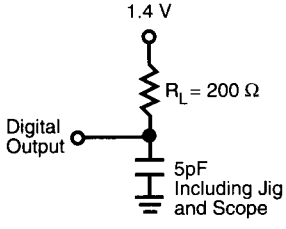


Figure 1c

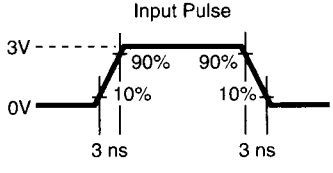


Figure 2

AC ELECTRICAL CHARACTERISTICS (over the operating range)

VIDEO OPERATION

NO.	PARAMETER NAME	PARAMETER	MS176-50 MIN.	MS176-50 MAX.	MS176-40 MIN.	MS176-40 MAX.	UNITS
1	t_{CHCH}	PCLK Period	20	—	25	—	ns
2	t_{CLCH}	PCLK Width LOW	6	—	9	—	ns
3	t_{CHCL}	PCLK Width HIGH	6	—	7	—	ns
4	Δt_{CHCH}	PCLK Jitter (1)	—	±2.5	—	±2.5	%
5	t_{PVCH}	Pixel Word Setup Time (2)	4	—	4	—	ns
6	t_{CHPX}	Pixel Word Hold Time (2)	4	—	4	—	ns
7	t_{BVCH}	$\overline{BLANK}$ Setup Time	4	—	4	—	ns
8	t_{CHBX}	$\overline{BLANK}$ Hold Time	4	—	4	—	ns
9	t_{CHAV}	PCLK to DAC Output Valid (3)	5	30	5	30	ns
10	Δt_{CHAV}	DAC to DAC Skew (4)	—	2	—	2	ns

READ CYCLE

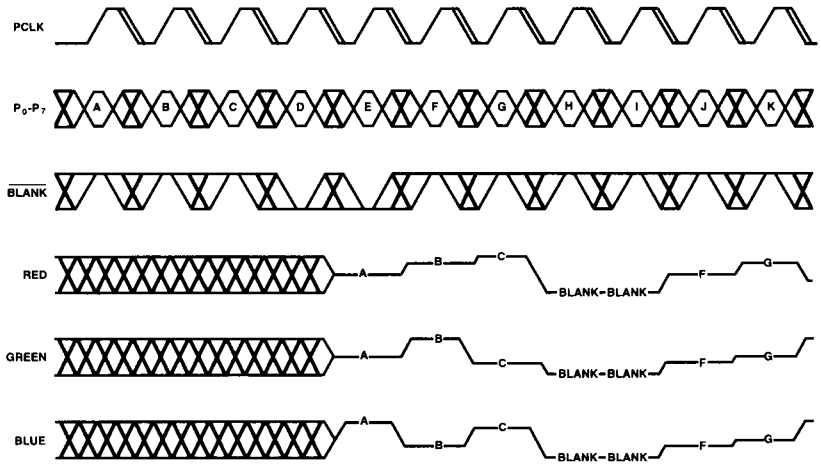
NO.	PARAMETER NAME	PARAMETER	MS176-50 MIN.	MS176-50 MAX.	MS176-40 MIN.	MS176-40 MAX.	UNITS
11	t_{RLRH}	Read Pulse Width	50	—	50	—	ns
12	t_{SVRL}	Register Select Setup Time	10	—	15	—	ns
13	t_{RLSX}	Register Select Hold Time	10	—	15	—	ns
14	t_{RLQX}	Read Enable to Output in Low Z	5	—	5	—	ns
15	t_{RLQV}	Read Enable to Output Valid	—	40	—	40	ns
16	t_{RHQX}	Output Hold Time	5	—	5	—	ns
17	t_{RHQZ}	Read Disable to Output in High Z (5)	—	20	—	20	ns
18	t_{RHRL1}	Successive Read Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
19	t_{RHWL1}	Read Write Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
20	t_{RHRL2}	Read After Color Read Interval (6)	$6(t_{CHCH})$	—	$6(t_{CHCH})$	—	ns
21	t_{RHWL2}	Write After Color Read Interval (6)	$6(t_{CHCH})$	—	$6(t_{CHCH})$	—	ns

WRITE CYCLE

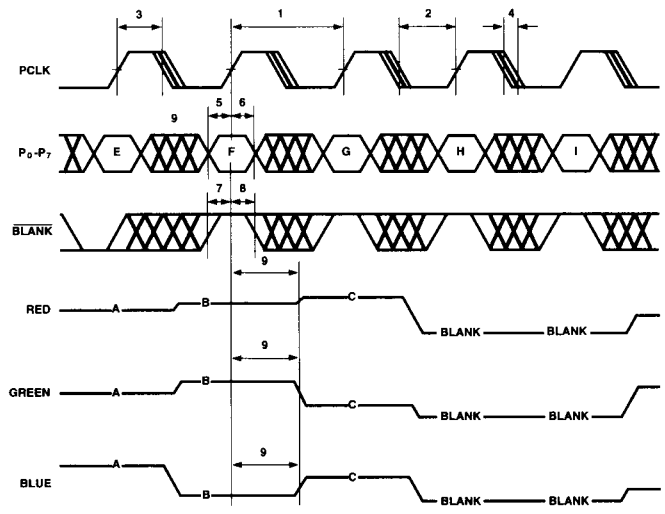
NO.	PARAMETER NAME	PARAMETER	MS176-50 MIN.	MS176-50 MAX.	MS176-40 MIN.	MS176-40 MAX.	UNITS
22	t_{WLWH}	Write Pulse Width	50	—	50	—	ns
23	t_{SVWL}	Register Select Setup Time	10	—	15	—	ns
24	t_{WLSX}	Register Select Hold Time	10	—	15	—	ns
25	t_{DVWH}	Data Setup to $\overline{W}$ High	10	—	15	—	ns
26	t_{WHDX}	Data Hold From $\overline{W}$ High	5	—	5	—	ns
27	t_{WHWL1}	Successive Write Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
28	t_{WHRL1}	Write to Read Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
29	t_{WHWL2}	Write After Color Write Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
30	t_{WHRL2}	Read After Color Write Interval (6)	$3(t_{CHCH})$	—	$3(t_{CHCH})$	—	ns
31	t_{WHRL3}	Read After Read Address Write (6)	$6(t_{CHCH})$	—	$6(t_{CHCH})$	—	ns

NOTES:
1. This parameter is the allowed pixel clock frequency variation. It does not permit the pixel clock to vary outside the minimum value for PCLK period (t_{CHCH}).
2. Pixel address inputs must be set to a valid logic level with the appropriate setup and hold time at each rising edge of PCLK (this requirement includes the blanking period).
3. Valid DAC output is measured at the 50% point between successive DAC values.
4. Between different analog outputs on the same device.
5. Transition is measured ±200mV from steady state output voltage with C_L = 5pF as shown in Figure 1C. This parameter is guaranteed and not 100% tested.
6. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

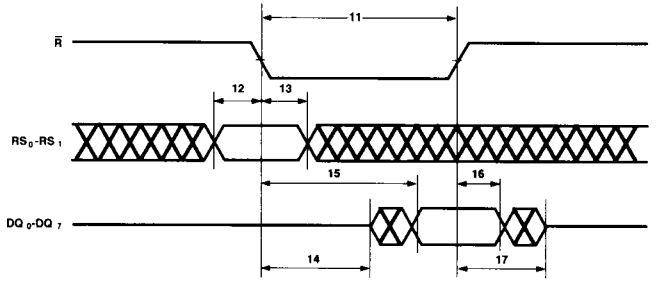
SYSTEM TIMING DIAGRAM



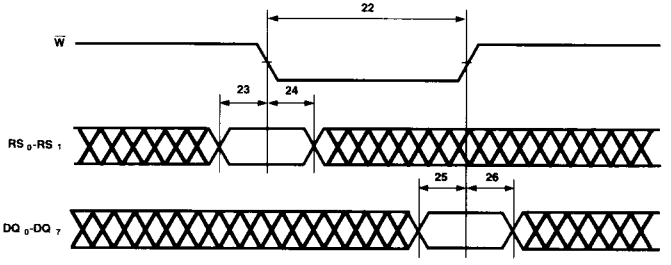
TIMING DIAGRAM DETAILING TIMING SPECIFICATIONS



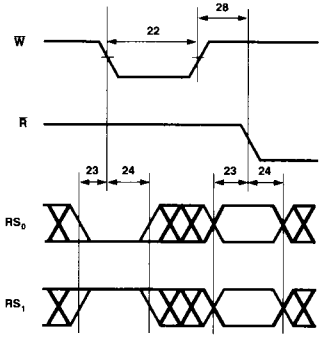
BASIC READ CYCLE TIMING DIAGRAM



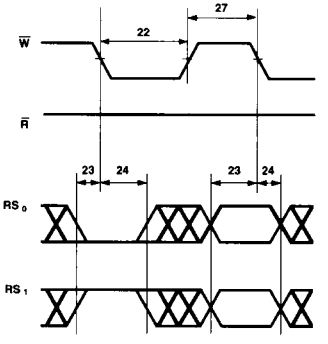
BASIC WRITE CYCLE TIMING DIAGRAM



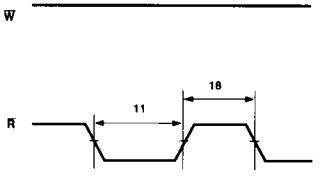
WRITE TO PIXEL MASK REGISTER FOLLOWED BY READ



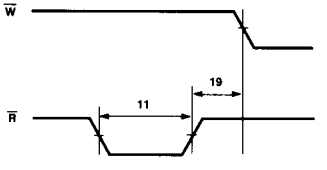
WRITE TO PIXEL MASK REGISTER FOLLOWED BY WRITE



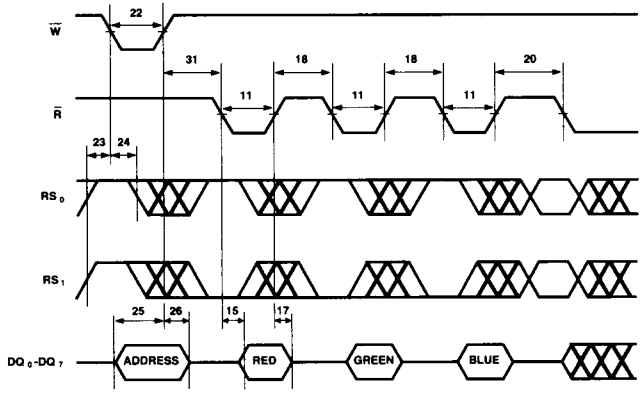
READ FROM PIXEL MASK OR PIXEL ADDRESS REGISTER (READ OR WRITE MODE) FOLLOWED BY READ



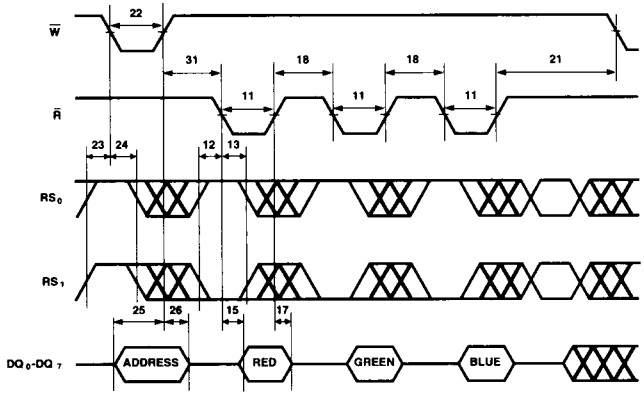
READ FROM PIXEL MASK OR PIXEL ADDRESS REGISTER (READ OR WRITE MODE) FOLLOWED BY WRITE



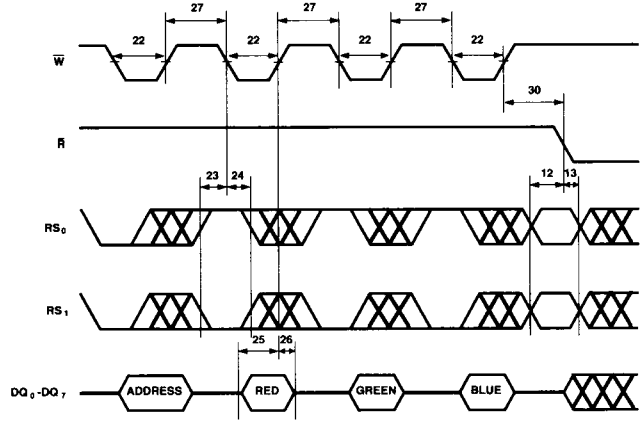
COLOR VALUE READ FOLLOWED BY ANY READ



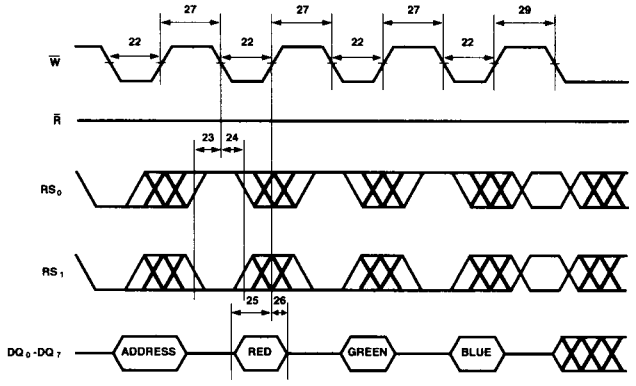
COLOR VALUE READ FOLLOWED BY ANY WRITE



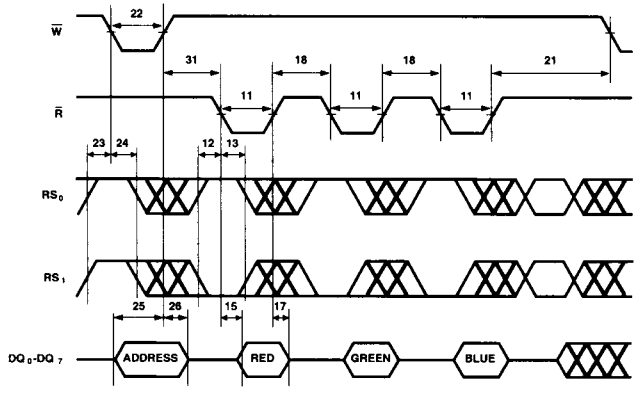
COLOR VALUE WRITE FOLLOWED BY ANY READ



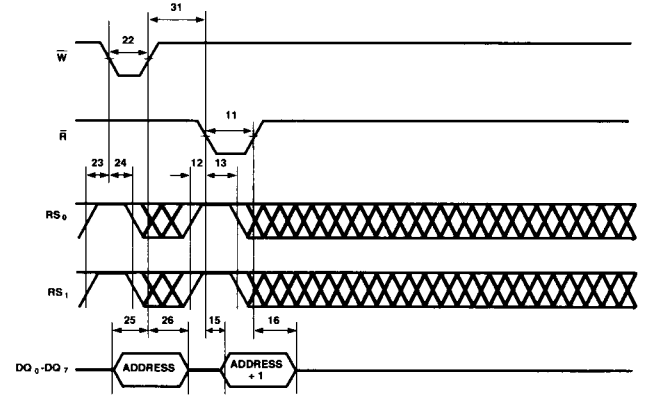
COLOR VALUE WRITE FOLLOWED BY ANY WRITE



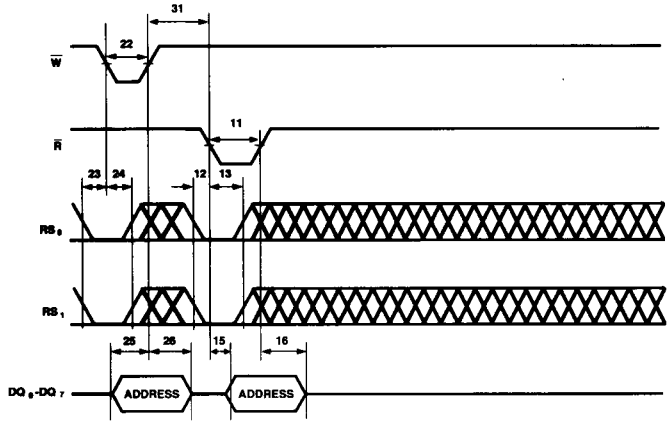
READ COLOR VALUE THEN READ PIXEL ADDRESS REGISTER (RAM READ)



WRITE AND READ BACK PIXEL ADDRESS REGISTER (READ MODE)



WRITE AND READ BACK PIXEL ADDRESS REGISTER (RAM WRITE)



SYSTEM APPLICATIONS NOTES

Current Reference Decoupling

The DACs in the MOSEL MS176 are composed of switched current sources which are based around a current mirror. The total current output of each DAC is determined by the number of active current sources and the reference current I_{REF}. I_{REF} develops a voltage reference relative to V_{CC} for the current mirror. Voltage variation in V_{CC} not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these V_{CC} variations, it is recommended that a high frequency capacitor in parallel with a larger capacitor be used to couple the I_{REF} input to V_{CC}. This will enable the current source to track both high and low frequency variations of V_{CC}. (A coupling capacitor in the range of 47 to 100 µF is appropriate for most applications.) If the variations of V_{CC} are minor, or are controlled by the reference circuit, then a coupling capacitor should not be used.

Power Supply

The MOSEL MS176 is a high speed device. During operation it may draw large transient currents from the power supply. To ensure proper operation good high frequency board layout techniques and power supply distribution should be used.

SPEED	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
40 MHZ	MS176-40JC	J44-2	0°C to + 70°C
40 MHZ	MS176-40PC	P28-1	0°C to + 70°C
50 MHZ	MS176-50JC	J44-2	0°C to + 70°C
50 MHZ	MS176-50PC	P28-1	0°C to + 70°C