
STM32
CubeMX

1. Description

1.1. Project

Project Name	stm32-ecu
Board Name	STM32MP157D-DK1
Generated with:	STM32CubeMX 6.3.0
Date	12/05/2021

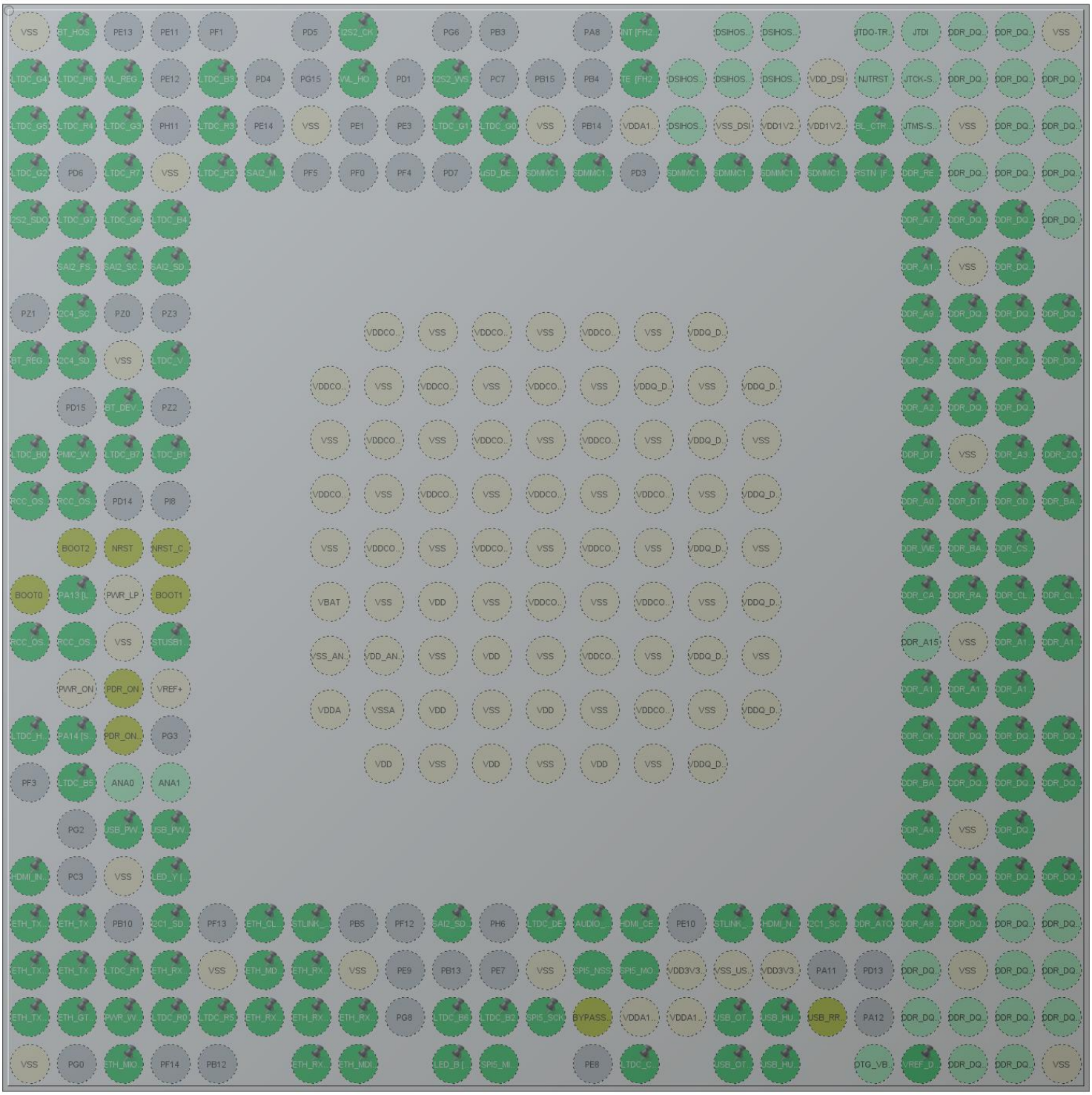
1.2. MCU

MCU Series	STM32MP1
MCU Line	STM32MP157
MCU name	STM32MP157DACx
MCU Package	TFBGA361
MCU Pin number	361

1.3. Core(s) information

Core(s)	ARM Cortex-A7 ARM Cortex-M4

2. Pinout Configuration



TFBGA361 (Top view)

3. Pins Configuration

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VSS	Power		
A2	PH5 *	I/O	GPIO_Input	BT_HOST_WAKE [LBEE5KL1DX_BT_HOST_WAKE]
A8	PA9	I/O	I2S2_CK	
A14	PF2 *	I/O	GPIO_Input	INT [FH26W-25S_INT]
A23	VSS	Power		
B1	PH15	I/O	LTDC_G4	
B2	PH12	I/O	LTDC_R6	
B3	PH4 *	I/O	GPIO_Output	WL_REG_ON [LBEE5KL1DX_WL_REG_ON]
B5	PD10	I/O	LTDC_B3	
B8	PD0 *	I/O	GPIO_Input	WL_HOST_WAKE [LBEE5KL1DX_WL_HOST_WAKE]
B10	PB9	I/O	I2S2_WS	
B14	PC6 *	I/O	GPIO_Output	TE [FH26W-25S_TE]
B18	VDD_DSI	Power		
C1	PI0	I/O	LTDC_G5	
C2	PH10	I/O	LTDC_R4	
C3	PH14	I/O	LTDC_G3	
C5	PH9	I/O	LTDC_R3	
C7	VSS	Power		
C10	PE6	I/O	LTDC_G1	
C11	PE5	I/O	LTDC_G0	
C12	VSS	Power		
C14	VDDA1V8_DSI	Power		
C16	VSS_DSI	Power		
C17	VDD1V2_DSI_PHY	Power		
C18	VDD1V2_DSI_REG	Power		
C19	PA15 *	I/O	GPIO_Output	BL_CTRL [STLD40DPUR_EN]
C21	VSS	Power		
D1	PH13	I/O	LTDC_G2	
D3	PE15	I/O	LTDC_R7	
D4	VSS	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
D5	PH8	I/O	LTDC_R2	
D6	PE0	I/O	SAI2_MCLK_A	
D11	PB7 *	I/O	GPIO_Input	uSD_DETECT [PJS008-2003-1]
D12	PD2	I/O	SDMMC1_CMD	SDMMC1_CMD [PJS008-2003-1]
D13	PC12	I/O	SDMMC1_CK	SDMMC1_CK [PJS008-2003-1]
D15	PC10	I/O	SDMMC1_D2	SDMMC1_D2 [PJS008-2003-1]
D16	PC11	I/O	SDMMC1_D3	SDMMC1_D3 [PJS008-2003-1]
D17	PC9	I/O	SDMMC1_D1	SDMMC1_D1 [PJS008-2003-1]
D18	PC8	I/O	SDMMC1_D0	SDMMC1_D0 [PJS008-2003-1]
D19	PE4 *	I/O	GPIO_Output	RSTN [FH26W-25S_RSTN]
D20	DDR_RESETN	MonoIO	DDR_RESETN	DDR_RESETN [MT41K256M16TW_RESET#]
E1	PI3	I/O	I2S2_SDO	
E2	PI2	I/O	LTDC_G7	
E3	PI1	I/O	LTDC_G6	
E4	PI4	I/O	LTDC_B4	
E20	DDR_A7	MonoIO	DDR_A7	DDR_A7 [MT41K256M16TW_A7]
E21	DDR_DQ3	MonoIO	DDR_DQ3	DDR_DQ3 [MT41K256M16TW_DQU3]
E22	DDR_DQ0	MonoIO	DDR_DQ0	DDR_DQ0 [MT41K256M16TW_DQU5]
F2	PI7	I/O	SAI2_FS_A	
F3	PI5	I/O	SAI2_SCK_A	
F4	PI6	I/O	SAI2_SD_A	
F20	DDR_A13	MonoIO	DDR_A13	DDR_A13 [MT41K256M16TW_A13]
F21	VSS	Power		
F22	DDR_DQ1	MonoIO	DDR_DQ1	DDR_DQ1 [MT41K256M16TW_DQU1]
G2	PZ4	I/O	I2C4_SCL	I2C4_SCL [STPMU1A_SCL]
G20	DDR_A9	MonoIO	DDR_A9	DDR_A9 [MT41K256M16TW_A9]

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
G21	DDR_DQ7	MonoIO	DDR_DQ7	DDR_DQ7 [MT41K256M16TW_DQU7]
G22	DDR_DQS0P	MonoIO	DDR_DQS0P	DDR_DQS0_P [MT41K256M16TW_DQSU]
G23	DDR_DQS0N	MonoIO	DDR_DQS0N	DDR_DQS0_N [MT41K256M16TW_DQSU#]
H1	PZ6 *	I/O	GPIO_Output	BT_REG_ON [LBEE5KL1DX_BT_REG_ON]
H2	PZ5	I/O	I2C4_SDA	I2C4_SDA [STPMU1A_SDA]
H3	VSS	Power		
H4	PI9	I/O	LTDC_VSYNC	
H20	DDR_A5	MonoIO	DDR_A5	DDR_A5 [MT41K256M16TW_A5]
H21	DDR_DQ2	MonoIO	DDR_DQ2	DDR_DQ2 [MT41K256M16TW_DQU4]
H22	DDR_DQ6	MonoIO	DDR_DQ6	DDR_DQ6 [MT41K256M16TW_DQU0]
H23	DDR_DQM0	MonoIO	DDR_DQM0	DDR_DQM0 [MT41K256M16TW_DMU]
J3	PZ7 *	I/O	GPIO_Output	BT_DEV_WAKE [LBEE5KL1DX_BT_DEV_WAKE]
J20	DDR_A2	MonoIO	DDR_A2	DDR_A2 [MT41K256M16TW_A2]
J21	DDR_DQ4	MonoIO	DDR_DQ4	DDR_DQ4 [MT41K256M16TW_DQU6]
J22	DDR_DQ5	MonoIO	DDR_DQ5	DDR_DQ5 [MT41K256M16TW_DQU2]
K1	PD9	I/O	LTDC_B0	
K2	PC13 *	I/O	GPIO_Output	PMIC_WAKEUP [STPMU1A_WAKEUP]
K3	PD8	I/O	LTDC_B7	
K4	PG12	I/O	LTDC_B1	
K20	DDR_DTO0	MonoIO	DDR_DTO0	DDR_DTO0
K21	VSS	Power		
K22	DDR_A3	MonoIO	DDR_A3	DDR_A3 [MT41K256M16TW_A3]
K23	DDR_ZQ	MonoIO	DDR_ZQ	DDR_ZQ
L1	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
L2	PC14-OSC32_IN	I/O	RCC_OSC32_IN	

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
L20	DDR_A0	MonoIO	DDR_A0	DDR_A0 [MT41K256M16TW_A0]
L21	DDR_DTO1	MonoIO	DDR_DTO1	DDR_DTO1
L22	DDR_ODT	MonoIO	DDR_ODT	DDR_ODT [MT41K256M16TW_ODT]
L23	DDR_BA0	MonoIO	DDR_BA0	DDR_BA0 [MT41K256M16TW_BA0]
M2	BOOT2	Boot		
M3	NRST	Reset		
M4	NRST_CORE	Reset		
M20	DDR_WEN	MonoIO	DDR_WEN	DDR_WEN_P [MT41K256M16TW_WE#]
M21	DDR_BA2	MonoIO	DDR_BA2	DDR_BA2 [MT41K256M16TW_BA2]
M22	DDR_CSN	MonoIO	DDR_CSN	DDR_CSN [MT41K256M16TW_CS#]
N1	BOOT0	Boot		
N2	PA13 *	I/O	GPIO_Output	PA13 [LD6_RED]
N3	PWR_LP	Power		
N4	BOOT1	Boot		
N20	DDR_CASN	MonoIO	DDR_CASN	DDR_CASN [MT41K256M16TW_CAS#]
N21	DDR_RASN	MonoIO	DDR_RASN	DDR_RASN [MT41K256M16TW_RAS#]
N22	DDR_CLKP	MonoIO	DDR_CLKP	DDR_CLK_P [MT41K256M16TW_CK]
N23	DDR_CLKN	MonoIO	DDR_CLKN	DDR_CLK_N [MT41K256M16TW_CK#]
P1	PH0-OSC_IN	I/O	RCC_OSC_IN	
P2	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
P3	VSS	Power		
P4	PI11 *	I/O	GPIO_Input	STUSB1600_IRQOUTn [STUSB1600_ALERT#]
P21	VSS	Power		
P22	DDR_A1	MonoIO	DDR_A1	DDR_A1 [MT41K256M16TW_A1]
P23	DDR_A12	MonoIO	DDR_A12	DDR_A12 [MT41K256M16TW_A12]
R2	PWR_ON	Power		
R3	PDR_ON	MonoIO		
R4	VREF+	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
R20	DDR_A11	MonoIO	DDR_A11	DDR_A11 [MT41K256M16TW_A11]
R21	DDR_A14	MonoIO	DDR_A14	DDR_A14 [MT41K256M16TW_A14]
R22	DDR_A10	MonoIO	DDR_A10	DDR_A10 [MT41K256M16TW_A10]
T1	PI10	I/O	LTDC_HSYNC	
T2	PA14 *	I/O	GPIO_Input	PA14 [SW-PUSH-TS-02H-Blue]
T3	PDR_ON_CORE	MonoIO		
T20	DDR_CKE	MonoIO	DDR_CKE	DDR_CKE [MT41K256M16TW_CKE]
T21	DDR_DQ8	MonoIO	DDR_DQ8	DDR_DQ8 [MT41K256M16TW_DQL2]
T22	DDR_DQ10	MonoIO	DDR_DQ10	DDR_DQ10 [MT41K256M16TW_DQL6]
T23	DDR_DQ13	MonoIO	DDR_DQ13	DDR_DQ13 [MT41K256M16TW_DQL4]
U2	PA3	I/O	LTDC_B5	
U20	DDR_BA1	MonoIO	DDR_BA1	DDR_BA1 [MT41K256M16TW_BA1]
U21	DDR_DQ9	MonoIO	DDR_DQ9	DDR_DQ9 [MT41K256M16TW_DQL0]
U22	DDR_DQS1P	MonoIO	DDR_DQS1P	DDR_DQS1_P [MT41K256M16TW_DQSL]
U23	DDR_DQS1N	MonoIO	DDR_DQS1N	DDR_DQS1_N [MT41K256M16TW_DQSL#]
V3	PA5	I/O	ADC1_INP19, ADC2_INP19	USB_PWR_CC2[317JD24B ZTF3K3C3_CC2]
V4	PA4	I/O	ADC1_INP18, ADC2_INP18	USB_PWR_CC1[317JD24B ZTF3K3C3_CC1]
V20	DDR_A4	MonoIO	DDR_A4	DDR_A4 [MT41K256M16TW_A4]
V21	VSS	Power		
V22	DDR_DQM1	MonoIO	DDR_DQM1	DDR_DQM1 [MT41K256M16TW_DML]
W1	PG1 *	I/O	GPIO_Input	HDMI_INT [SiI9022ACNU_INT]
W3	VSS	Power		
W4	PH7 *	I/O	GPIO_Output	LED_Y [LD7_ORANGE]
W20	DDR_A6	MonoIO	DDR_A6	DDR_A6 [MT41K256M16TW_A6]

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
W21	DDR_DQ11	MonoIO	DDR_DQ11	DDR_DQ11 [MT41K256M16TW_DQL1]
W22	DDR_DQ14	MonoIO	DDR_DQ14	DDR_DQ14 [MT41K256M16TW_DQL7]
W23	DDR_DQ12	MonoIO	DDR_DQ12	DDR_DQ12 [MT41K256M16TW_DQL5]
Y1	PE2	I/O	ETH1_TXD3	ETH_TXD3 [RTL8211F_TXD3]
Y2	PC2	I/O	ETH1_TXD2	ETH_TXD2 [RTL8211F_TXD2]
Y4	PF15	I/O	I2C1_SDA	I2C1_SDA [CS42L51-CNZ_SDA]
Y6	PG5	I/O	ETH1_CLK125	ETH_CLK125 [RTL8211F_CLKOUT]
Y7	PG11	I/O	UART4_TX	STLINK_RX [STM32F103CBT6_PA3]
Y10	PF11	I/O	SAI2_SD_B	
Y12	PF10	I/O	LTDC_DE	
Y13	PG9 *	I/O	GPIO_Output	AUDIO_RST [CS42L51-CNZ_RESET]
Y14	PB6	I/O	CEC	HDMI_CEC [Sil9022ACNU_CEC_D]
Y16	PB2	I/O	UART4_RX	STLINK_TX [STM32F103CBT6_PA2]
Y17	PA10 *	I/O	GPIO_Output	HDMI_NRST [Sil9022ACNU_RESET#]
Y18	PD12	I/O	I2C1_SCL	I2C1_SCL [CS42L51-CNZ_SCL]
Y19	DDR_ATO	MonoIO	DDR_ATO	DDR_ATO
Y20	DDR_A8	MonoIO	DDR_A8	DDR_A8 [MT41K256M16TW_A8]
Y21	DDR_DQ15	MonoIO	DDR_DQ15	DDR_DQ15 [MT41K256M16TW_DQL3]
AA1	PG14	I/O	ETH1_TXD1	ETH_TXD1 [RTL8211F_TXD1]
AA2	PG13	I/O	ETH1_TXD0	ETH_TXD0 [RTL8211F_TXD0]
AA3	PH3	I/O	LTDC_R1	
AA4	PA1	I/O	ETH1_RX_CLK	ETH_RX_CLK [RTL8211F_RXCLK_PHYAD1]
AA5	VSS	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
AA6	PC1	I/O	ETH1_MDC	ETH_MDC [RTL8211F_MDC]
AA7	PB1	I/O	ETH1_RXD3	ETH_RXD3 [RTL8211F_RXD3_PHYAD0]
AA8	VSS	Power		
AA12	VSS	Power		
AA13	PF6	I/O	SPI5_NSS	
AA14	PF9	I/O	SPI5_MOSI	
AA15	VDD3V3_USBHS	Power		
AA16	VSS_USBHS	Power		
AA17	VDD3V3_USBFS	Power		
AA21	VSS	Power		
AB1	PB11	I/O	ETH1_TX_CTL	ETH_TX_EN [RTL8211F_TXCTL]
AB2	PG4	I/O	ETH1_GTX_CLK	ETH_GTX_CLK [RTL8211F_TXCLK]
AB3	PA0	I/O	PWR_WKUP1	
AB4	PH2	I/O	LTDC_R0	
AB5	PC0	I/O	LTDC_R5	
AB6	PB0	I/O	ETH1_RXD2	ETH_RXD2 [RTL8211F_RXD2_PLLOFF]
AB7	PC5	I/O	ETH1_RXD1	ETH_RXD1 [RTL8211F_RXD1_TXDLY]
AB8	PA7	I/O	ETH1_RX_CTL	ETH_RX_DV [RTL8211F_RXCTL_PHYAD2]
AB10	PB8	I/O	LTDC_B6	
AB11	PG10	I/O	LTDC_B2	
AB12	PF7	I/O	SPI5_SCK	
AB13	BYPASS_REG1V8	MonoIO		
AB14	VDDA1V8_REG	Power		
AB15	VDDA1V1_REG	Power		
AB16	USB_DM2	MonoIO	USB_OTG_HS_DM	
AB17	USB_DM1	MonoIO	USBH_HS1_DM	USB_HUB_N [USB2514B_USB_UP_DM]
AB18	USB_RREF	MonoIO		
AC1	VSS	Power		
AC3	PA2	I/O	ETH1_MDIO	ETH_MIO [RTL8211F_MIO]
AC7	PC4	I/O	ETH1_RXD0	ETH_RXD0 [RTL8211F_RXD0_RXDLY]

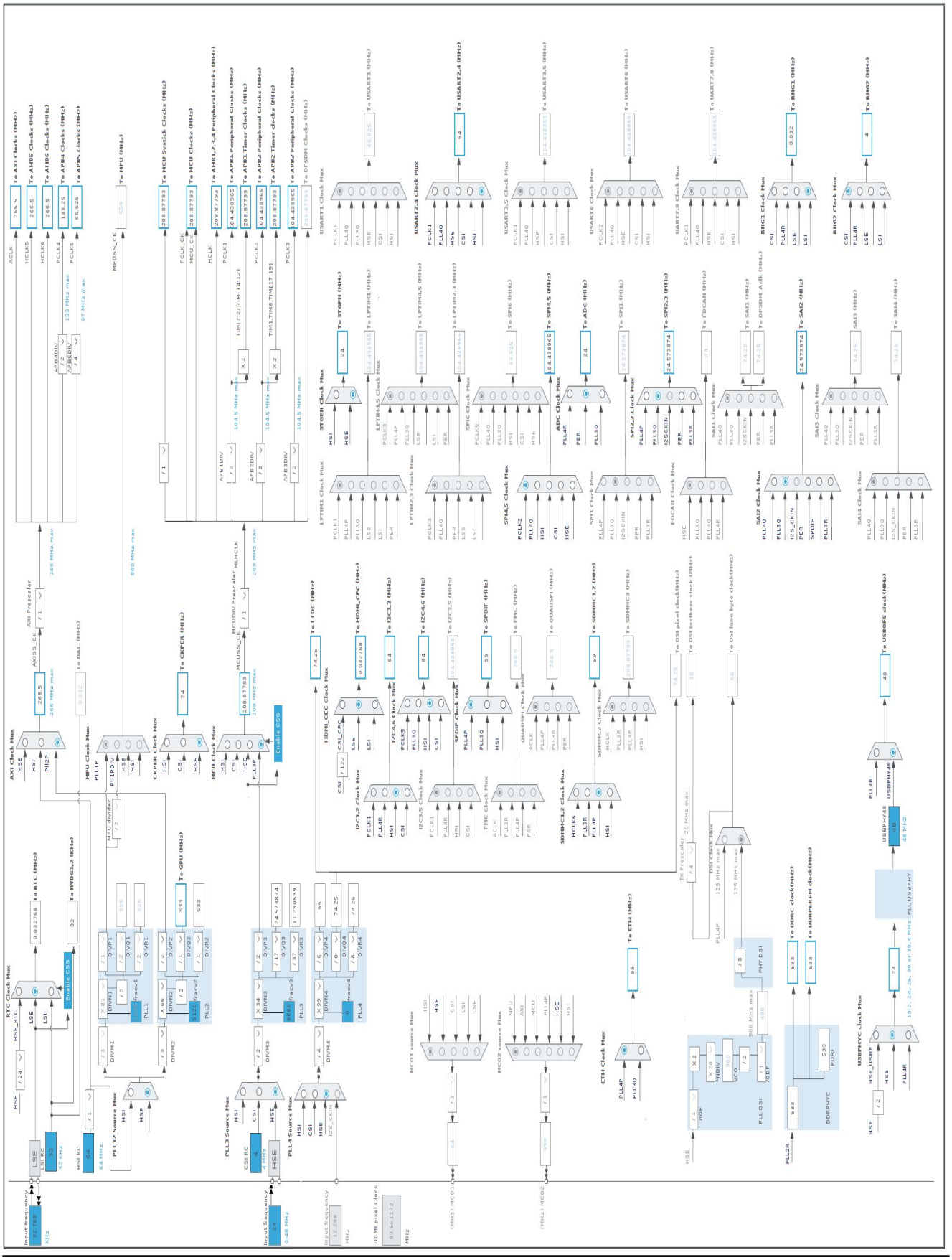
Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
AC8	PA6 *	I/O	GPIO_Input	ETH_MDINT [RTL8211F_INT]
AC10	PD11 *	I/O	GPIO_Output	LED_B [LD8_BLUE]
AC11	PF8	I/O	SPI5_MISO	
AC14	PG7	I/O	LTDC_CLK	
AC16	USB_DP2	MonoIO	USB_OTG_HS_DP	
AC17	USB_DP1	MonoIO	USBH_HS1_DP	USB_HUB_P [USB2514B_USB_UP_DP]
AC20	DDR_VREF	MonoIO	DDR_VREF	VREF_DDR
AC23	VSS	Power		
1A2	VDDCORE	Power		
1A3	VSS	Power		
1A4	VDDCORE	Power		
1A5	VSS	Power		
1A6	VDDCORE	Power		
1A7	VSS	Power		
1A8	VDDQ_DDR	Power		
1B1	VDDCORE	Power		
1B2	VSS	Power		
1B3	VDDCORE	Power		
1B4	VSS	Power		
1B5	VDDCORE	Power		
1B6	VSS	Power		
1B7	VDDQ_DDR	Power		
1B8	VSS	Power		
1B9	VDDQ_DDR	Power		
1C1	VSS	Power		
1C2	VDDCORE	Power		
1C3	VSS	Power		
1C4	VDDCORE	Power		
1C5	VSS	Power		
1C6	VDDCORE	Power		
1C7	VSS	Power		
1C8	VDDQ_DDR	Power		
1C9	VSS	Power		
1D1	VDDCORE	Power		
1D2	VSS	Power		
1D3	VDDCORE	Power		
1D4	VSS	Power		
1D5	VDDCORE	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1D6	VSS	Power		
1D7	VDDCORE	Power		
1D8	VSS	Power		
1D9	VDDQ_DDR	Power		
1E1	VSS	Power		
1E2	VDDCORE	Power		
1E3	VSS	Power		
1E4	VDDCORE	Power		
1E5	VSS	Power		
1E6	VDDCORE	Power		
1E7	VSS	Power		
1E8	VDDQ_DDR	Power		
1E9	VSS	Power		
1F1	VBAT	Power		
1F2	VSS	Power		
1F3	VDD	Power		
1F4	VSS	Power		
1F5	VDDCORE	Power		
1F6	VSS	Power		
1F7	VDDCORE	Power		
1F8	VSS	Power		
1F9	VDDQ_DDR	Power		
1G1	VSS_ANA	Power		
1G2	VDD_ANA	Power		
1G3	VSS	Power		
1G4	VDD	Power		
1G5	VSS	Power		
1G6	VDDCORE	Power		
1G7	VSS	Power		
1G8	VDDQ_DDR	Power		
1G9	VSS	Power		
1H1	VDDA	Power		
1H2	VSSA	Power		
1H3	VDD	Power		
1H4	VSS	Power		
1H5	VDD	Power		
1H6	VSS	Power		
1H7	VDDCORE	Power		
1H8	VSS	Power		

Pin Number TFBGA361	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1H9	VDDQ_DDR	Power		
1J2	VDD	Power		
1J3	VSS	Power		
1J4	VDD	Power		
1J5	VSS	Power		
1J6	VDD	Power		
1J7	VSS	Power		
1J8	VDDQ_DDR	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	stm32-ecu
Project Folder	/home/jordan/Documents/2021/stm32-ecu
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_MP1 V1.4.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls ARM Cortex-A7

Rank	Function Name	Peripheral Instance Name

5.4. Advanced Settings - Generated Function Calls ARM Cortex-M4

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ETZPC_Init	ETZPC
4	MX_IPCC_Init	IPCC
5	MX_DMA_Init	DMA
6	MX_SPI5_Init	SPI5

Rank	Function Name	Peripheral Instance Name
7	MX_RNG2_Init	RNG2

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32MP1
Line	STM32MP157
MCU	STM32MP157DACx
Datasheet	DS12504_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

6.3. Battery Selection

Battery	Li-SOCL2(DD36000)
Capacity	36000.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	450.0 mA
Max Pulse Current	1000.0 mA
Cells in series	1
Cells in parallel	1

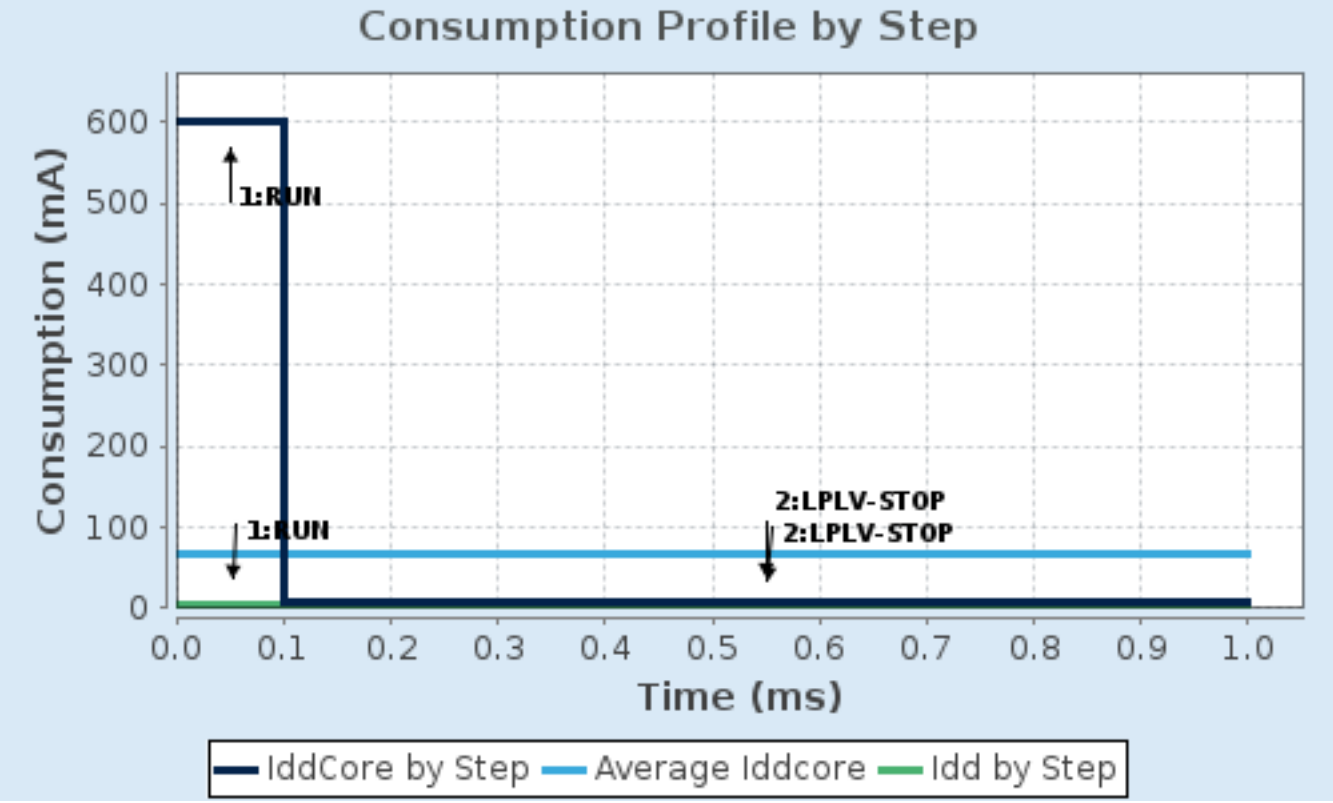
6.4. Sequence

Step	Step1	Step2
Mode	RUN	LPLV-STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Vdd Core	1.38	0.85
MPU0 Mode	P0RUN	P0STOP
MPU1 Mode	P1RUN	P1STOP
MCU Mode	CRUN	CSTOP
Fetch Type	SRAM	NA
MPU0/MPU1 Frequency	800 MHz	0 Hz
Clock Configuration	HSE HSI LSI PLL ALL_IPs_ON	ALL CLOCKS OFF
MCU Frequency	210 MHz	0 Hz
AXI Frequency	264 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Idd Core	600 mA	6.05 mA
Idd	3.7 mA	0.83 mA
Duration	0.1 ms	0.9 ms
DMIPS	0.0	0.0
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	65.44 mA
Battery Life	22 days, 21 hours	Average DMIPS	0.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
600
500
400
300
200
100
0
1:RUN
1:RUN
2:LPLV-STOP
2:LPLV-STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
IddCore by Step
Average Iddcore
Idd by Step

7. Peripherals and Middlewares Configuration

7.1. ADC1

IN18: Single-ended

mode: IN19 Single-ended

7.1.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Mode
Independent mode	Clock Prescaler
Asynchronous clock mode divided by 1	Resolution
ADC 16-bit resolution	Scan Conversion Mode
Disabled	Continuous Conversion Mode
Disabled	Discontinuous Conversion Mode
Disabled	End Of Conversion Selection
End of single conversion	Overrun behaviour
Overrun data preserved	Conversion Data Management Mode
Regular Conversion data stored in DR register only	Low Power Auto Wait
Disabled	Enable Regular Conversions
Enable	Left Bit Shift
No bit shift	Enable Regular Oversampling
Disable	Number Of Conversion
1	External Trigger Conversion Source
Regular Conversion launched by software	External Trigger Conversion Edge
None	Rank
1	Channel
Channel 18	Sampling Time
1.5 Cycles	Offset Number
No offset	Enable Injected Conversions
Disable	Enable Analog WatchDog1 Mode
false	Enable Analog WatchDog2 Mode
false	Enable Analog WatchDog3 Mode
false	

7.2. ADC2

IN18: Single-ended

mode: IN19 Single-ended

7.2.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Mode
Independent mode	Clock Prescaler
Asynchronous clock mode divided by 1	Resolution
ADC 16-bit resolution	Scan Conversion Mode
Disabled	Continuous Conversion Mode
Disabled	Discontinuous Conversion Mode
Disabled	End Of Conversion Selection
End of single conversion	Overrun behaviour
Overrun data preserved	Conversion Data Management Mode
Regular Conversion data stored in DR register only	Low Power Auto Wait
Disabled	Enable Regular Conversions
Enable	Left Bit Shift
No bit shift	Enable Regular Oversampling
Disable	Number Of Conversion
1	External Trigger Conversion Source
Regular Conversion launched by software	External Trigger Conversion Edge
None	Rank
1	Channel
Channel 18	Sampling Time
1.5 Cycles	Offset Number
No offset	Enable Injected Conversions
Disable	Enable Analog WatchDog1 Mode
false	Enable Analog WatchDog2 Mode
false	Enable Analog WatchDog3 Mode
false	

7.3. BSEC

mode: Activated

7.3.1. Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	

	Cortex-A7 secure
Power Domain:	

7.4. CRC1

mode: Activated

7.4.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Default Polynomial State
Enable	Default Init Value State
Enable	Input Data Inversion Mode
None	Output Data Inversion Mode
Disable	Input Data Format
Bytes	

7.5. DDR

DDR Type

DDR Type: DDR3 / DDR3L

Width

Width: 16bits

Density for DDR3(L) 16bits

Density for DDR3(L) 16bits: 4Gb

7.5.1. Parameter Settings:

Core(s) Settings:

Context(s):	Boot loader Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	DDR subsystem frequency
533.0	Speed Bin Grade
DDR3-1066G / 8-8-8	Impedance During Read
Ron 40 ohm / ODT = 80 ohm (Default)	Impedance During Write

Ron 53 ohm / ODT = 60 ohm (Default)	Address Mapping configuration
Row - Bank - Column	Relaxed Timing mode
false	Temperature case over 85°C support
false	Burst Length (BL)
8	

7.5.2. DDR tuning:

Core(s) Settings:

Context(s):	Boot loader Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Skip built-in calibration
false	Byte Lane 0 - Slave DLL phase
0	Byte Lane 0 - DQS gating phase select fine tuning
2	Byte Lane 0 - DQS gating system latency fine tuning
0	Byte Lane 0 - DQS delay fine tuning
3	Byte Lane 0 - DQS# delay fine tuning
3	Byte lane 0 – DQ delay for bit 0 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 0 – DQ delay for bit 1 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 0 – DQ delay for bit 2 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 0 – DQ delay for bit 3 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 0 – DQ delay for bit 4 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 0 – DQ delay for bit 5 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 0 – DQ delay for bit 6 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 0 – DQ delay for bit 7 fine tuning (both DQS/DQS# clock)
0xF	Byte Lane 1 - Slave DLL phase
0	Byte Lane 1 - DQS gating system latency fine tuning
2	Byte Lane 1 - DQS gating system latency fine tuning
0	Byte Lane 1 - DQS delay fine tuning
3	Byte Lane 1 - DQS# delay fine tuning
3	Byte lane 1 – DQ delay for bit 0 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 1 – DQ delay for bit 1 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 1 – DQ delay for bit 2 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 1 – DQ delay for bit 3 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 1 – DQ delay for bit 4 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 1 – DQ delay for bit 5 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 1 – DQ delay for bit 6 fine tuning (both DQS/DQS# clock)
0xF	Byte lane 1 – DQ delay for bit 7 fine tuning (both DQS/DQS# clock)
0xF	

7.6. DTS

mode: Activated

7.6.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.7. ETH1

Mode: RGMII (Reduced GMII)

mode: ETH 125MHz Clock Input

7.7.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.8. ETZPC

mode: Activated

7.8.1. Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure Cortex-M4
Initialized Context:	Cortex-A7 secure
Power Domain:	

7.9. GIC

7.9.1. Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 secure
Power Domain:	

7.10. GPU

mode: Activated

7.10.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.11. HASH1

mode: Activated

7.11.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure Boot loader
Initialized Context:	Cortex-A7 non secure
Power Domain:	Secure hash algorithm type
SHA1	Hash data type in bit
32	

7.12. HDMI_CEC

mode: Activated

7.12.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	

	Cortex-A7 non secure
Power Domain:	Signal Free Time
2.5, 4 or 6 nominal data bit periods	Rx tolerance
Standard tolerance	Signal Free Time option
SFT timer starts when Transmission Start Of Message is set by software	Listening mode
Receive all messages	Logical address 0
Disable	Logical address 1
Disable	Logical address 2
Disable	Logical address 3
Disable	Logical address 4
Disable	Logical address 5
Disable	Logical address 6
Disable	Logical address 7
Disable	Logical address 8
Disable	Logical address 9
Disable	Logical address 10
Disable	Logical address 11
Disable	Logical address 12
Disable	Logical address 13
Disable	Logical address 14
Disable	Received data buffer name
cec_receive_buffer	Stop reception on bit rising error
Reception is stopped	Generate error bit on bit rising error
No error bit generation	Generate error bit on long bit period error
No error bit generation	Avoid error bit generation on error detection in broadcast
Error bit generation	

7.13. HSEM

mode: Activated

7.13.1. Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure Cortex-M4
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.14. I2C1

I2C: I2C

7.14.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Custom Timing
Disabled	I2C Speed Mode
Standard Mode	I2C Speed Frequency (KHz)
100	Rise Time (ns)
0	Fall Time (ns)
0	Coefficient of Digital Filter
0	Analog Filter
Enabled	Timing
0x10707DBC	Clock No Stretch Mode
Disabled	General Call Address Detection
Disabled	Primary Address Length selection
7-bit	Dual Address Acknowledged
Disabled	Primary slave address
0	

7.15. I2C4

I2C: I2C

7.15.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure Boot loader Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Custom Timing
Disabled	I2C Speed Mode
Standard Mode	I2C Speed Frequency (KHz)
100	Rise Time (ns)
0	Fall Time (ns)

0	Coefficient of Digital Filter
0	Analog Filter
Enabled	Timing
0x10707DBC	Clock No Stretch Mode
Disabled	General Call Address Detection
Disabled	Primary Address Length selection
7-bit	Dual Address Acknowledged
Disabled	Primary slave address
0	

7.16. I2S2

Mode: Half-Duplex Master -- EV1 DK2 only --

7.16.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Transmission Mode
Mode Master Transmit	Communication Standard
I2S Philips	Data and Frame Format
16 Bits Data on 16 Bits Frame	Selected Audio Frequency
16 KHz	Real Audio Frequency
15.998 KHz *	Error between Selected and Real
-0.01 % *	Clock Source
PLL I2SR Clock	Clock Polarity
Low	First Bit
Firstbit Msb	Ws Inversion
Ws Inversion Disable	Io Swap
Io Swap Disable	Data24 Bit Alignment
Data 24 Bit Alignment Right	Fifo Threshold
Fifo Threshold 01 Data	Master Keep Io State
Master Keep Io State Disable	Slave Extend Fre Detection
Slave Extend Fre Detection Disable	

7.17. IPCC

mode: Activated

7.17.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure Cortex-M4
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.18. IWDG2

mode: Activated

7.18.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	IWDG counter clock prescaler
4	IWDG window value
4095	IWDG down-counter reload value
4095	

7.19. LTDC

Display Type: RGB888 (24 bits)

7.19.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Horizontal Synchronization Width
8	Horizontal Back Porch
7	Active Width
640	Horizontal Front Porch
6	HSync Width
7	Accumulated Horizontal Back Porch Width
14	Accumulated Active Width
654	Total Width

660	Vertical Synchronization Height
4	Vertical Back Porch
2	Active Height
480	Vertical Front Porch
2	VSync Height
3	Accumulated Vertical Back Porch Height
5	Accumulated Active Height
485	Total Height
487	Horizontal Synchronization Polarity
Active Low	Vertical Synchronization Polarity
Active Low	Not Data Enable Polarity
Active Low	Pixel Clock Polarity
Normal Input	Red
0	Green
0	Blue
0	

7.19.2. Layer Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Layer 0 - Blue
0	Layer 0 - Green
0	Layer 0 - Red
0	Layer 1 - Blue
0	Layer 1 - Green
0	Layer 1 - Red
0	Number of Layers
2 layers	Layer 0 - Window Horizontal Start
0	Layer 0 - Window Horizontal Stop
0	Layer 0 - Window Vertical Start
0	Layer 0 - Window Vertical Stop
0	Layer 1 - Window Horizontal Start
0	Layer 1 - Window Horizontal Stop
0	Layer 1 - Window Vertical Start
0	Layer 1 - Window Vertical Stop
0	Layer 0 - Pixel Format
ARGB8888	Layer 1 - Pixel Format
ARGB8888	Layer 0 - Alpha constant for blending
0	Layer 0 - Default Alpha value

0	Layer 0 - Blending Factor1
Alpha constant	Layer 0 - Blending Factor2
Alpha constant	Layer 1 - Alpha constant for blending
0	Layer 1 - Default Alpha value
0	Layer 1 - Blending Factor1
Alpha constant	Layer 1 - Blending Factor2
Alpha constant	Layer 0 - Color Frame Buffer Start Adress
0	Layer 0 - Color Frame Buffer Line Length (Image Width)
0	Layer 0 - Color Frame Buffer Number of Lines (Image Height)
0	Layer 1 - Color Frame Buffer Start Adress
0	Layer 1 - Color Frame Buffer Line Length (Image Width)
0	Layer 1 - Color Frame Buffer Number of Lines (Image Height)
0	

7.20. PWR

mode: Wake-Up 1

7.20.1. Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure Cortex-M4
Initialized Context:	Cortex-A7 secure
Power Domain:	

7.21. RCC

High Speed Clock (HSE): DIGBYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.21.1. Parameter Settings:

Core(s) Settings:

Context(s):	Boot ROM Boot loader Cortex-A7 secure Cortex-A7 non secure Cortex-M4
Initialized Context:	

	Cortex-A7 non secure
Power Domain:	PLL1 CSG mode
DISABLED	PLL2 CSG mode
DISABLED	PLL3 CSG mode
DISABLED	PLL4 CSG mode
DISABLED	TIM Group1 Prescaler Selection
Disabled	TIM Group2 Prescaler Selection
Disabled	HSE Startup Timout Value (ms)
100	LSE Startup Timout Value (ms)
5000	LSE Drive Capability
LSE oscillator medium high drive capability	CSI Calibration Value
16	HSI Calibration Value
16	HSI clock calibration feature
Enable	CSI clock calibration feature
Enable	Periodic calibration Value
60	VDD voltage (V)
3.3	User defined configuration
FALSE	

7.22. RNG1

mode: Activated

7.22.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 secure
Power Domain:	Clock Error Detection
Enable	

7.23. RNG2

mode: Activated

7.23.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4

Initialized Context:	Cortex-M4
Power Domain:	Clock Error Detection
Enable	

7.24. RTC

mode: Activate Clock Source

7.24.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Hour Format
Hourformat 24	Asynchronous Predivider value
127	Synchronous Predivider value
255	

7.25. SAI2

Mode: Master with Master Clock Out

Mode: SPDIF TX Transmitter (IEC60958)

7.25.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	Synchronization Inputs
Asynchronous	Protocol
Free	Audio Mode
Master Transmit	Frame Length
8 bits	Data Size
24 Bits	Slot Size
DataSize	Output Mode
Stereo	Companding Mode
No companding mode	SAI SD Line Output Mode
Driven	First Bit
MSB First	Frame Synchro Active Level Length

1	Frame Synchro Definition
Start Frame	Frame Synchro Polarity
Active Low	Frame Synchro Offset
First Bit	First Bit Offset
0	Number of Slots
1	Slot Active Final Value
0x00000000	Slot Active
Neither	Clock Source
SAI PLL Clock	Master Clock Divider
Enabled	Audio Frequency
192 KHz	Real Audio Frequency
95.991 KHz *	Error between Selected
-50.0 % *	Clock Strobing
Falling Edge	Fifo Threshold
Empty	Output Drive
Disabled	Master Clock Over Sampling
Disabled	Synchronization Inputs
Asynchronous	Protocol
SPDIF	Audio Mode
Master Transmit	Output Mode
Stereo	Companding Mode
No companding mode	Audio Frequency
48 KHz	Real Audio Frequency
0	Fifo Threshold
Empty	Output Drive
Disabled	

7.26. SDMMC1

Mode: SD 4 bits Wide bus

7.26.1. Parameter Settings:

Core(s) Settings:

Context(s):	Boot ROM Cortex-A7 non secure Boot loader
Initialized Context:	Cortex-A7 non secure
Power Domain:	Clock transition on which the bit capture is made
Rising transition	SDMMC Clock output enable when the bus is idle
Disable the power save for the clock	SDMMC hardware flow control

The hardware control flow is disabled	SDMMCCLK clock divide factor
0	

7.27. SPI5

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.27.1. Parameter Settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	Frame Format
Motorola	Data Size
8 Bits *	First Bit
MSB First	Prescaler (for Baud Rate)
64 *	Baud Rate
1.631858 MBits/s *	Clock Polarity (CPOL)
Low	Clock Phase (CPHA)
2 Edge *	CRC Calculation
Disabled	NSSP Mode
Enabled	NSS Signal Type
Output Hardware	Fifo Threshold
Fifo Threshold 01 Data	Tx Crc Initialization Pattern
All Zero Pattern	Rx Crc Initialization Pattern
All Zero Pattern	Nss Polarity
Nss Polarity Low	Master Ss Idleness
00 Cycle	Master Inter Data Idleness
00 Cycle	Master Receiver Auto Susp
Disable	Master Keep Io State
Master Keep Io State Disable	IO Swap
Disabled	

7.28. SYS

Timebase Source: TIM1

7.28.1. Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	

7.29. TAMP

mode: Activated

7.29.1. Core(s) Settings:

Context(s):	Cortex-A7 secure Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.30. UART4

Mode: Asynchronous

7.30.1. Parameter Settings:

Core(s) Settings:

Context(s):	Boot ROM Cortex-A7 non secure Boot loader
Initialized Context:	Cortex-A7 non secure
Power Domain:	Baud Rate
115200	Word Length
8 Bits (including Parity)	Parity
None	Stop Bits
1	Data Direction
Receive and Transmit	Over Sampling
16 Samples	Single Sample
Disable	ClockPrescaler
1	Fifo Mode
FIFO mode disable	Txfifo Threshold
1 eighth full configuration	Rxfifo Threshold
1 eighth full configuration	Auto Baudrate

Disable	TX Pin Active Level Inversion
Disable	RX Pin Active Level Inversion
Disable	Data Inversion
Disable	TX and RX Pins Swapping
Disable	Overrun
Enable	DMA on RX Error
Enable	MSB First
Disable	

7.31. USBH_HS1

mode: USB Host controller

7.31.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.32. USB_OTG_HS

High Speed: OTG/Dual_Role_Device Type C

7.32.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure Boot loader
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.33. VREFBUF

mode: Activated

7.33.1. Core(s) Settings:

Context(s):	Cortex-A7 non secure
Initialized Context:	Cortex-A7 non secure
Power Domain:	

7.34. FREERTOS

Interface: CMSIS_V1

7.34.1. Config parameters:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	FreeRTOS API
CMSIS v1	FreeRTOS version
10.2.1	CMSIS-RTOS version
1.02	ENABLE_MPU
Disabled	ENABLE_FPU
Enabled *	USE_PREEMPTION
Enabled	CPU_CLOCK_HZ
SystemCoreClock	TICK_RATE_HZ
1000	MAX_PRIORITIES
7	MINIMAL_STACK_SIZE
128	MAX_TASK_NAME_LEN
16	USE_16_BIT_TICKS
Disabled	IDLE_SHOULD_YIELD
Enabled	USE_MUTEXES
Enabled	USE_RECURSIVE_MUTEXES
Enabled *	USE_COUNTING_SEMAPHORES
Enabled *	QUEUE_REGISTRY_SIZE
8	USE_APPLICATION_TASK_TAG
Disabled	ENABLE_BACKWARD_COMPATIBILITY
Enabled	USE_PORT_OPTIMISED_TASK_SELECTION
Enabled	USE_TICKLESS_IDLE
Disabled	USE_TASK_NOTIFICATIONS
Enabled	RECORD_STACK_HIGH_ADDRESS
Disabled	Memory Allocation
Dynamic / Static	TOTAL_HEAP_SIZE
3072	Memory Management scheme
heap_4	USE_IDLE_HOOK
Disabled	USE_TICK_HOOK
Disabled	USE_MALLOC_FAILED_HOOK
Enabled *	USE_DAEMON_TASK_STARTUP_HOOK
Disabled	CHECK_FOR_STACK_OVERFLOW

Option1 *	GENERATE_RUN_TIME_STATS
Disabled	USE_TRACE_FACILITY
Disabled	USE_STATS_FORMATTING_FUNCTIONS
Disabled	USE_CO_ROUTINES
Disabled	MAX_CO_ROUTINE_PRIORITIES
2	USE_TIMERS
Enabled	TIMER_TASK_PRIORITY
3 *	TIMER_QUEUE_LENGTH
32 *	TIMER_TASK_STACK_DEPTH
256	LIBRARY_LOWEST_INTERRUPT_PRIORITY
15	LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY
5	MESSAGE_BUFFER_LENGTH_TYPE
size_t	USE_POSIX_ERRNO
Disabled	

7.34.2. Include parameters:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	vTaskPrioritySet
Enabled	uxTaskPriorityGet
Enabled	vTaskDelete
Enabled	vTaskCleanUpResources
Disabled	vTaskSuspend
Enabled	vTaskDelayUntil
Disabled	vTaskDelay
Enabled	xTaskGetSchedulerState
Enabled	xTaskResumeFromISR
Enabled	xQueueGetMutexHolder
Enabled *	xSemaphoreGetMutexHolder
Enabled *	pcTaskGetTaskName
Disabled	uxTaskGetStackHighWaterMark
Disabled	xTaskGetCurrentTaskHandle
Enabled *	eTaskGetState
Disabled	xEventGroupSetBitFromISR
Disabled	xTimerPendFunctionCall
Enabled *	xTaskAbortDelay
Disabled	xTaskGetHandle
Enabled *	uxTaskGetStackHighWaterMark2

Disabled

7.34.3. Advanced settings:

Core(s) Settings:

Context(s):	Cortex-M4
Initialized Context:	Cortex-M4
Power Domain:	USE_NEWLIB_REENTRANT
Enabled *	Use FW pack heap file
Enabled	

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
ADC1	PA5	ADC1_INP19	Analog mode	n/a	n/a	USB_PWR_CC2[317JD24BZTF3K3C3_CC2]	Cortex-A7 non secure	Cortex-A7 non secure
	PA4	ADC1_INP18	Analog mode	n/a	n/a	USB_PWR_CC1[317JD24BZTF3K3C3_CC1]	Cortex-A7 non secure	Cortex-A7 non secure
ADC2	PA5	ADC2_INP19	Analog mode	n/a	n/a	USB_PWR_CC2[317JD24BZTF3K3C3_CC2]	Cortex-A7 non secure	Cortex-A7 non secure
	PA4	ADC2_INP18	Analog mode	n/a	n/a	USB_PWR_CC1[317JD24BZTF3K3C3_CC1]	Cortex-A7 non secure	Cortex-A7 non secure
DDR	DDR_RESETN	DDR_RESETN	n/a	n/a	n/a	DDR_RESETN [MT41K256M16TW_RESET#]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A7	DDR_A7	n/a	n/a	n/a	DDR_A7 [MT41K256M16TW_A7]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ3	DDR_DQ3	n/a	n/a	n/a	DDR_DQ3 [MT41K256M16TW_DQU3]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ0	DDR_DQ0	n/a	n/a	n/a	DDR_DQ0 [MT41K256M16TW_DQU5]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A13	DDR_A13	n/a	n/a	n/a	DDR_A13 [MT41K256M16TW_A13]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ1	DDR_DQ1	n/a	n/a	n/a	DDR_DQ1 [MT41K256M16TW_DQU1]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A9	DDR_A9	n/a	n/a	n/a	DDR_A9 [MT41K256M16TW_A9]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ7	DDR_DQ7	n/a	n/a	n/a	DDR_DQ7 [MT41K256M16TW_DQU7]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQS0P	DDR_DQS0P	n/a	n/a	n/a	DDR_DQS0_P [MT41K256M16TW_DQSU]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQS0N	DDR_DQS0N	n/a	n/a	n/a	DDR_DQS0_N [MT41K256M16TW_DQSU#]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	DDR_A5	DDR_A5	n/a	n/a	n/a	DDR_A5 [MT41K256M16TW_A5]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ2	DDR_DQ2	n/a	n/a	n/a	DDR_DQ2 [MT41K256M16TW_DQU4]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ6	DDR_DQ6	n/a	n/a	n/a	DDR_DQ6 [MT41K256M16TW_DQU0]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQM0	DDR_DQM0	n/a	n/a	n/a	DDR_DQM0 [MT41K256M16TW_DMU]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A2	DDR_A2	n/a	n/a	n/a	DDR_A2 [MT41K256M16TW_A2]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ4	DDR_DQ4	n/a	n/a	n/a	DDR_DQ4 [MT41K256M16TW_DQU6]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ5	DDR_DQ5	n/a	n/a	n/a	DDR_DQ5 [MT41K256M16TW_DQU2]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DTO0	DDR_DTO0	n/a	n/a	n/a	DDR_DTO0	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A3	DDR_A3	n/a	n/a	n/a	DDR_A3 [MT41K256M16TW_A3]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_ZQ	DDR_ZQ	n/a	n/a	n/a	DDR_ZQ	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A0	DDR_A0	n/a	n/a	n/a	DDR_A0 [MT41K256M16TW_A0]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DTO1	DDR_DTO1	n/a	n/a	n/a	DDR_DTO1	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_ODT	DDR_ODT	n/a	n/a	n/a	DDR_ODT [MT41K256M16TW_ODT]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_BA0	DDR_BA0	n/a	n/a	n/a	DDR_BA0 [MT41K256M16TW_BA0]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_WEN	DDR_WEN	n/a	n/a	n/a	DDR_WEN_P [MT41K256M16TW_WE#]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_BA2	DDR_BA2	n/a	n/a	n/a	DDR_BA2 [MT41K256M16TW_	Boot loader Cortex-A7	Boot loader Cortex-A7

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
						BA2]	secure	secure
	DDR_CSN	DDR_CSN	n/a	n/a	n/a	DDR_CSN [MT41K256M16TW_CS#]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_CASN	DDR_CASN	n/a	n/a	n/a	DDR_CASN [MT41K256M16TW_CAS#]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_RASN	DDR_RASN	n/a	n/a	n/a	DDR_RASN [MT41K256M16TW_RAS#]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_CLKP	DDR_CLKP	n/a	n/a	n/a	DDR_CLK_P [MT41K256M16TW_CK]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_CLKN	DDR_CLKN	n/a	n/a	n/a	DDR_CLK_N [MT41K256M16TW_CK#]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A1	DDR_A1	n/a	n/a	n/a	DDR_A1 [MT41K256M16TW_A1]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A12	DDR_A12	n/a	n/a	n/a	DDR_A12 [MT41K256M16TW_A12]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A11	DDR_A11	n/a	n/a	n/a	DDR_A11 [MT41K256M16TW_A11]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A14	DDR_A14	n/a	n/a	n/a	DDR_A14 [MT41K256M16TW_A14]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A10	DDR_A10	n/a	n/a	n/a	DDR_A10 [MT41K256M16TW_A10]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_CKE	DDR_CKE	n/a	n/a	n/a	DDR_CKE [MT41K256M16TW_CKE]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ8	DDR_DQ8	n/a	n/a	n/a	DDR_DQ8 [MT41K256M16TW_DQL2]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ10	DDR_DQ10	n/a	n/a	n/a	DDR_DQ10 [MT41K256M16TW_DQL6]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ13	DDR_DQ13	n/a	n/a	n/a	DDR_DQ13 [MT41K256M16TW_DQL4]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_BA1	DDR_BA1	n/a	n/a	n/a	DDR_BA1 [MT41K256M16TW_BA1]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	DDR_DQ9	DDR_DQ9	n/a	n/a	n/a	DDR_DQ9 [MT41K256M16TW_DQL0]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQS1P	DDR_DQS1P	n/a	n/a	n/a	DDR_DQS1_P [MT41K256M16TW_DQSL]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQS1N	DDR_DQS1N	n/a	n/a	n/a	DDR_DQS1_N [MT41K256M16TW_DQSL#]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A4	DDR_A4	n/a	n/a	n/a	DDR_A4 [MT41K256M16TW_A4]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQM1	DDR_DQM1	n/a	n/a	n/a	DDR_DQM1 [MT41K256M16TW_DML]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A6	DDR_A6	n/a	n/a	n/a	DDR_A6 [MT41K256M16TW_A6]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ11	DDR_DQ11	n/a	n/a	n/a	DDR_DQ11 [MT41K256M16TW_DQL1]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ14	DDR_DQ14	n/a	n/a	n/a	DDR_DQ14 [MT41K256M16TW_DQL7]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ12	DDR_DQ12	n/a	n/a	n/a	DDR_DQ12 [MT41K256M16TW_DQL5]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_ATO	DDR_ATO	n/a	n/a	n/a	DDR_ATO	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_A8	DDR_A8	n/a	n/a	n/a	DDR_A8 [MT41K256M16TW_A8]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_DQ15	DDR_DQ15	n/a	n/a	n/a	DDR_DQ15 [MT41K256M16TW_DQL3]	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
	DDR_VREF	DDR_VREF	n/a	n/a	n/a	VREF_DDR	Boot loader Cortex-A7 secure	Boot loader Cortex-A7 secure
ETH1	PE2	ETH1_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	High	ETH_TXD3 [RTL8211F_TXD3]	Cortex-A7 non secure	Cortex-A7 non secure
	PC2	ETH1_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	High	ETH_TXD2 [RTL8211F_TXD2]	Cortex-A7 non secure	Cortex-A7 non secure
	PG5	ETH1_CLK125	Alternate Function Push Pull	No pull-up and no pull-down	High	ETH_CLK125 [RTL8211F_CLKOUT]	Cortex-A7 non secure	Cortex-A7 non secure

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PG14	ETH1_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High	ETH_TXD1 [RTL8211F_TXD1]	Cortex-A7 non secure	Cortex-A7 non secure
	PG13	ETH1_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High	ETH_TXD0 [RTL8211F_TXD0]	Cortex-A7 non secure	Cortex-A7 non secure
	PA1	ETH1_RX_CLK	Alternate function	No pull-up and no pull-down	n/a	ETH_RX_CLK [RTL8211F_RXCLK_PHYAD1]	Cortex-A7 non secure	Cortex-A7 non secure
	PC1	ETH1_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High	ETH_MDC [RTL8211F_MDC]	Cortex-A7 non secure	Cortex-A7 non secure
	PB1	ETH1_RXD3	Alternate function	No pull-up and no pull-down	n/a	ETH_RXD3 [RTL8211F_RXD3_PHYAD0]	Cortex-A7 non secure	Cortex-A7 non secure
	PB11	ETH1_TX_CTL	Alternate Function Push Pull	No pull-up and no pull-down	High	ETH_TX_EN [RTL8211F_TXCTL]	Cortex-A7 non secure	Cortex-A7 non secure
	PG4	ETH1_GTX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High	ETH_GTX_CLK [RTL8211F_TXCLK]	Cortex-A7 non secure	Cortex-A7 non secure
	PB0	ETH1_RXD2	Alternate function	No pull-up and no pull-down	n/a	ETH_RXD2 [RTL8211F_RXD2_PLLOFF]	Cortex-A7 non secure	Cortex-A7 non secure
	PC5	ETH1_RXD1	Alternate function	No pull-up and no pull-down	n/a	ETH_RXD1 [RTL8211F_RXD1_TXDLY]	Cortex-A7 non secure	Cortex-A7 non secure
	PA7	ETH1_RX_CTL	Alternate function	No pull-up and no pull-down	n/a	ETH_RX_DV [RTL8211F_RXCTL_PHYAD2]	Cortex-A7 non secure	Cortex-A7 non secure
	PA2	ETH1_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	ETH_MIO [RTL8211F_MIO]	Cortex-A7 non secure	Cortex-A7 non secure
	PC4	ETH1_RXD0	Alternate function	No pull-up and no pull-down	n/a	ETH_RXD0 [RTL8211F_RXD0_RXDLY]	Cortex-A7 non secure	Cortex-A7 non secure
HDMI_CEC	PB6	CEC	Alternate Function Open Drain	No pull-up and no pull-down	Low	HDMI_CEC [SiI9022ACNU_CEC_D]	Cortex-A7 non secure	Cortex-A7 non secure
I2C1	PF15	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	I2C1_SDA [CS42L51-CNZ_SDA]	Cortex-A7 non secure	Cortex-A7 non secure
	PD12	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	I2C1_SCL [CS42L51-CNZ_SCL]	Cortex-A7 non secure	Cortex-A7 non secure
I2C4	PZ4	I2C4_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	I2C4_SCL [STPMU1A_SCL]	Cortex-A7 secure Boot loader	Cortex-A7 secure Boot loader
	PZ5	I2C4_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	I2C4_SDA [STPMU1A_SDA]	Cortex-A7 secure Boot loader	Cortex-A7 secure Boot loader
I2S2	PA9	I2S2_CK	Alternate Function	No pull-up and no pull-	Medium		Cortex-A7 non	Cortex-A7 non

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down			secure	secure
	PB9	I2S2_WS	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	Cortex-A7 non secure
	PI3	I2S2_SDO	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	Cortex-A7 non secure
LTDC	PH15	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PH12	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PD10	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PH10	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PH14	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PH9	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PE6	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PE5	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PH13	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PE15	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PH8	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PI2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PI4	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PD9	LTDC_B0	Alternate Function	No pull-up and no pull-			Cortex-A7 non	Cortex-A7 non

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
			Push Pull	down	**Medium ***		secure	secure
	PD8	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PG12	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PA3	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PH3	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PH2	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PC0	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PG10	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	**Medium ***		Cortex-A7 non secure	Cortex-A7 non secure
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-A7 non secure	Cortex-A7 non secure
PWR	PA0	PWR_WKUP1	n/a	n/a	n/a		Cortex-A7 secure* Cortex-A7 non	Cortex-A7 secure* Cortex-A7 non
RCC	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a		Boot ROM Boot loader Cortex-A7	Boot ROM Boot loader Cortex-A7
	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a		Boot ROM Boot loader Cortex-A7	Boot ROM Boot loader Cortex-A7
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a		Boot ROM Boot loader Cortex-A7	Boot ROM Boot loader Cortex-A7
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a		Boot ROM Boot loader Cortex-A7	Boot ROM Boot loader Cortex-A7
SAI2	PE0	SAI2_MCLK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	Cortex-A7 non secure

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
	PI7	SAI2_FS_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	Cortex-A7 non secure
	PI5	SAI2_SCK_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	Cortex-A7 non secure
	PI6	SAI2_SD_A	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	Cortex-A7 non secure
	PF11	SAI2_SD_B	Alternate Function Push Pull	No pull-up and no pull-down	Low		Cortex-A7 non secure	Cortex-A7 non secure
SDMMC1	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Medium	SDMMC1_CMD [PJS008-2003-1]	Boot ROM Cortex-A7 non secure*	Boot ROM Cortex-A7 non secure*
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	SDMMC1_CK [PJS008-2003-1]	Boot ROM Cortex-A7 non secure*	Boot ROM Cortex-A7 non secure*
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Medium	SDMMC1_D2 [PJS008-2003-1]	Boot ROM Cortex-A7 non secure*	Boot ROM Cortex-A7 non secure*
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Medium	SDMMC1_D3 [PJS008-2003-1]	Boot ROM Cortex-A7 non secure*	Boot ROM Cortex-A7 non secure*
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Medium	SDMMC1_D1 [PJS008-2003-1]	Boot ROM Cortex-A7 non secure*	Boot ROM Cortex-A7 non secure*
	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Medium	SDMMC1_D0 [PJS008-2003-1]	Boot ROM Cortex-A7 non secure*	Boot ROM Cortex-A7 non secure*
SPI5	PF6	SPI5_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	Cortex-M4
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	Cortex-M4
	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	Cortex-M4
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Medium		Cortex-M4	Cortex-M4
UART4	PG11	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	STLINK_RX [STM32F103CBT6_PA3]	Boot ROM Cortex-A7 non secure*	Boot ROM Cortex-A7 non secure*
	PB2	UART4_RX	Alternate function	No pull-up and no pull-down	n/a	STLINK_TX [STM32F103CBT6_PA2]	Boot ROM Cortex-A7 non secure*	Boot ROM Cortex-A7 non secure*
USBH_HS1	USB_DM1	USBH_HS1_DM	n/a	n/a	n/a	USB_HUB_N [USB2514B_USB_UP_DM]	Cortex-A7 non secure	Cortex-A7 non secure
	USB_DP1	USBH_HS1_DP	n/a	n/a	n/a	USB_HUB_P [USB2514B_USB_UP_DP]	Cortex-A7 non secure	Cortex-A7 non secure

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
USB_OTG_HS	USB_DM2	USB_OTG_HS_DM	n/a	n/a	n/a		Cortex-A7 non secure* Boot loader	Cortex-A7 non secure* Boot loader
	USB_DP2	USB_OTG_HS_DP	n/a	n/a	n/a		Cortex-A7 non secure* Boot loader	Cortex-A7 non secure* Boot loader
GPIO	PH5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	BT_HOST_WAKE [LBEE5KL1DX_BT_HOST_WAKE]		
	PF2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INT [FH26W-25S_INT]		
	PH4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WL_REG_ON [LBEE5KL1DX_WL_REG_ON]		
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	WL_HOST_WAKE [LBEE5KL1DX_WL_HOST_WAKE]		
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TE [FH26W-25S_TE]		
	PA15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BL_CTRL [STLD40DPUR_EN]		
	PB7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	uSD_DETECT [PJS008-2003-1]		
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RSTN [FH26W-25S_RSTN]		
	PZ6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BT_REG_ON [LBEE5KL1DX_BT_REG_ON]		
	PZ7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BT_DEV_WAKE [LBEE5KL1DX_BT_DEV_WAKE]		
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PMIC_WAKEUP [STPMU1A_WAKEUP]		
	PA13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PA13 [LD6_RED]		
	PI11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	STUSB1600_IRQOUTn [STUSB1600_ALER		
	PA14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	PA14 [SW-PUSH-TS-02H-Blue]		
	PG1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	HDMI_INT [Sil9022ACNU_INT]		
	PH7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_Y [LD7_ORANGE]		
	PG9	GPIO_Output	Output Push Pull	No pull-up and no pull-	Low	AUDIO_RST		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label	Context	Power Domain
				down		[CS42L51-CNZ_RESET]		
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	HDMI_NRST [SiI9022ACNU_RESET#]		
	PA6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	ETH_MDINT [RTL8211F_INT]		
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_B [LD8_BLUE]		

* Initialized context

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI5_RX	DMA2_Stream0	Peripheral To Memory	Low
SPI5_TX	DMA2_Stream1	Memory To Peripheral	Low

SPI5_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI5_TX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

8.3. MDMA configuration

nothing configured in DMA service

8.4. NVIC configuration

8.4.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	1	0
Pre-fetch fault, memory access fault	true	1	0
Undefined instruction or illegal state	true	1	0
System service call via SWI instruction	true	1	0
Debug monitor	true	1	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
TIM1 update interrupt	true	15	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream1 global interrupt	true	5	0
SPI5 global interrupt	true	5	0
IPCC RX1 occupied interrupt	true	5	0
IPCC TX1 free interrupt	true	5	0
RCC wake-up interrupt	true	0	0
RCC global interrupt	unused		
FPU global interrupt	unused		
HSEM interrupt 2	unused		
RNG2 global interrupt	unused		
Cortex-A7 send event interrupt through EXTI line 66	unused		

8.4.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
TIM1 update interrupt	false	true	true
DMA2 stream0 global interrupt	false	true	true

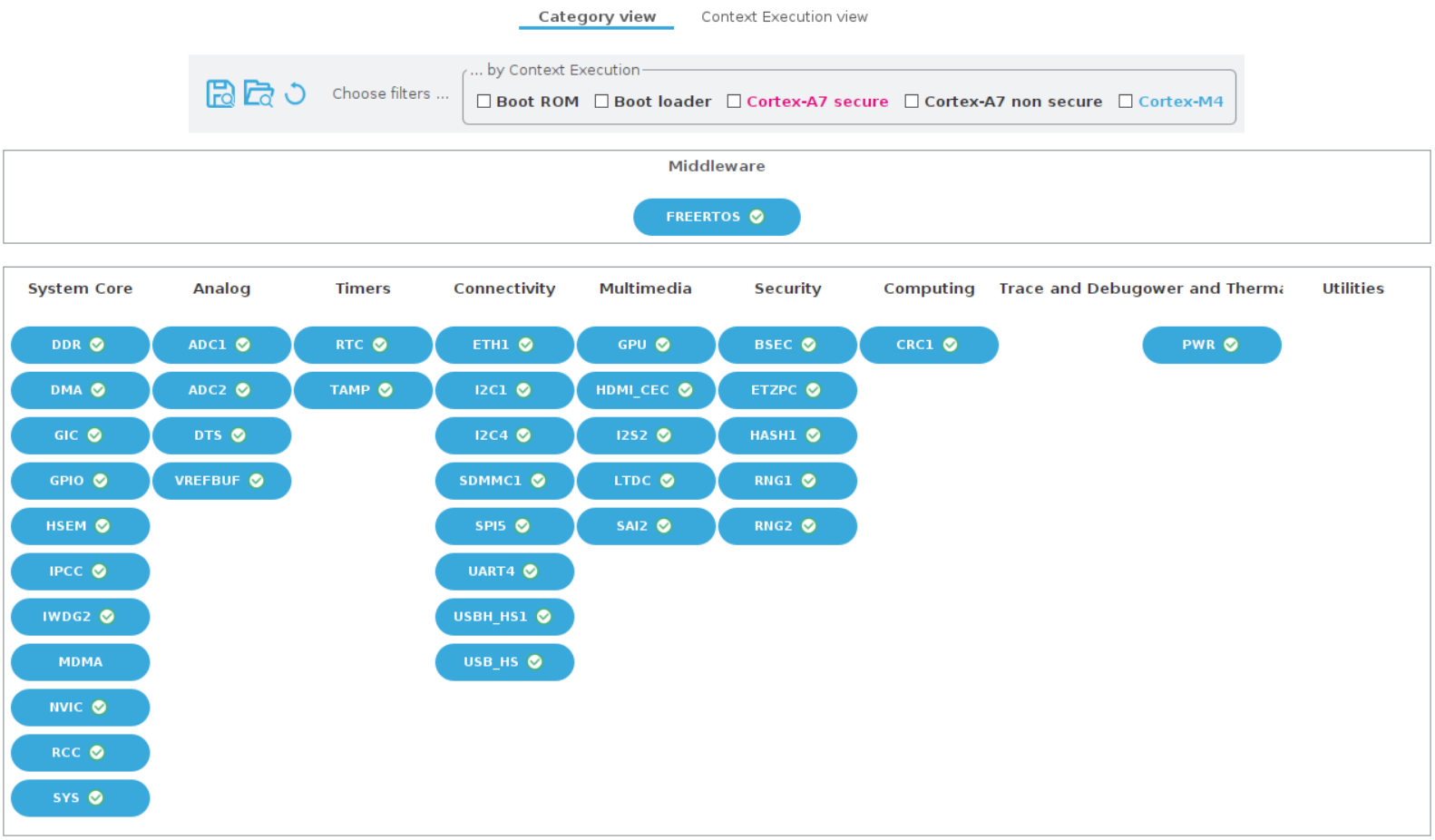
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
DMA2 stream1 global interrupt	false	true	true
SPI5 global interrupt	false	true	true
IPCC RX1 occupied interrupt	false	true	true
IPCC TX1 free interrupt	false	true	true
RCC wake-up interrupt	false	true	true

*** User modified value**

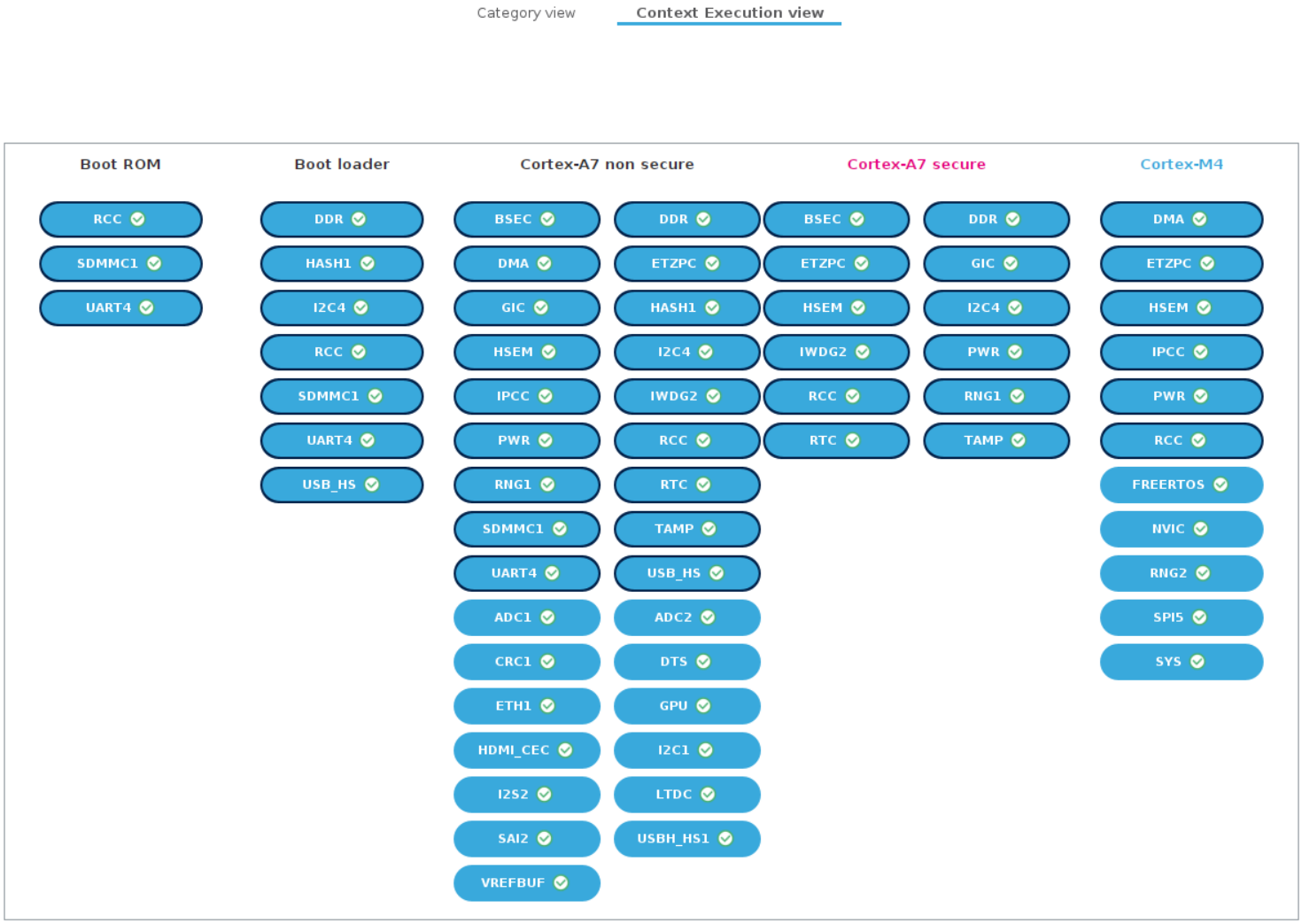
9. System Views

9.1. Category view

9.1.1. Current



9.2. Context Execution view



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00489389.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00327659.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00596687.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00516256.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
Application note	http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note	http://www.st.com/resource/en/application_note/DM00389996.pdf
Application note	http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note	http://www.st.com/resource/en/application_note/DM00449434.pdf
Application note	http://www.st.com/resource/en/application_note/DM00462392.pdf
Application note	http://www.st.com/resource/en/application_note/DM00505673.pdf
Application note	http://www.st.com/resource/en/application_note/DM00535045.pdf
Application note	http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00560967.pdf
Application note	http://www.st.com/resource/en/application_note/DM00561921.pdf
Application note	http://www.st.com/resource/en/application_note/DM00564136.pdf
Application note	http://www.st.com/resource/en/application_note/DM00589815.pdf
Application note	http://www.st.com/resource/en/application_note/DM00595472.pdf
Application note	http://www.st.com/resource/en/application_note/DM00625700.pdf
Application note	http://www.st.com/resource/en/application_note/DM00681502.pdf
Application note	http://www.st.com/resource/en/application_note/DM00693021.pdf

Application note	http://www.st.com/resource/en/application_note/DM00713831.pdf
Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf