			expanded_region		
	e		u_ocl_region inst		
		±		M00_AXI_araddr[33:0]	M00_AXI_araddr[33:0]
				M00_AXI_arburst[1:0] M00_AXI_arcache[3:0]	M00_AXI_arburst[1:0] M00_AXI_arcache[3:0]
				M00_AXI_arid[3:0]	M00_AXI_arid[3:0] M00_AXI_arlen[7:0]
				M00_AXI_arlock	M00_AXI_arlock
				M00_AXI_arprot[2:0] M00_AXI_argos[3:0]	M00_AXI_arprot(2:0) M00_AXI_argos(3:0)
				M00_AXI_arsize[2:0] M00_AXI_arvalid	M00_AXI_arsize[2:0] M00_AXI_arvalid
				M00_AXI_awaddr[33:0]	M00_AXI_awaddr[33:0
				M00_AXI_awburst[1:0] M00_AXI_awcache[3:0]	M00_AXI_awburst[1:0] M00_AXI_awcache[3:0
				M00_AXI_awid[3:0] M00_AXI_awlen[7:0]	M00_AXI_awid[3:0] M00_AXI_awlen[7:0]
				M00_AXI_awlock	M00_AXI_awlock
				M00_AXI_awprot[2:0] M00_AXI_awqos[3:0]	M00_AXI_awprot(2:0) M00_AXI_awqos(3:0)
				M00_AXI_awsize[2:0] M00_AXI_awvalid	M00_AXI_awsize[2:0] M00_AXI_awvalid
				M00_AXI_bready	M00_AXI_bready
				M00_AXI_rready M00_AXI_wdata[511:0]	M00_AXI_rready M00_AXI_wdata[511:0
CONTROL_CL	K CONTROL_CLI	<		M00_AXI_wlast M00_AXI_wstrb[63:0]	M00_AXI_wlast M00_AXI_wstrb(63:0)
CONTROL_RESE	T CONTROL_RESET	т		M00_AXI_wvalid M01_AXI_araddr[33:0]	M00_AXI_wvalid M01_AXI_araddr[33:0]
DATA_RESE	T DATA_RESET	т		M01_AXI_arburst[1:0]	M01_AXI_arburst[1:0]
KERNEL_CLK KERNEL_RESET		+		M01_AXI_arcache[3:0] M01_AXI_arid[3:0]	M01_AXI_arcache[3:0 M01_AXI_arid[3:0]
M00_AXI_arread		т-		M01_AXI_arlen[7:0] M01_AXI_arlock	M01_AXI_arlen[7:0] M01_AXI_arlock
M00_AXI_bid[3:	M00_AXI_bid[3:0	9		M01_AXI_arprot[2:0]	M01_AXI_arprot[2:0]
M00_AXI_bresp[1: M00_AXI_bval	d M00_AXI_bvalid	d		M01_AXI_arqos[3:0] M01_AXI_arsize[2:0]	M01_AXI_argos[3:0] M01_AXI_arsize[2:0]
M00_AXI_rdata[511: M00_AXI_rid[3:				M01_AXI_arvalid M01_AXI_awaddr[33:0]	M01_AXI_arvalid M01_AXI_awaddr[33:0
M00_AXI_rla M00_AXI_rresp[1:	st M00_AXI_rlas	ıt _		M01_AXI_awburst[1:0]	M01_AXI_awburst[1:0] M01_AXI_awcache[3:0
M00_AXI_rval	d M00_AXI_rvalid	d		M01_AXI_awid[3:0] M01_AXI_awid[3:0]	M01_AXI_awid[3:0]
M00_AXI_wread				M01_AXI_awlen[7:0] M01_AXI_awlock	M01_AXI_awlen[7:0] M01_AXI_awlock
M01_AXI_awread M01_AXI_bid[3:				M01_AXI_awprot[2:0] M01_AXI_awqos[3:0]	M01_AXI_awprot[2:0] M01_AXI_awqos[3:0]
M01_AXI_bresp[1:	0] M01_AXI_bresp[1:0	1		M01_AXI_awsize[2:0]	M01_AXI_awsize[2:0]
M01_AXI_bval M01_AXI_rdata[511:	M01_AXI_rdata[511:0	1		M01_AXI_awvalid M01_AXI_bready	M01_AXI_awvalid M01_AXI_bready
M01_AXI_rid[3: M01_AXI_rla				M01_AXI_rready M01_AXI_wdata[511:0]	M01_AXI_rready M01_AXI_wdata[511:0
M01_AXI_rresp[1: M01_AXI_rval	) M01_AXI_rresp[1:0	0		M01_AXI_wlast M01_AXI_wstrb[63:0]	M01_AXI_wlast M01_AXI_wstrb[63:0]
M01_AXI_wread	y M01_AXI_wread	у		M01_AXI_wvalid	M01_AXI_wvalid
M02_AXI_arreac		T		M02_AXI_araddr[33:0] M02_AXI_arburst[1:0]	M02_AXI_araddr[33:0 M02_AXI_arburst[1:0]
M02_AXI_bid[3: M02_AXI_bresp[1:		_		M02_AXI_arcache[3:0] M02_AXI_arid[3:0]	M02_AXI_arcache[3:0 M02_AXI_arid[3:0]
M02_AXI_bval	d M02_AXI_bvalis	_		M02_AXI_arlen[7:0]	M02_AXI_arlen[7:0]
M02_AXI_rdata[511: M02_AXI_rid[3:		9		M02_AXI_arlock M02_AXI_arprot[2:0]	M02_AXI_arlock M02_AXI_arprot[2:0]
M02_AXI_rla M02_AXI_rresp[1:		1		M02_AXI_argos[3:0] M02_AXI_arsize[2:0]	M02_AXI_argos[3:0] M02_AXI_arsize[2:0]
M02_AXI_rval	d M02_AXI_rvalis	+		M02_AXI_arvalid M02_AXI_awaddr[33:0]	M02_AXI_arvalid M02_AXI_awaddr[33:0
M03_AXI_arreac	y M03_AXI_arread	у		M02_AXI_awburst[1:0]	M02_AXI_awburst[1:0]
M03_AXI_awread M03_AXI_bid[3:				M02_AXI_awcache[3:0] M02_AXI_awid[3:0]	M02_AXI_awcache[3:0 M02_AXI_awid[3:0]
M03_AXI_bresp[1: M03_AXI_bval				M02_AXI_awlen[7:0] M02_AXI_awlock	M02_AXI_awlen[7:0] M02_AXI_awlock
M03_AXI_rdata[511: M03_AXI_rid[3:	M03_AXI_rdata(511:0	1		M02_AXI_awprot[2:0]	M02_AXI_awprot[2:0] M02_AXI_awqos[3:0]
M03_AXI_rla	M03_AXI_rlas			M02_AXI_awqos[3:0] M02_AXI_awsize[2:0]	M02_AXI_awsize[2:0]
M03_AXI_rresp[1: M03_AXI_rval				M02_AXI_awvalid M02_AXI_bready	M02_AXI_awvalid M02_AXI_bready
M03_AXI_wread S_AXI_araddr[16:				M02_AXI_rready M02_AXI_wdata[611:0]	M02_AXI_rready M02_AXI_wdata[511:0
S_AXI_arprot[2:	S_AXI_arprot[2:0	1		M02_AXI_wlast	M02_AXI_wlast
S_AXI_argos[3: S_AXI_arval				M02_AXI_wstrb[63:0] M02_AXI_wvalid	M02_AXI_wstrb[63:0] M02_AXI_wvalid
S_AXI_awaddr[16: S_AXI_awprot[2:		+		M03_AXI_araddr[33:0] M03_AXI_arburst[1:0]	M03_AXI_araddr[33:0 M03_AXI_arburst[1:0]
S_AXI_awqos[3:	S_AXI_awqos[3:0	1		M03_AXI_arcache[3:0]	M03_AXI_arcache[3:0] M03_AXI_arid[3:0]
S_AXI_awval	y S_AXI_bread	у		M03_AXI_arid[3:0] M03_AXI_arlen[7:0]	M03_AXI_arlen[7:0]
S_AXI_rread S_AXI_wdata(31:				M03_AXI_arlock M03_AXI_arprot[2:0]	M03_AXI_arlock M03_AXI_arprot(2:0)
S_AXI_wstrb[3: S_AXI_wvai	S_AXI_wstrb[3:0	1		M03_AXI_arqos[3:0] M03_AXI_arsize[2:0]	M03_AXI_argos[3:0] M03_AXI_arsize[2:0]
J_AAL_WVai	- S_AXI_wvalid	Ť		M03_AXI_arvalid	M03_AXI_arvalid
				M03_AXI_awaddr[33:0] M03_AXI_awburst[1:0]	M03_AXI_awaddr[33:0 M03_AXI_awburst[1:0
				M03_AXI_awcache[3:0] M03_AXI_awid[3:0]	M03_AXI_awcache[3:0]
				M03_AXI_awlen[7:0]	M03_AXI_awlen[7:0]
				M03_AXI_awlock M03_AXI_awprot[2:0]	M03_AXI_awlock M03_AXI_awprot[2:0]
				M03_AXI_awqos[3:0] M03_AXI_awsize[2:0]	M03_AXI_awqos[3:0] M03_AXI_awsize[2:0]
				M03_AXI_awvalid	M03_AXI_awvalid
				M03_AXI_bready M03_AXI_rready	M03_AXI_bready M03_AXI_rready
				M03_AXI_wdata[611:0] M03_AXI_wlast	M03_AXI_wdata[511:0 M03_AXI_wlast
				M03_AXI_wstrb[63:0]	M03_AXI_wstrb[63:0] M03_AXI_wvalid
				M03_AXI_wvalid S_AXI_arready	S_AXI_arready
				S_AXI_awready S_AXI_bresp[1:0]	S_AXI_awready S_AXI_bresp(1:0)
				S_AXI_bvalid S_AXI_rdata[31:0]	S_AXI_bvalid S_AXI_rdata[31:0]
				0_PLAI_(Udid[31:U]	
				S_AXI_rresp[1:0]	S_AXI_rresp[1:0]
				S_AXI_rresp[1:0] S_AXI_rvalid S_AXI_wready	S_AXI_rresp[1:0] S_AXI_rvalid S_AXI_wready
			lesign_u_ocl_region_0bd_2 cl_design_u_ocl_region_0	S_AXI_vready S_AXI_wready	S_AXI_rvalid