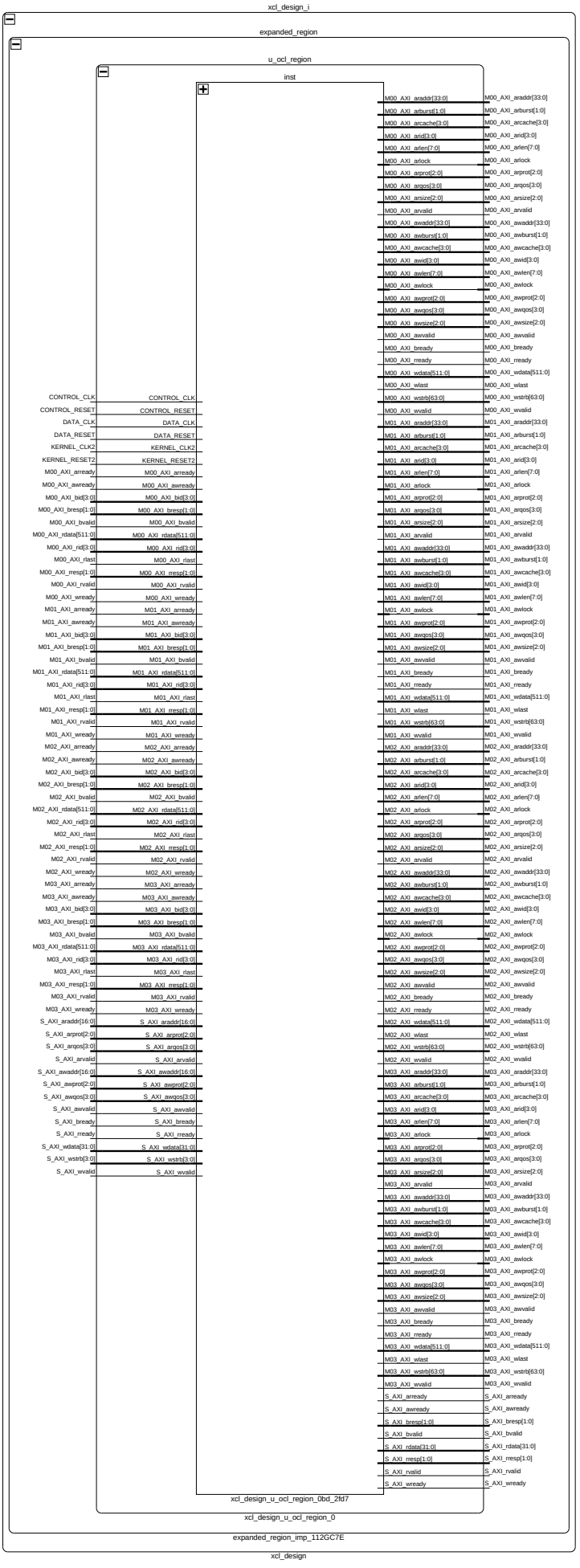
xcl_design_i
expanded_region
u_ocl_region
inst
CONTROL_CLK
CONTROL_RESET
DATA_CLK
DATA_RESET
KERNEL_CLK2
KERNEL_RESET2
M00_AXI_arready
M00_AXI_awready
M00_AXI_bid[3:0]
M00_AXI_bresp[1:0]
M00_AXI_bvalid
M00_AXI_rdata[511:0]
M00_AXI_rid[3:0]
M00_AXI_rlast
M00_AXI_rresp[1:0]
M00_AXI_rvalid
M00_AXI_wready
M01_AXI_arready
M01_AXI_awready
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M02_AXI_awready
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M02_AXI_bvalid
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M03_AXI_arready
M03_AXI_awready
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M03_AXI_bresp[1:0]
M03_AXI_bvalid
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M03_AXI_rresp[1:0]
M03_AXI_rvalid
M03_AXI_wready
S_AXI_araddr[16:0]
S_AXI_arprot[2:0]
S_AXI_arqos[3:0]
S_AXI_arvalid
S_AXI_awaddr[16:0]
S_AXI_awprot[2:0]
S_AXI_awqos[3:0]
S_AXI_awvalid
S_AXI_bready
S_AXI_rready
S_AXI_wdata[31:0]
S_AXI_wstrb[3:0]
S_AXI_wvalid
CONTROL_CLK
CONTROL_RESET
DATA_CLK
DATA_RESET
KERNEL_CLK2
KERNEL_RESET2
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M00_AXI_awready
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S_AXI_rready
S_AXI_wdata[31:0]
S_AXI_wstrb[3:0]
S_AXI_wvalid
xcl_design_u_ocl_region_0bd_2fd7
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M00_AXI_arcache[3:0]
M00_AXI_arid[3:0]
M00_AXI_arlen[7:0]
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M00_AXI_arprot[2:0]
M00_AXI_arqos[3:0]
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M00_AXI_awlen[7:0]
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M00_AXI_awprot[2:0]
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M00_AXI_awsize[2:0]
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M00_AXI_rready
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M00_AXI_wstrb[63:0]
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expanded_region_imp_112GC7E
xcl_design