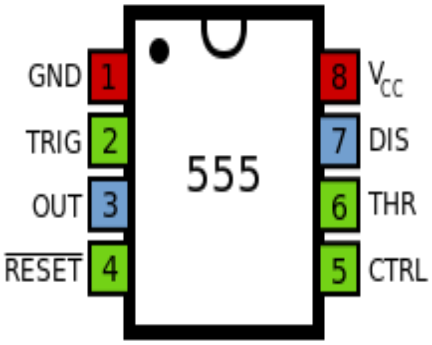
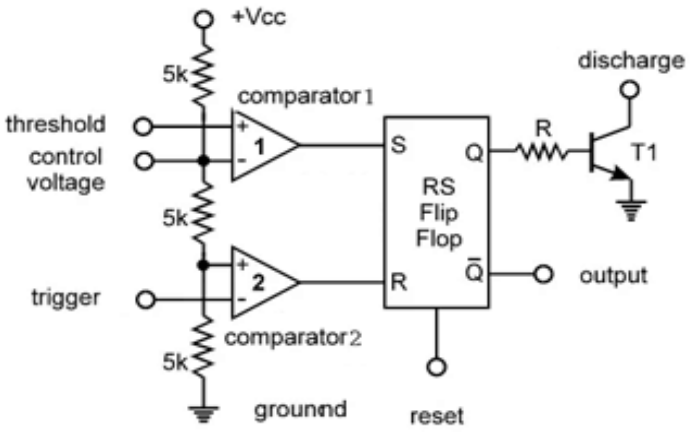
555 TIMER IC

The **555 timer IC** is an integrated circuit (chip) used in a variety of timer, pulse generation, and oscillator applications. The 555 can be used to provide time delays, as an oscillator, and as a flip-flop element



PIN STRUCTURE



INTERNAL STRUCTURE

Pin	Name	Purpose
1	GND	Ground reference voltage, low level (0 V)
2	TRIG	The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 1/3 V_{CC}, CTRL being 2/3 V_{CC} by default if CTRL is left open).
3	OUT	This output is driven to approximately 1.7 V below +Vcc , or to GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides THR.
5	CTRL	Provides "control" access to the internal voltage divider (by default, 2/3 V_{CC}).

6	THR	The timing (OUT high) interval ends when the voltage at THR ("threshold") is greater than that at CTRL (2/3 V_{CC} if CTRL is open).
7	DIS	Open Collector output which may discharge a capacitor between intervals. In phase with output.
8	V_{CC}	Positive supply voltage, which is usually between 3 and 15 V depending on the variation.

Detailed functions of various pins are as follows:

Pin 1. GROUND: This pin is connected to the ground. For the timer to function, this pin must and should be connected to ground. All voltages are measured with respect to this terminal.

Pin 2. TRIGGER: This pin is an inverting input the comparator 2 which is responsible for transition of flip flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied.

Pin 3. OUTPUT: Output of the timer is available at this pin. This pin is drawn from PUSH-PULL configuration formed by transistors.

There are two ways in which a load can be connected to the output terminal either between pin 3 and ground pin (pin 1) - called ***normally off load*** or between pin 3 and supply pin (pin 8) - called ***normally on load.***

Pin 4. RESET: To disable or reset the timer a negative pulse is applied to this pin due to the fact it is referred to as reset terminal. When this pin is not to be used for reset purpose, it should be connected to + VCC to avoid any possibility of false triggering_.

Pin 5: Control Voltage Terminal: The function of this terminal is to control the threshold and trigger levels. Thus either the external voltage or a pot connected to this pin determines the pulse width of the output waveform. The control pin is connected from the negative input pin of comparator 1.

When this pin is not used, it should be connected to ground through a 0.01 micro Farad to avoid any noise problem.

Pin 6: Threshold Terminal: This is the non-inverting input terminal of comparator 1, which compares the voltage applied to the terminal with a reference voltage of 2/3 VCC. The amplitude of voltage applied to this terminal is responsible for the set state of _flip-flop.

Pin 7: Discharge Terminal: This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal and ground. It is called discharge terminal because when transistor saturates, capacitor discharges through the transistor. The capacitor charges at a rate determined by the external resistor and capacitor, when the transistor is cut-off.

Pin 8: Supply Terminal: A supply voltage of + 5 V to + 18 V is applied to this terminal with respect to ground (pin 1).

CONSTUCTION

As we can see through the internal diagram the three resistors in the internal resistors are of 5 k each giving the IC name 555 Timer. A 555 timer has two comparators, which are basically 2 op-amps), an R-S flip-flop, two transistors and a resistive network.
Resistive network consists of three equal resistors and acts as a voltage divider.
Comparator 1 compares threshold voltage with a reference voltage + 2/3 VCC volts.
Comparator 2 compares the trigger voltage with a reference voltage + 1/3 VCC volts.
Output of both the comparators is supplied to the flip-flop. Flip-flop assumes its state according to the output of the two compa-rators. One of the two transistors is a discharge transistor of which collector is connected to pin 7. This tran-sistor saturates or cuts-off according to the output state of the flip-flop. The saturated transis-tor provides a discharge path to a capacitor con-nected externally. Base of another transistor is connected to a reset terminal. A pulse applied to this terminal resets the whole timer irrespective of any input.

WORKING PRINCIPLE

The internal resistors act as a voltage divider network, providing (2/3)Vcc at the non-inverting terminal of the upper comparator and (1/3)Vcc at the inverting terminal of the lower comparator. In most applications, the control input is not used, so that the control voltage equals +(2/3) VCC. Upper comparator has a threshold input (pin 6) and a control input (pin 5). Output of the upper comparator is applied to set (S) input of the flip-flop. Whenever the threshold voltage exceeds the control voltage, the upper comparator will set the flip-flop and its output is high. A high output from the flip-flop when given to the base of the discharge transistor saturates it and thus discharges the transistor that is connected externally to the discharge pin 7. The complementary signal out of the flip-flop goes to pin 3, the output. The output available at pin 3 is low. These conditions will prevail until lower comparator triggers the flip-flop. Even if the voltage at the threshold input falls below (2/3)

VCC, that is upper comparator cannot cause the flip-flop to change again. It means that the upper comparator can only force the flip-flop's output high.

To change the output of flip-flop to low, the voltage at the trigger input must fall below + (1/3) Vcc. When this occurs, lower comparator triggers the flip-flop, forcing its output low. The low output from the flip-flop turns the discharge transistor off and forces the power amplifier to output a high. These conditions will continue independent of the voltage on the trigger input. Lower comparator can only cause the flip-flop to output low.

From the above discussion it is concluded that for the having low output from the timer 555, the voltage on the threshold input must exceed the control voltage or + (2/3) VCC. This also turns the discharge transistor on. To force the output from the timer high, the voltage on the trigger input must drop below +(1/3) VCC. This turns the discharge transistor off.

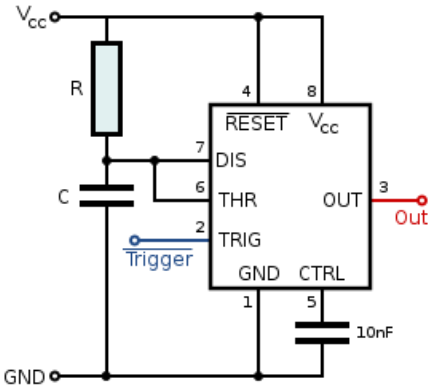
A voltage may be applied to the control input to change the levels at which the switching occurs. When not in use, a 0.01 nano Farad capacitor should be connected between pin 5 and ground to prevent noise coupled onto this pin from causing false tri

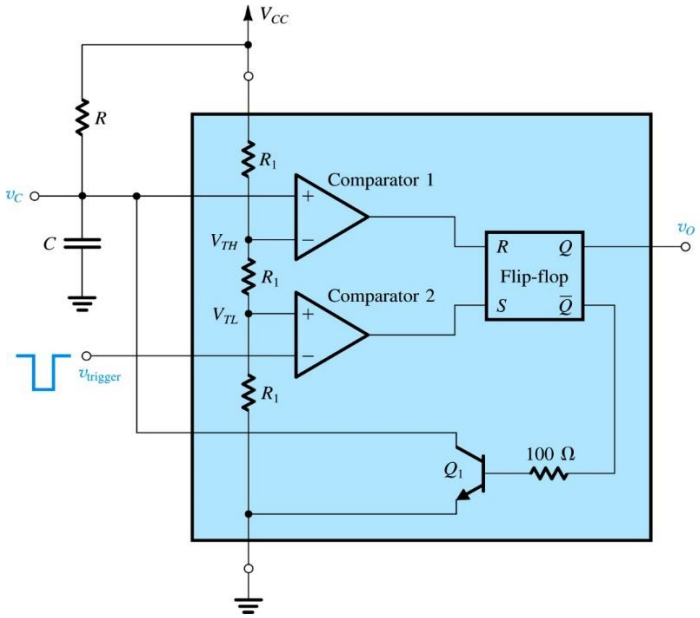
Connecting the reset (pin 4) to a logic low will place a high on the output of flip-flop. The discharge transistor will go on and the power amplifier will output a low. This condition will continue until reset is taken high. This allows synchronization or resetting of the circuit's operation. When not in use, reset should be tied to +VCC.

The IC 555 has three operating modes:

1) Monostable Mode

Monostable Multivibrator has one stable state and it switches to unstable state known as Quasi state for a time period T when it is triggered. The time period T is determined by the RC time constant in the circuit. Monostable mode of 555 timer is commonly used for generate Pulse width modulated waves.





Schematic view **Internal view**

The internal view doesn't contain pin for Reset and control as is not used here but reset pin is connected to Vcc and control is grounded via capacitor as seen in schematic view.

Working

The stable state of the monostable mode depicts that the flip flop is in reset sate indicating that the output q is low and its inverting output is high which turns the transistor q1 and q1 remains in saturation region giving output at comparator 1 low as well as trigger is first connected to Vcc giving low at comparator 2.

Now when a negative pulse (with respect to V_{TL} is applied to the Trigger pin of 555 Timer, output of lower comparator will become HIGH and will set the flip flop making the output q high and inverted output q low thus turning off the transistor and now in turn capacitor starts charging up through resistor R and its voltage Vc rises exponentially towards Vcc and this state is called the quasi stable state. now this sate prevails until Vc

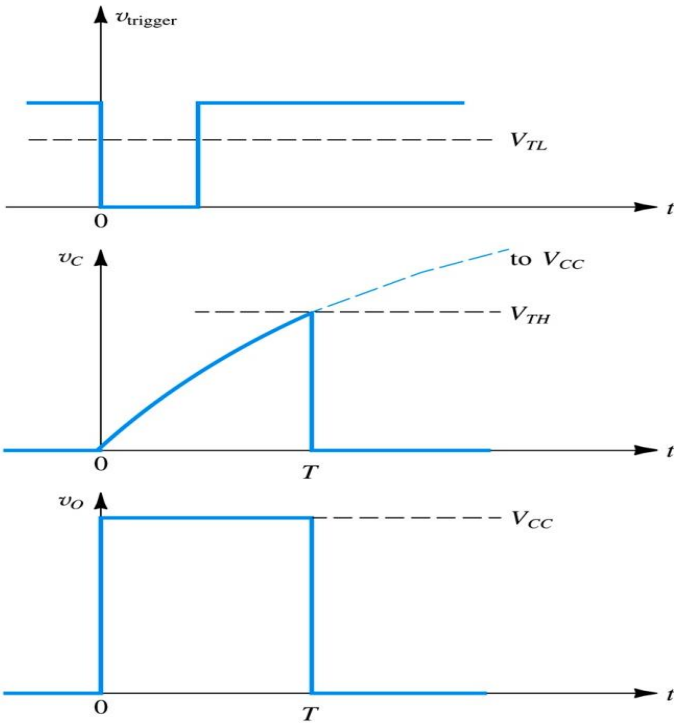
(the capacitor voltage) and begins to exceed , the threshold of comparator 1 V_{TH} i.e 2/3 Vcc at which the output of comparator goes high thus again resetting the flipflopand turning on the transistor which discharges the capacitor rapidly and thus Vc reaches zero again and in this way the monostable multi vibrator is again in its stable state and wil remain till the triggered button is positive .

Now the time for quai stable state is dependent on the resisitor R and the capacitor C.

As Vc = Vcc(1- e(-t/CR))

And as Vc = V_{TH}

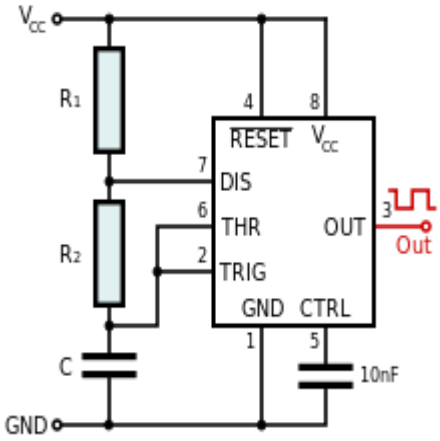
it leads that T (time period) = 1.1CR



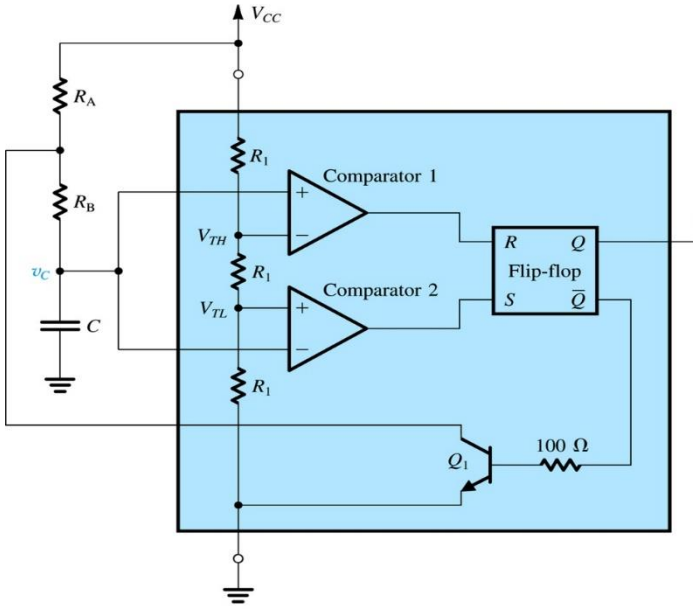
1) Astable Mode

The astable multivibrator generates a square wave. The astable multivibrator does not require any external trigger to change the state of the output. Therefore it is also known as oscillator. The time during which the output is either high or low is determined by the two resistors and a capacitor which are connected to the 555 timer.

The internal view doesn't contain pin for Reset and control as is not used here but reset pin is connected to Vcc and control is grounded via capacitor as seen in schematic view.



Schematic view



Internal view

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Working

As there is no stable state in the astable mode . it employs two resistor R1 and R2 as well as a capacitor C which decides operation . Assume that initially capacitor is discharged and flip flop is set and q is high whereas inverted output is low and thus transistor is off.Now C will charge up through the series combination of R1 and R2 and the voltage Vc will rise exponentially towards Vcc till it's equal to V_{TL} the output of comparatror gets low however this does not affect the ckt operation and flip flop remains set and it remains set till it crosses V_{TH} which makes the comparator output high and thus resets the flip flop.now output q is low but inverted output is one , turni8ng on the transistorwhich makes zero votage across the common node of R1 and R2 and then the capacitor starts discharging vis resistor R2 and the collector of Q1. Now Vc decreases exponentially towards zero and when it reaches V_{TL} and thus giving high at comparator 2 and setting the flip flop and giving high output and again the same procedure continues as transistor q1 is off again.this gives rise to the square wave.

Now Vc for charging can be described as

$$Vc = Vcc - (Vcc - V_{TL})\exp(-t/C(R1+R2)$$

Now for charging time Vc= V_{TH} =2/3Vcc and V_{TL} =1/3Vcc

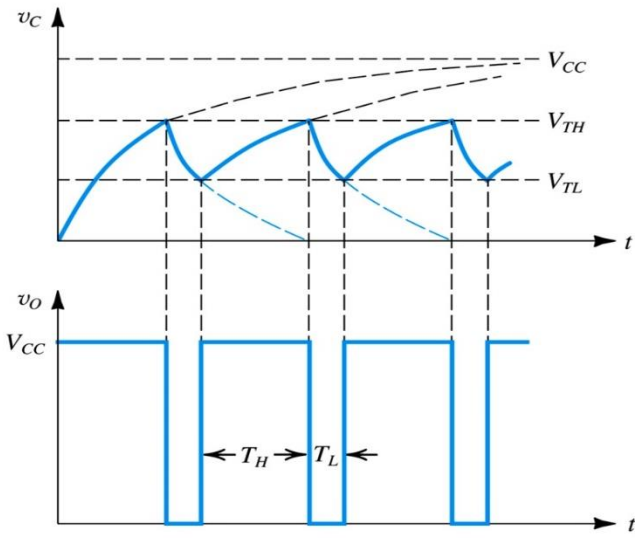
Which gives time $T_H = 0.69C(R1+R2)$

Similarly , Now Vc for discharging can be described as

$V_c = V_{TH} \exp(-t/CR2)$

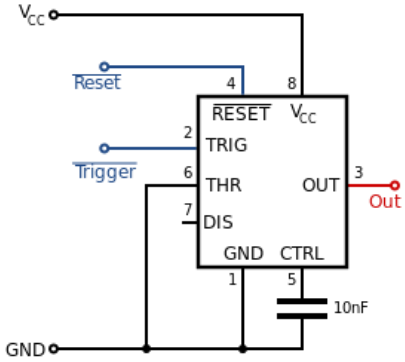
Substituting $V_c = V_{TL} = 1/3Vcc$ and $V_{TH} = 2/3Vcc$

$T_L = 0.69CR2$

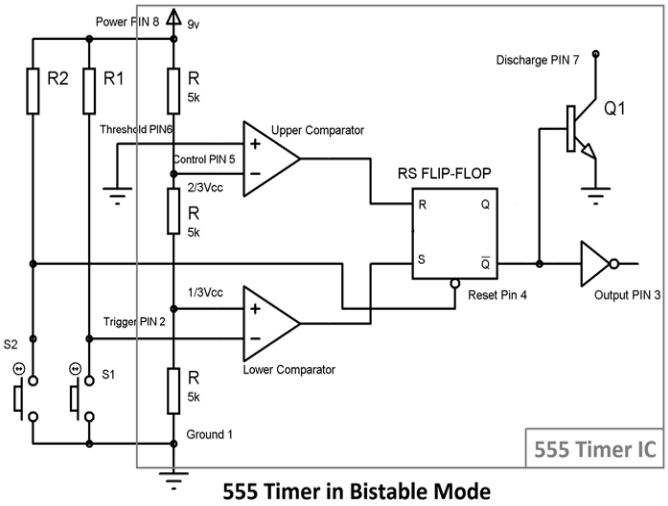


2) BISTABLE MODE

A Bistable multivibrator is a type of circuit which has two stable states (high and low). It stays in the same state until and unless an external trigger input is applied. Bistable multi vibrators are also called as flip-flops or latches. The term flip-flop is used because it 'flips' to one state and stays there until a trigger is applied and once the trigger is applied it 'flops' back to the original state.



Schematic view



555 Timer in Bistable Mode

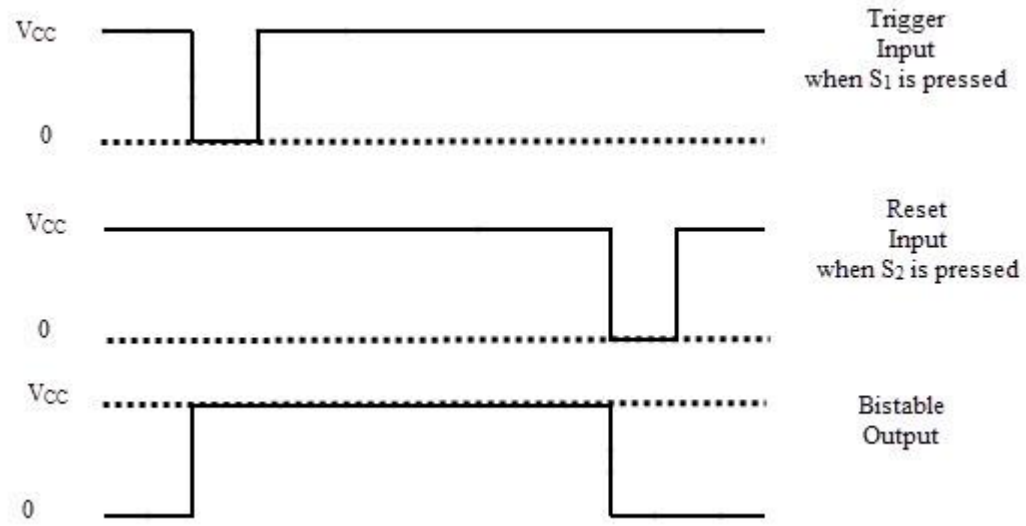
Internal view

A bistable multivibrator is one of the easiest circuits that can be built using a 555 timer. It doesn't require a capacitor as the RC charging unit is not responsible for the generation of the output. The generation of high and low outputs is controlled by the external trigger and reset signals.

The explanation of the bistable mode of operation of the 555 timer is as follows. The trigger and reset pins (pins 2 and 4) are connected to the supply through two resistors R1 and R2. Two switches are connected between these pins and ground in order to make them go low. The switch at the trigger input will act as SET input for the internal flip-flop. The switch at the reset input will act as reset for the internal flip-flop.

When the switch S1 is pressed, the voltage from VCC will bypass the trigger terminal and is shorted to ground through R1. Hence, the trigger pulse will momentarily go low and the output of the timer at pin 3 will become HIGH. The output stays HIGH because there is no input from the threshold pin 6 and the output of the internal comparator (comparator 1) will not go high.

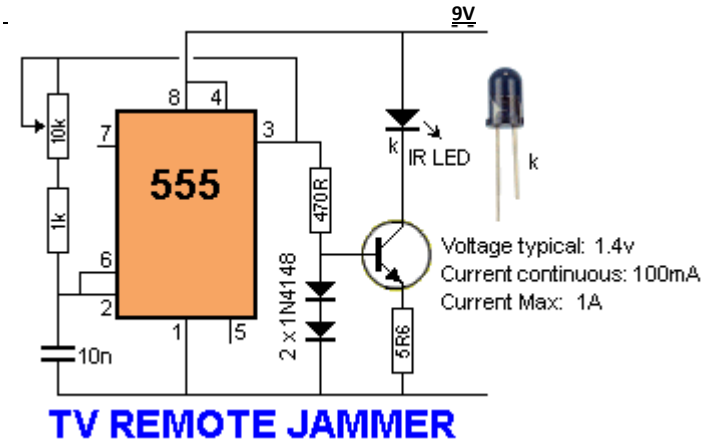
When the switch S2 is pressed, the voltage from VCC will bypass the reset terminal and is shorted to ground through the resistor R2. This pin is internally connected to the RESET terminal of the flip-flop. When this signal goes low for a moment, the flip-flop receives the reset signal and RESETs the flip-flop. Hence, the output will become LOW. The waveforms of the bistable mode of operation of the 555 timer are shown below.



555 Timer IC has various applications some of which are :-

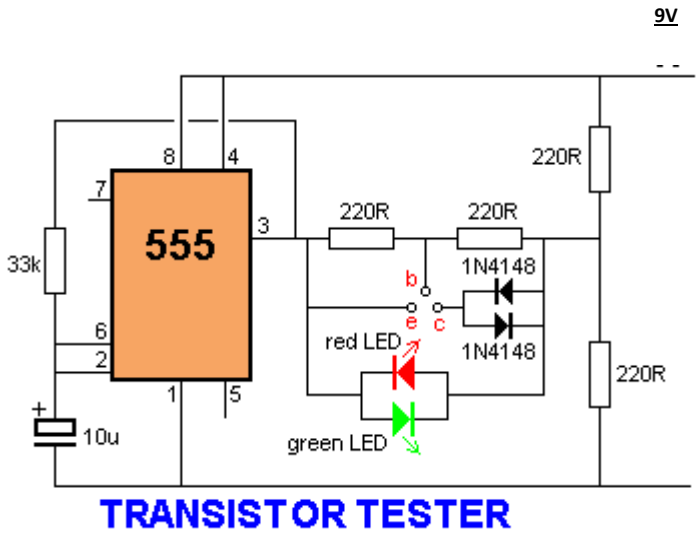
1) TV remote Jammer
2) Transistor Tester
3) Traffic Light

1) TV Remote Jammer



This circuit confuses the infra-red receiver in a TV. It produces a constant signal that interferes with the signal from a remote control and prevents the TV detecting a channel-change or any other command. This allows you to watch your own program without anyone changing the channel !! The circuit is adjusted to produce a 38kHz signal. The IR diode is called an Infra-red transmitting Diode or IR emitter diode to distinguish it from a receiving diode, called an IR receiver or IR receiving diode.. There are so many IR emitters that we cannot put a generic number on the circuit to represent the type of diode. Some types include: CY85G, LD271, CQY37N (45), INF3850, INF3880, INF3940 (30). The current through the IR LED is limited to 100mA by the inclusion of the two 1N4148 diodes, as these form a constant-current arrangement when combined with the transistor and 5R6 resistor.

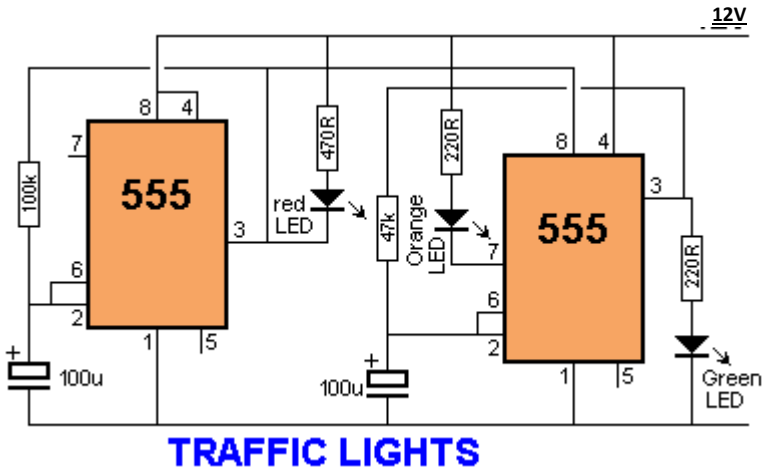
2) Transistor Tester



The 555 operates at 2Hz. Output pin 3 drives the circuit with a positive then zero voltage. The other end of the circuit is connected to a voltage divider with the mid-point at approx. 4.5v. This allows the red and green LEDs to alternately flash when no transistor is connected to the tester.

If a good transistor is connected, it will produce a short across the LED pair when the voltage is in one direction and only one LED will flash. If the transistor is open, both LED's will flash and if the transistor is shorted, neither LED will flash.

3) Traffic Light



This ckt uses two 555 IC's two implement a traffic light layout. The red LED has an equal on-off period and when it is off, the first 555 delivers power to the second 555. This illuminates the Green LED and then the second 555 changes state to turn off the Green LED and turn on the Orange LED for a short period of time before the first 555 changes state to turn off the second 555 and turn on the red LED. A supply voltage of 9v to 12v is needed because the second 555 receives a supply of about 2v less than rail. This circuit also shows how to connect LEDs high and low to a 555 and also turn off the 555 by controlling the supply to pin 8. Connecting the LEDs high and low to pin 3 will not work and since pin 7 is in phase with pin 3, it can be used to advantage in this design.