VLSI Assignment

In this assignment, you will design the hardware to implement the following function:

$$E = A / 2^{i} + B \times 2^{j}$$
$$F = E \times C$$

Where:

- A, B, C and E are 8-bit unsigned numbers
- i and j are 3-bit unsigned numbers.
- F is 16-bit unsigned number

Design Specification:

- Implement the design using Verilog language. Do not use the following math operations: -, +, ×, / , shift/rotate. You need to implement them yourself.
- The top design name is mydesign and the port definition is illustrated below. You must use the below testbench and template in your design.
- Use your own choice of multiplier algorithm to implement the multiplier.

Team and Report Rules:

- Teams: you must form a team of 2-3 students.
- Submission and DEMO:
    - What you should submit:
        - Code (Verilog files)
        - Report: which includes
            - the names of the students,
            - status of the code,
            - waveforms.
    - Submission deadline is: 8:00AM on Tuesday 26/12
    - DEMO:
        - Time: during the class of Tuesday 26/12 (9:30-10:30)
        - You will be assigned a time slot to show in the lab
        - You will be asked to explain and modify your code
- This assignment accounts for 15% of your grade. Cheating results in 0-grade.

The followings are the design template and testbench files.

mydesign.v

```
module mydesign
  (
  input  [7:0] A,
  input  [7:0] B,
  input  [7:0] C,
  input  [2:0] i,
  input  [2:0] j,
  output reg [15:0] F
  );

  /// Your Design

endmodule
```

mydesign_tb.v

```
`timescale 1ns/100ps
module mydesign_tb;
  reg    [7:0] A;
  reg    [7:0] B;
  reg    [7:0] C;
  reg    [2:0] i, j;
  wire   [15:0] F;

  // Mydesign one round in hardware
  mydesign mydesign (
  .A  (A),
  .B  (B),
  .C  (C),
  .i  (i),
  .j  (j),
  .F  (F)
  );

  initial begin
    $monitor (" (values are in HEX) A=%h   B=%h  C=%h   i=%h   j=%h   F=%h", A, B, C,
i, j,  F);

    A= 8'h06;   B=8'h06;   C=8'h06   ;   i=3'h1;   j=3'h1;
    #10;

    A= 8'h01;   B=8'h01;   C=8'h01   ;   i=3'h1;   j=3'h1;
    #10;

    A= 8'hFF;   B=8'hFF;   C=8'hFF   ;   i=3'h7;   j=3'h7;
    #10;

    A= 8'hFF;   B=8'hFF;   C=8'hFF   ;   i=3'h0;   j=3'h0;
    #10;

    $stop;
  end

endmodule
```

Correct Output

```
#  (values are in HEX) A=06   B=06  C=06   i=1   j=1   F=005a
#  (values are in HEX) A=01   B=01  C=01   i=1   j=1   F=0002
#  (values are in HEX) A=ff   B=ff  C=ff   i=7   j=7   F=807f
#  (values are in HEX) A=ff   B=ff  C=ff   i=0   j=0   F=fd02
```