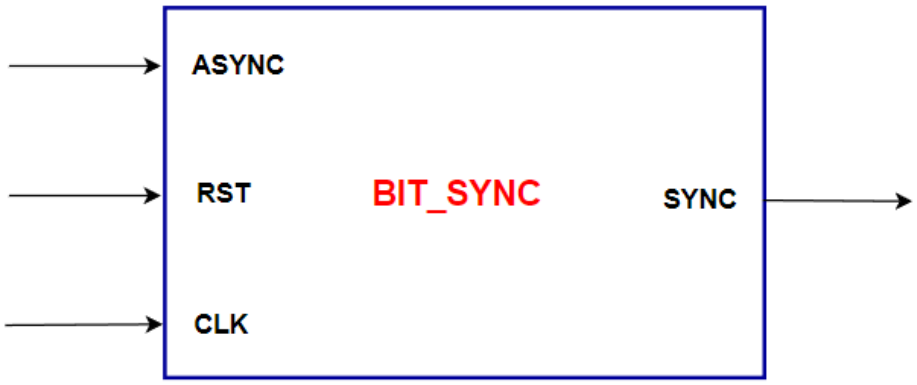
Bit Synchronizer

Introduction: -

Clock Domain Crossing (CDC) in digital domain is defined as the process of passing a signal or vector (multi bit signal) from one clock domain to another clock domain which introduce many issues as metastability, data incoherence and data loss. There are many techniques to synchronize asynchronous signals to avoid CDC issues as: -

- **Multi-Flop Synchronization Scheme**: Used to synchronize single bit or multiple bits encoded in gray code.

Block Interface



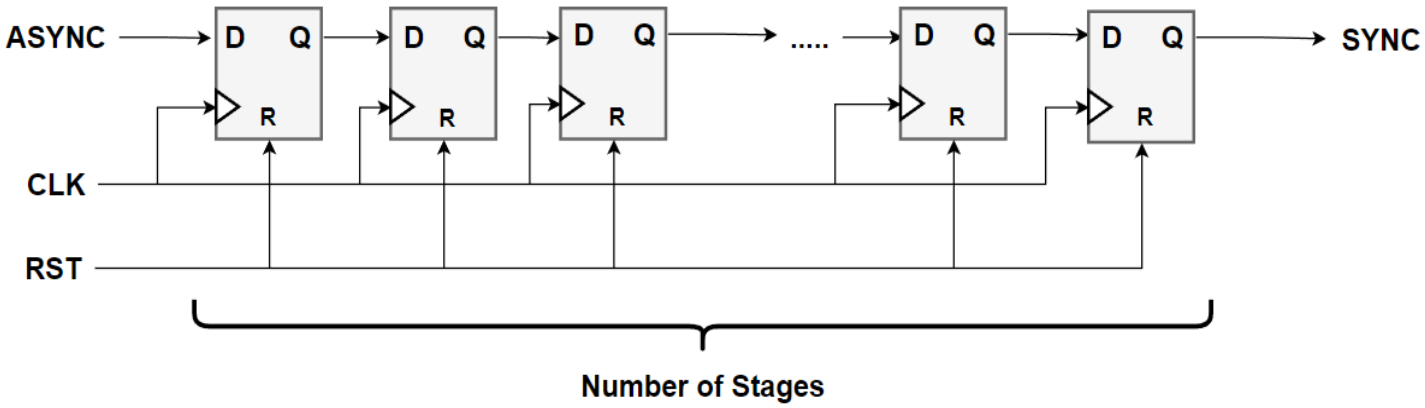
Ports Description

Signal Name	Description	Width
ASYNC	Unsynchronized bit/bus	**Parameterized (default = 1)**
CLK	Destination domain clock	**1**
RST	Destination domain Active Low Asynchronous Reset	**1**
SYNC	Synchronized bit/bus	**Parameterized (default = 1)**

Parameter Description

parameter Name	Description
NUM_STAGES	**Number of Flip Flop Stages**
BUS_WIDTH	**Width of synchronized signal**

Block Diagram



Hint: Number of stages is parameterized.

Required

1. Write a Verilog Code to capture the above block diagram.

2. Write a testbench to your synchronizer and validate the latency of your synchronized signal equals to FF stage or not