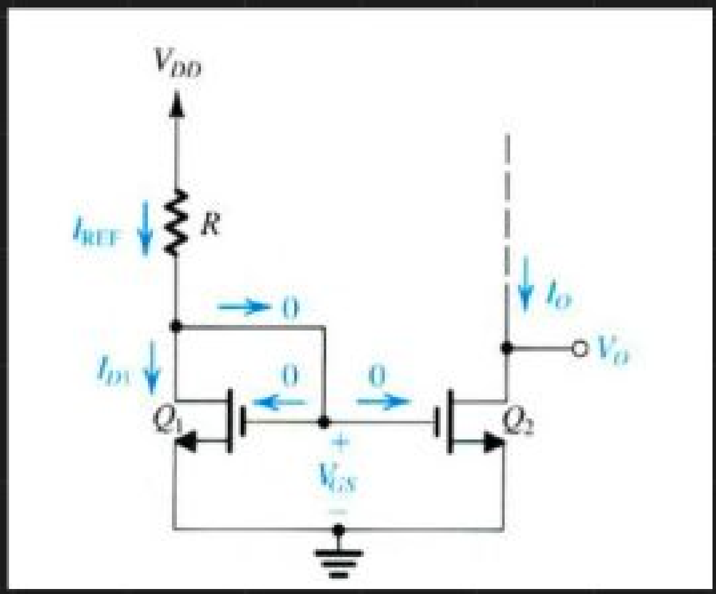
D 8.1 Using two matched MOS transistors with $W/L = 10$, $k_n' = 400\ \mu A/V^2$, and $V_{tn} = 0.5$ V, design the circuit in Fig. 8.1 to provide $I_O = 80\ \mu A$. Assume $V_{DD} = 1.8$ V and neglect the effect of channel-length modulation. Specify the value required for R and the minimum value that V_O can have while Q_2 still operates in saturation.



• $I_{ref} = I_o = 80\,\mu A = 0{,}08\ mA$

→ design : $R = ?$

∵ $V_{DD} - I_{ref} R - V_{GS} = 0$

∴ $1{,}8 - 0{,}08 R - V_{GS} = 0$ → ①

→ ∵ $I = \frac{1}{2} k_n' \left(\frac{W}{L}\right) (V_{ov})^2$

∴ $80\mu = \frac{1}{2} (400\mu)(10)(V_{ov})^2$

∴ $V_{ov} = 0{,}2v = V_{GS} - V_t$

∴ $V_{GS} = 0{,}2 + 0{,}5 = 0{,}7v$

→ ∴ ① → $1{,}8 - 0{,}08 R - 0{,}7 = 0$

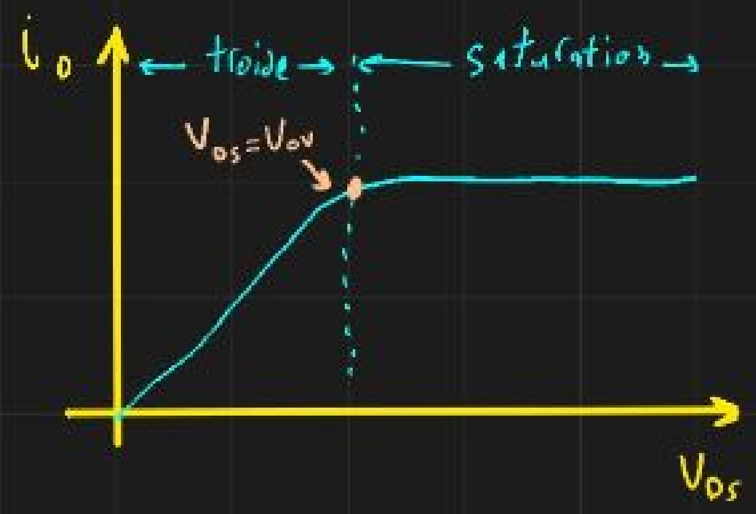
∴ $\boxed{R = 13{,}75\ K\Omega}$

→ $V_{o_{min}}$ while Q_2 in saturation

$V_{DS_{min}} = V_{ov} = 0{,}2v$

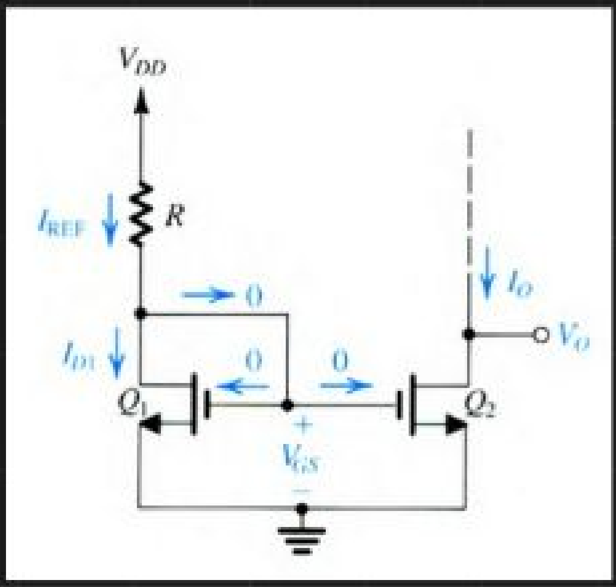
∵ $V_o = V_{DS}$

∴ $\boxed{V_{o_{min}} = 0{,}2v}$



VE 8.1

8.2 For $V_{DD} = 1.2$ V and using $I_{REF} = 10\ \mu A$, it is required to design the circuit of Fig. 8.1 to obtain an output current whose nominal value is 60 μA. Find R and W_2 if Q_1 and Q_2 have equal channel lengths of 0.4 μm, $W_1 = 1$ μm, $V_t = 0.4$ V, and $k_n' = 400\ \mu A/V^2$. What is the lowest possible value of V_O? Assuming that for this process technology, the Early voltage $V_A' = 6$ V/μm, find the output resistance of the current source. Also, find the change in output current resulting from a +0.2-V change in V_O.



$\cdot\ I_{ref} = 10\ \mu A = 0{,}01\ mA$, $I_o = 60\ \mu A = 0{,}06\ mA$, $W_2 = ?$ $R = ?$, $L_1 = L_2 = 0{,}4\ \mu m$, $W_1 = 1\ \mu m$

→ design: W_2? R?

→ $V_{DD} - I_{ref} R - V_{GS} = 0$

$\therefore 1{,}2 - 0{,}01 R - V_{GS} = 0 \rightarrow ①$

→ $I_{ref} = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_1 (V_{ov})^2$

$\therefore 10\ \mu = \frac{1}{2}(400\ \mu)\left(\frac{1}{0{,}4}\right)(V_{ov})^2$

$\therefore V_{ov} = 0{,}14\ v = V_{GS} - V_t$

$\therefore V_{GS} = 0{,}14 + 0{,}4 = 0{,}54\ v$

① → $1{,}2 - 0{,}01 R - 0{,}54 = 0$

$\therefore \boxed{R = 66\ K\Omega}$

$\because I_o = \frac{1}{2} k_n' \left(\frac{W}{L}\right)_2 (V_{ov})^2$

$\therefore 60\ \mu = \frac{1}{2}(400\ \mu)\left(\frac{W_2}{0{,}4}\right)(0{,}14)^2$

$\therefore \boxed{W_2 = 6.12\ \mu m}$

" or "

$\because \frac{I_o}{I_{ref}} = \frac{(W_2/L_2)}{(W_1/L_1)}$

$\therefore \frac{60}{10} = \frac{W_2}{1}$

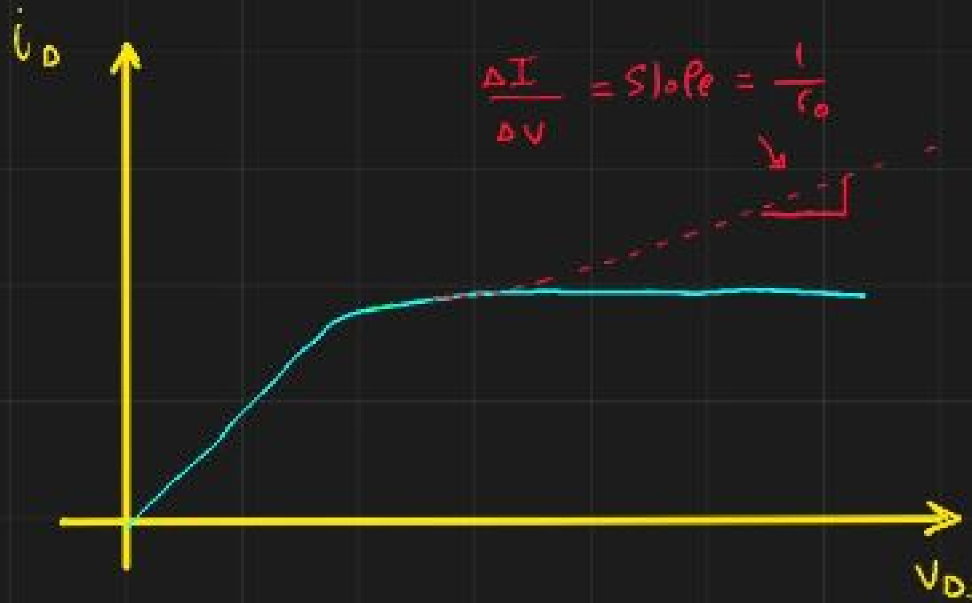
$\therefore \boxed{W_2 = 6\ \mu m}$

→ $r_o = ?$ $V_A' = 6\ v/\mu m$

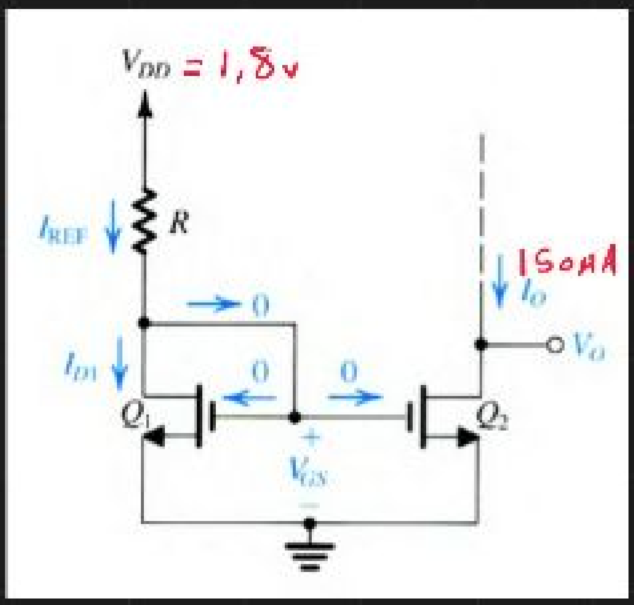
$r_o = \frac{V_A}{I_D} = \frac{V_A' L_2}{I_o} = \frac{6(0{,}4)}{0{,}06} \rightarrow \therefore \boxed{r_o = 40\ K\Omega}$

→ $\Delta I = ?$ when $\Delta V = 0{,}2\ v$

$\because \frac{\Delta I}{\Delta V} = \frac{1}{r_o} \rightarrow \therefore \frac{\Delta I}{0{,}2} = \frac{1}{40} \rightarrow \therefore \boxed{\Delta I = 5\ \mu A}$



D 8.3 Using $V_{DD} = 1.8$ V and a pair of matched MOSFETs, design the current-source circuit of Fig. 8.1 to provide an output current of 150-μA nominal value. To simplify matters, assume that the nominal value of the output current is obtained at $V_O \simeq V_{GS}$. The circuit must operate for V_O in the range of 0.3 V to V_{DD} and the change in I_O over this range must be limited to 10% of the nominal value of I_O. Find the required value of R and the device dimensions. For the fabrication-process technology used, $\mu_n C_{ox} = 400\ \mu A/V^2$, $V_A' = 10$ V/μm, and $V_t = 0.5$ V.



$I_o = 150\,\mu A = 0{,}15\,mA$ @ $V_o = V_{GS} = V_{D2}$ $0{,}3 < V_o < V_{DD}^{\,1{,}8}$ $\Delta I_o < \frac{10}{100}(150)$

$\Delta I_o < 15\,\mu A$

→ Design : R = ? W ? L ?

. $1{,}8 - I_{ref}\,R - V_{GS} = 0$ assume $Q_1 Q_2$ matched

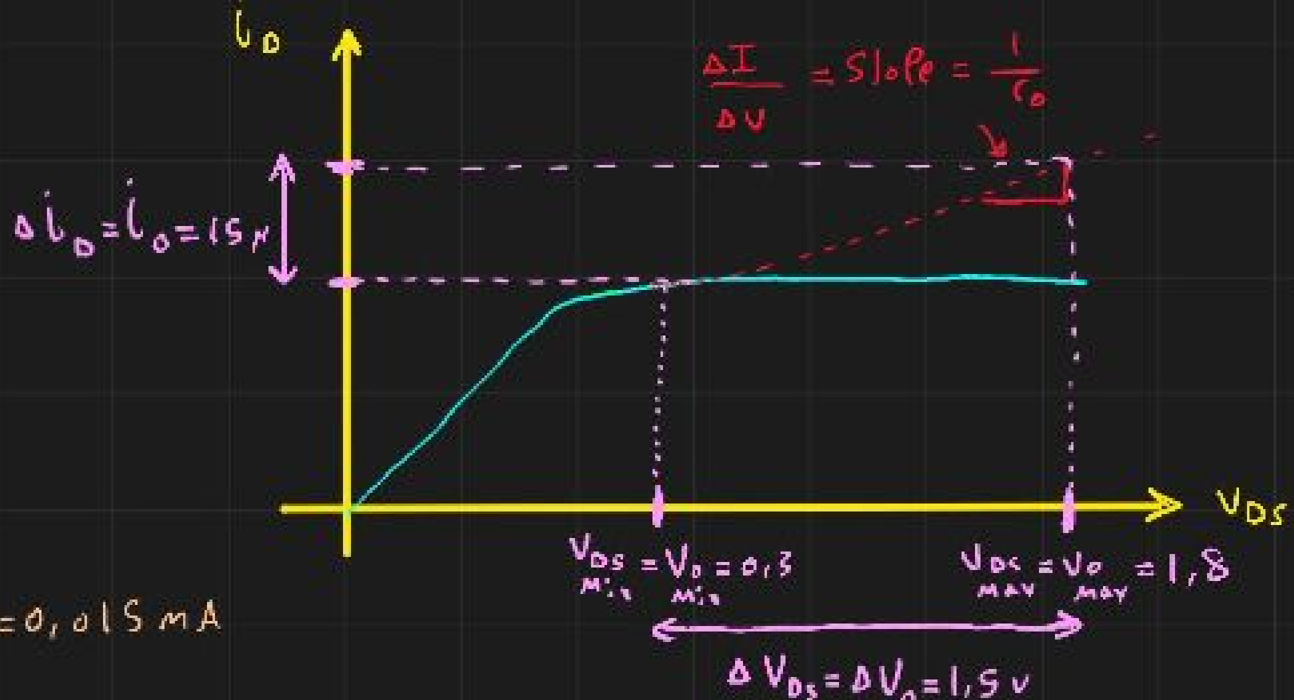
$\therefore 1{,}8 - 0{,}15\,R - V_{GS} = 0 \rightarrow (1)$

$\rightarrow I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right)(V_{ov})^2$

$\therefore 150 = \frac{1}{2}(400)\left(\frac{W}{L}\right)(V_{ov})^2 \rightarrow (2)$

$\rightarrow \because V_o = V_{DS}$, $\because V_{o\,min} = 0{,}3 \rightsquigarrow \therefore V_{DS\,min} = 0{,}3$

$\because V_{DS\,min} = V_{ov} \rightsquigarrow \therefore \boxed{V_{ov} = 0{,}3}$



$\rightarrow \because V_o = V_{DS} \rightsquigarrow \therefore 0{,}3 < V_{DS} < 1{,}8 \rightsquigarrow \therefore \Delta V_{DS} = 1{,}5\,v$

$\rightsquigarrow \Delta I_D = 15\,\mu A = 0{,}015\,mA$

$\because r_o = \frac{1}{\text{Slope}} = \frac{\Delta V_D}{\Delta i_D} \rightsquigarrow \therefore \boxed{r_o = \frac{1{,}5}{0{,}015} = 100\,k\Omega}$

$\rightarrow \because r_o = \frac{V_A}{I_o} = \frac{V_A' L_o}{I_o} \rightsquigarrow \therefore 100k = \frac{(10/\mu)(L_o)}{15\mu} \rightsquigarrow \therefore \boxed{L = 1{,}5\,\mu m}$

(2) $\rightarrow 150\mu = \frac{1}{2}(400\mu)\left(\frac{W}{1{,}5\mu}\right)(0{,}3)^2 \rightsquigarrow \therefore \boxed{W = 12{,}5\,\mu m}$

or more Practicly - including chaneel length effect:

$150\mu = \frac{1}{2}(400\mu)\left(\frac{W}{1{,}5\mu}\right)(0{,}3)^2(1 + \lambda V_{DS})$

$\because V_{DS} = V_{GS} = V_{ov} + V_t = 0{,}3 + 0{,}5 = 0{,}8\,v$

$\therefore \lambda = \frac{1}{V_A} = \frac{1}{V_A' \cdot L} = \frac{1}{10(1{,}5)} = \frac{1}{15}$

$\therefore 150\mu = \frac{1}{2}(400\mu)\left(\frac{W}{1{,}5\mu}\right)(0{,}3)^2\left(1 + \frac{0{,}8}{15}\right) \rightsquigarrow \therefore \boxed{W = 11{,}86\,\mu m}$

(1) $\rightarrow 1{,}8 - 0{,}15\,R - 0{,}8 = 0 \rightsquigarrow \therefore \boxed{R = 6{,}67\,k\Omega}$

8.6 For the current-steering circuit of Fig. P8.6, find I_O in terms of I_{REF} and device W/L ratios.

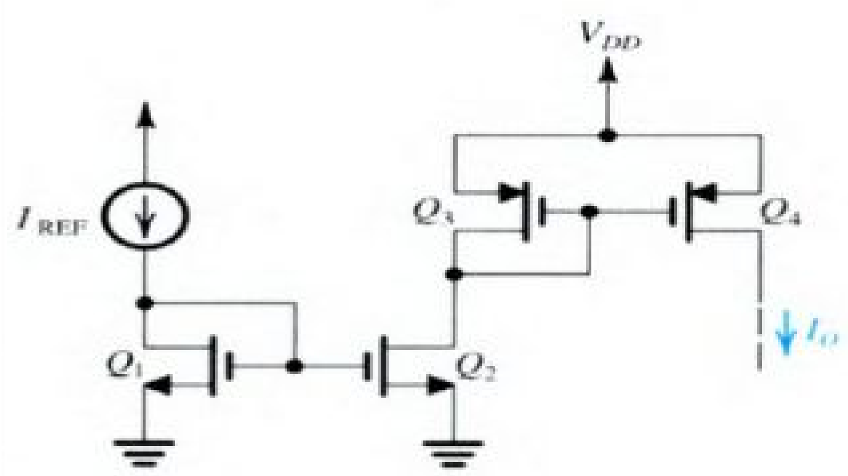


Figure P8.6

$$\because \frac{I_{D2}}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \longrightarrow ①$$

$$\because I_{D2} = I_{D3}$$

$$\therefore \frac{I_{D4}}{I_{D3}} = \frac{(W/L)_4}{(W/L)_3} = \frac{I_o}{I_{D2}} \longrightarrow ②$$

$$\therefore \frac{I_o}{\cancel{I_{D2}}} \cdot \frac{\cancel{I_{D2}}}{I_{ref}} = \frac{(W/L)_4}{(W/L)_3} \cdot \frac{(W/L)_2}{(W/L)_1} \rightsquigarrow \therefore \frac{I_o}{I_{ref}} = \frac{(W/L)_4}{(W/L)_3} \cdot \frac{(W/L)_2}{(W/L)_1}$$

D 8.7 The current-steering circuit of Fig. P8.7 is fabricated in a CMOS technology for which $\mu_n C_{ox} = 400\ \mu A/V^2$, $\mu_p C_{ox} = 100\ \mu A/V^2$, $V_{tn} = 0.5$ V, $V_{tp} = -0.5$ V, $V'_{An} = 6$ V/μm, and $|V'_{Ap}| = 6$ V/μm. If all devices have $L = 0.5$ μm, design the circuit so that $I_{REF} = 20\ \mu A$, $I_2 = 80\ \mu A$, $I_3 = I_4 = 50\ \mu A$, and $I_5 = 100\ \mu A$. Use the minimum possible device widths needed to operate the current source Q_2 with voltages at its drain as high as +0.8 V and to operate the current sink Q_5 with voltages at its drain as low as –0.8 V. Specify the widths of all devices and the value of R. Find the output resistance of the current source Q_2 and the output resistance of the current sink Q_5.

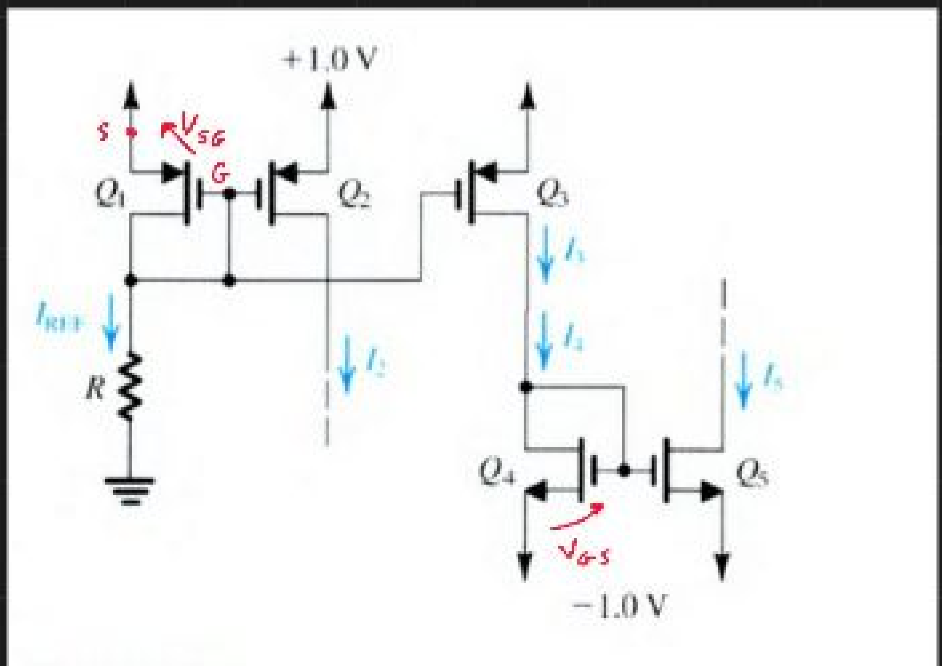


Figure P8.7

• $L_1 = L_2 = L_3 = L_4 = L = 0{,}5\ \mu m$, $I_{ref} = 20\ \mu A = 0{,}02\ mA$ $I_2 = 80\ \mu A = 0{,}08\ mA$ $I_3 = I_4 = 50\ \mu A = 0{,}05\ mA$

$I_5 = 100\ \mu A = 0{,}1\ mA$

• W?? @ Q_2 C.S $V_{d_2\,max} = 0{,}8$ Q_5 C-Sink $V_{d_5\,max} = -0{,}8$ V

→ $R = ?$ $W_{1\to 5} = ?$ r_{o_2} ? r_{o_5} ?

→ need to obtain V_{ov} from above conditions

• For PMOS $V_{SD\,min} = V_{ov}$ (Q_2)

$\because V_{SD} = V_S - V_D$

$\therefore V_{SD\,min} = 1 - 0{,}8 = 0{,}2$

$\therefore \boxed{V_{ov_2} = 0{,}2} = V_{ov_1} = V_{ov_3}$ (Same V_{GS})

(Q_5) NMOS $V_{DS\,min} = V_{ov}$

$\because V_{DS} = V_D - V_S$

$\therefore V_{DS\,min} = -0{,}8 - (-1) = 0{,}2$

$\therefore \boxed{V_{ov_5} = 0{,}2\ V} = V_{ov_4}$ (Same V_{GS})

$\therefore Q_1$:

$I_{D_1} = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_1 (V_{ov_1})^2$

$\therefore 20 = \frac{1}{2}(100\mu)\left(\frac{W_1}{0{,}5\mu}\right)(0{,}2)^2$

$\therefore \boxed{W_1 = 5\ \mu m}$

$\therefore Q_2$:

$\because \frac{I_2}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \rightarrow \therefore \frac{80}{20} = \frac{W_2}{5}$

$\therefore \boxed{W_2 = 20\ \mu m}$

$\therefore Q_3$:

$I_{D_3} = \frac{1}{2} k_p' \left(\frac{W}{L}\right)_3 (V_{ov_3})^2$

$\therefore 50\mu = \frac{1}{2}(100\mu)\left(\frac{W_3}{0{,}5\mu}\right)(0{,}2)^2$

$\therefore \boxed{W_3 = 12{,}5\ \mu m}$

Same for Q_4, Q_5

$R = ?$

$\rightarrow 1 - V_{SG} - I_{ref} R = 0$

$\because V_{SG} = V_{ov} + V_t$

$\therefore V_{SG} = 0{,}2 + (0{,}5)$

$\therefore V_{SG} = 0{,}7$

$\therefore \boxed{R = 15\ k\Omega}$

r_{o_2} ? r_{o_5} ?

$\rightarrow r_{o_2} = \frac{V_A}{I_2} = \frac{V_A' L}{I_2} = \frac{6(0{,}5)}{80\mu}$

$\therefore \boxed{r_{o_2} = 37{,}5\ k\Omega}$

Same for r_{o_5} ✓