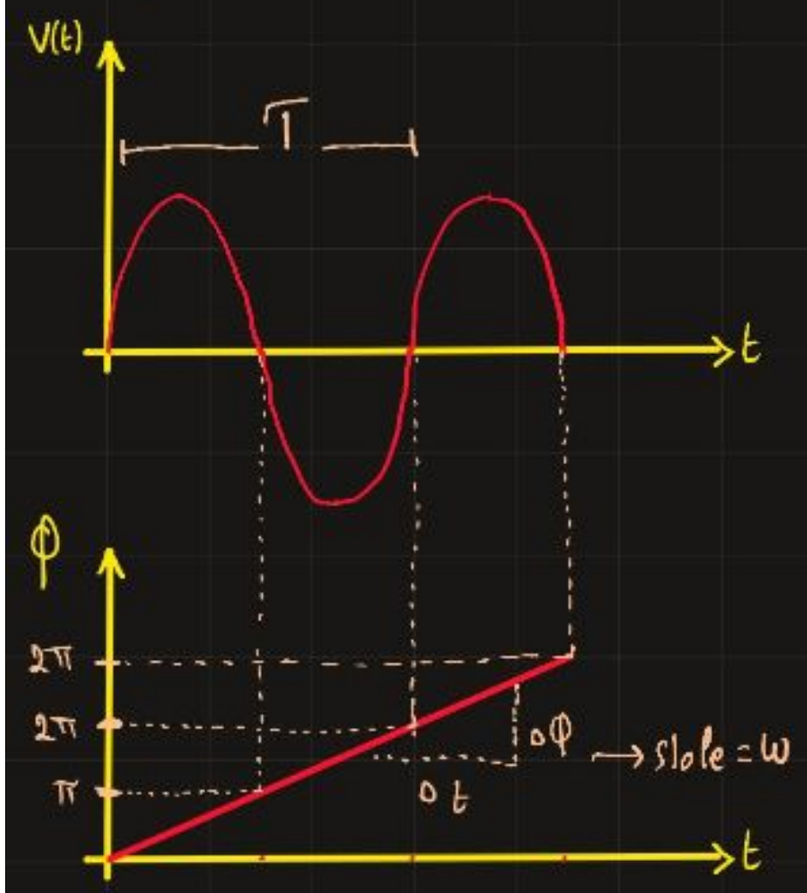
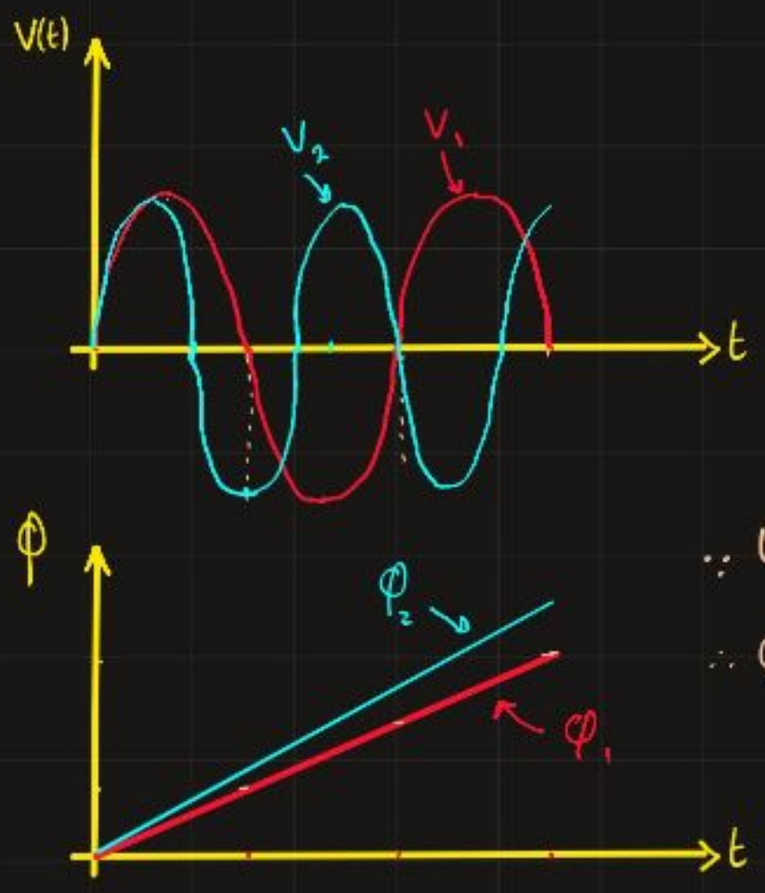
✱ What is Phase?

$\rightarrow \varphi = \int \omega \, dt$ $\rightsquigarrow \omega = \frac{\partial \varphi}{\partial t} = \frac{2\pi}{T}$



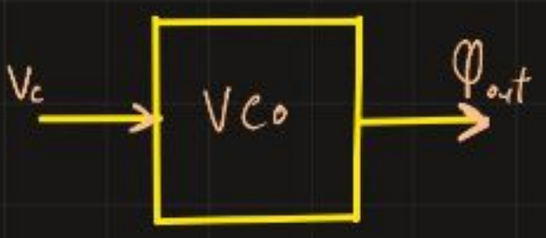
→ every Period T the phase accumilate 2π



$\because \omega_2 > \omega_1$

$\therefore \varphi_2 = \frac{\partial \omega_2}{\partial t} > \varphi_1 = \frac{\partial \omega_1}{\partial t}$

✱ Voltage controled oscillator (VCO) :



→ VCO efficiently Provides oscillating waveform with Variable Frequency controled by V_c.

→ $\omega_{out} = \omega_0 + K_{VCO} \cdot V_c$ ①

. where ω_0 is free running frequency "constant"

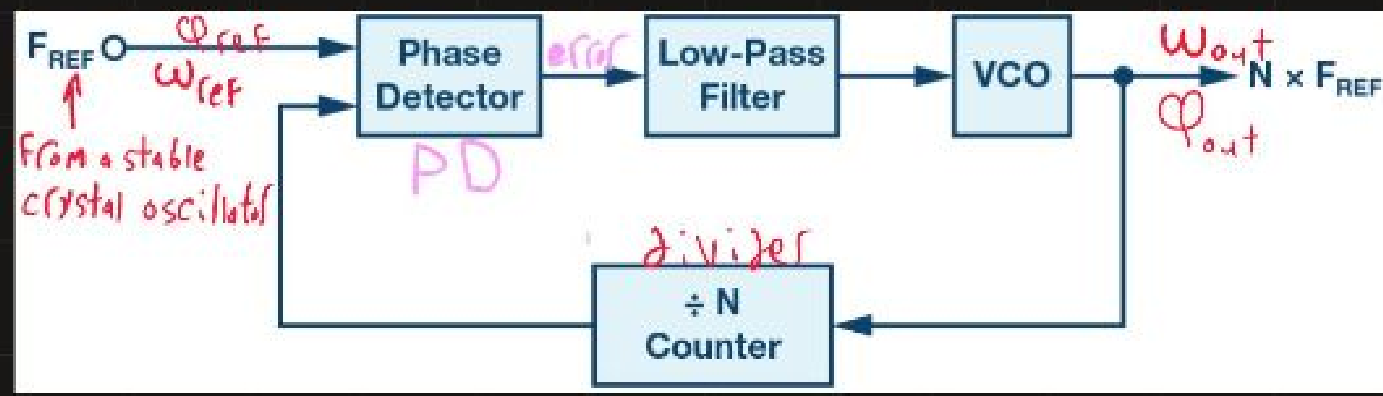
. K_{VCO} : gain of VCO [rad/sec.V]

→ equation ① assumes that the Frequency ω_{out} changes Linearly with the controled Voltage V_c which isn't always true especialy For high frequencies.

→ VCO have a certion range of controled Voltages and frequencies [$V_1 \rightarrow V_2$, $\omega_1 \rightarrow \omega_2$] "bounds"

* Phase locked loop (PLL):

- PD: find difference "Compair" Phases of two signals
- Reference: a very stable oscillator who has accurate ω_{ref}
- LPF: remove noise, can be as simple as RC LPF
- Divider: divides output frequency ω_o by N if we want to change ω_o insted of paying anew crystal, can be set to one $N=1$ if no modification needed.



→ $\varphi_{ref} - \varphi_{out} = \varphi_{error}$ ← target φ_{error} ↓↓ , note φ_{error} needs to be constant.

$\therefore \frac{\partial \varphi_{ref}}{\partial t} - \frac{\partial \varphi_{out}}{\partial t} = \frac{\partial \varphi_{error}}{\partial t}$

$\therefore \omega_{ref} = \omega_{out}$ ← only if $\frac{\partial \varphi_{error}}{\partial t} = 0$

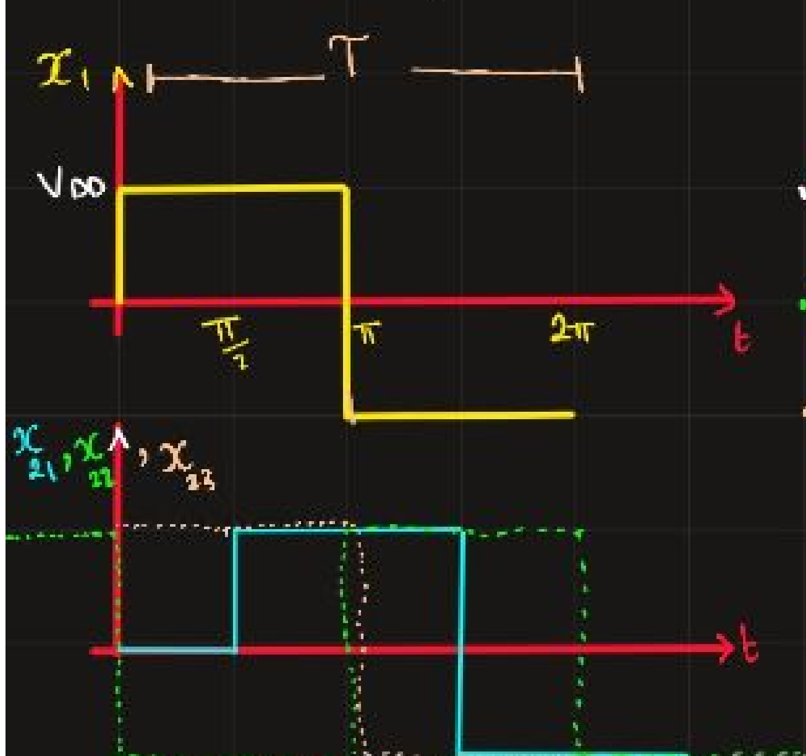
→ So if the phase error φ_{error} is constant then the PLL will make $\omega_{out} = \omega_{ref}$

→ if the ω_{ref} is stable .... then why not use it in the first place?

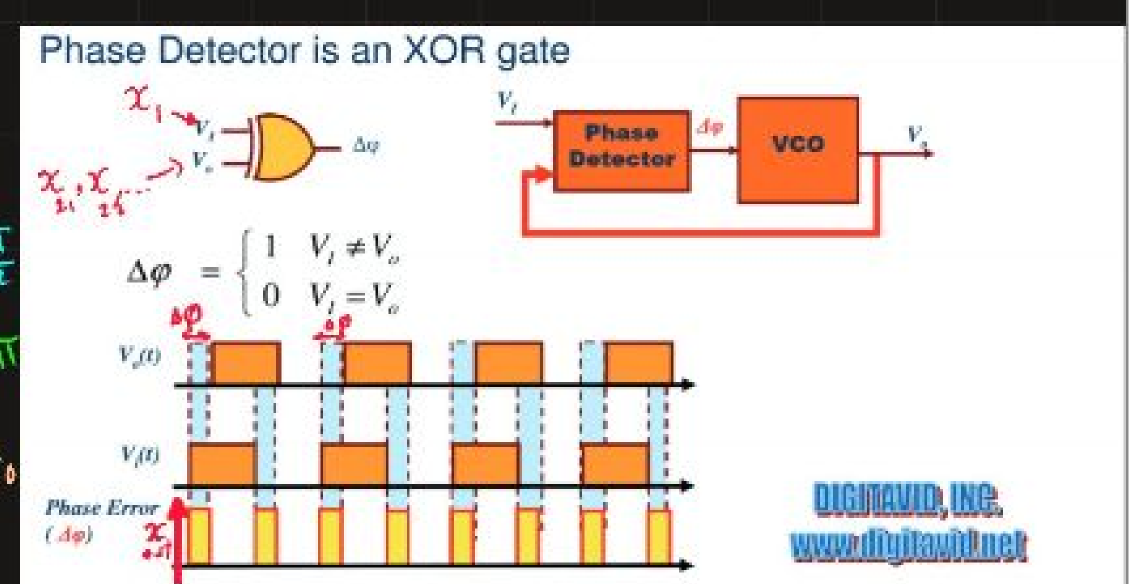
↳ the crystal has one pre-defined freq. we can't change it directly, but using the PLL with the divider we can get any ratio of ω_{ref} by controlling N. $\omega_{out} = N \cdot \omega_{ref}$

→ The PLL can be implemented by XOR gate:

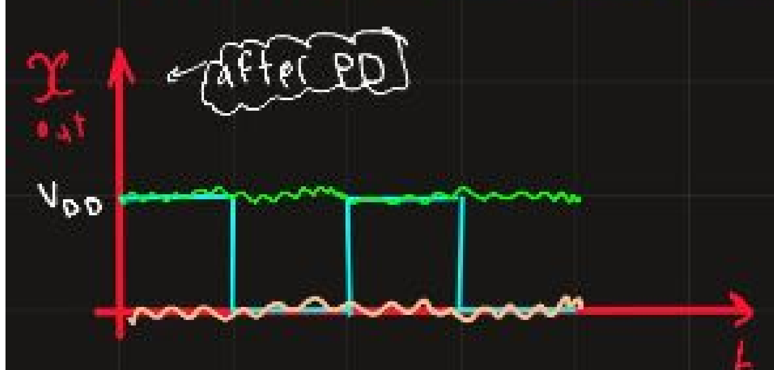
- as $\Delta\varphi$ ↑↑ , the duty cycle of x_{out} ↑↑



- x_{21} is phase shifted from x_1 by $\frac{\pi}{2}$ ⇝ $\therefore \Delta\varphi = \frac{\pi}{2}$
- x_{22} ← Flipped .... π .... π
- x_{23} .... 2π or zero .... zero

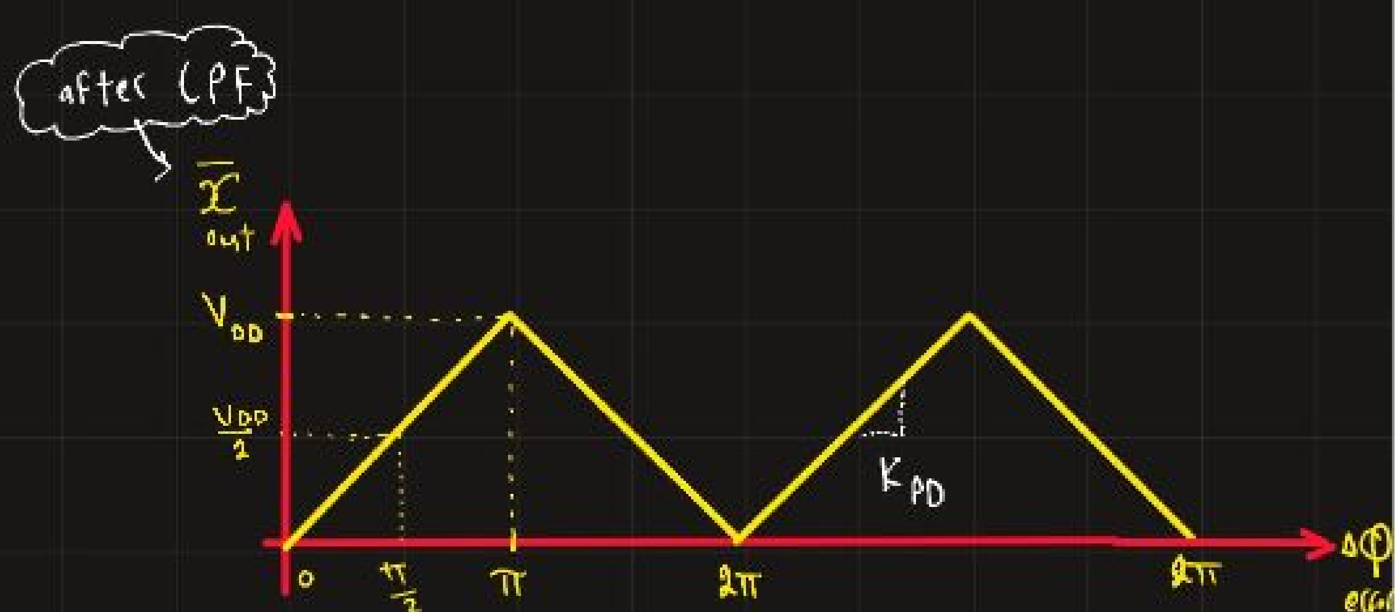


$\Delta\varphi = \begin{cases} 1 & V_i \neq V_o \\ 0 & V_i = V_o \end{cases}$



- $\bar{x}_{21} = \frac{1}{2} V_{DD}$
- $\bar{x}_{22} = V_{DD}$
- $\bar{x}_{23} = 0$

} ∴ ⇝



∴ the output of PD + LPF is linear with the $\Delta\varphi_{error}$ ⇝ ∴ PD+LPF can be modeled using a linear amplifier with gain K_{PD} ⇝ 

⇝ ∴ $V_c = K_{PD} \cdot \Delta\varphi_{error}$

⇝ PD works with only digital signals, if sin or cos convert them to square first.

• we can drive an expression for the $\Delta\varphi_{error}$ with K_{PD} & K_{vco} to help us in the design: at steady state

∴ $V_c = K_{PD} \cdot \varphi_e$ → (1)

∴ $\omega_{out} = \omega_o + K_{vco} \cdot V_c$ → (2)

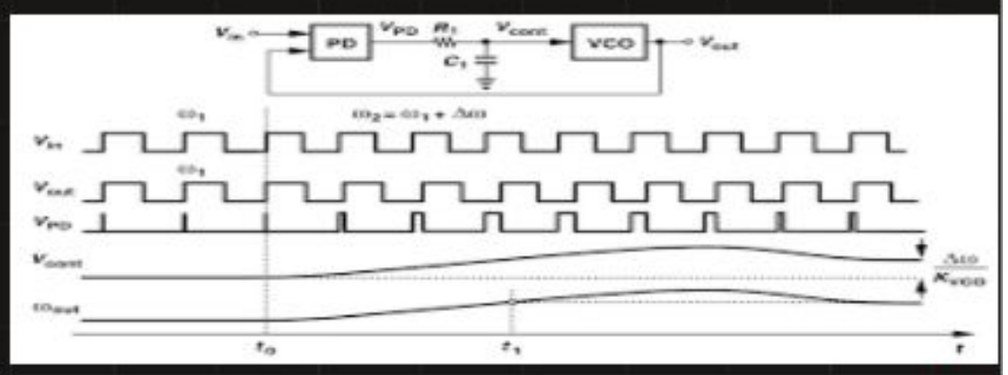
→ ∴ $\omega_{out} = \omega_o + K_{vco}[K_{PD}\varphi_e]$

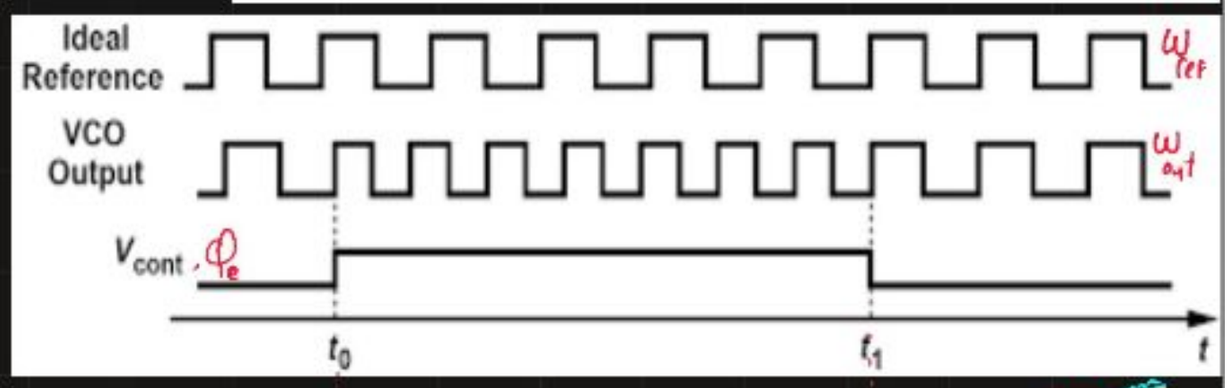
∴ $\varphi_e = \dfrac{\omega_{out} - \omega_o}{K_{PD}\ K_{vco}}$ (3) #

∴ to get low φ_e ⇝ K_{PD}↑↑ and K_{vco} ↑↑

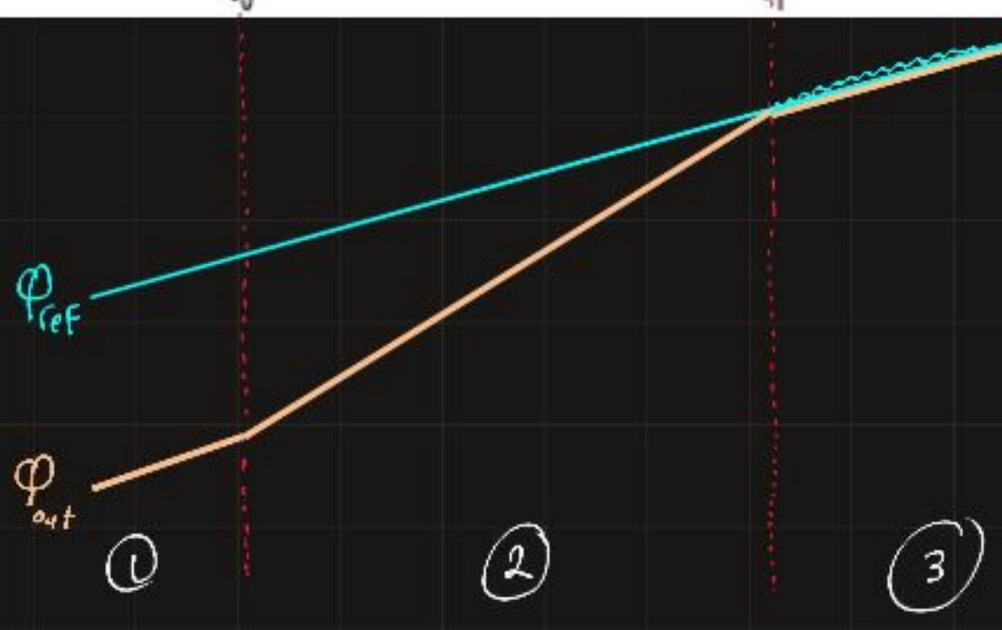
• example:

→ at region ① $\omega_{ref} = \omega_{out}$ but there is a phase difference φ_e so at to φ_e↑↑ ⇝ it acts as a signal to the VCO to increas ω_{out} remember $V_c = K_{PD} \cdot \varphi_e$ ⇝ φ_e↑↑ V_c↑↑ ω_{out} ↑↑





→ at region ② we can see that the slope of φ_{out} is increasing this is because ω_{out} is increasing, and it will continue to change untill the φ_e becomes zero or a designed value of eq(2).



→ at region ③ $\varphi_e = 0$ or a designed value, and as a result the ω_{out} is now back to the initial value.

Notes: • at region ① at the begind even though $\omega_{out} = \omega_{ref}$ but the device went through region ② & ③ this is because the PPL senses the phase error only and at region ① $\varphi_e \neq 0$.

• time PLL takes to achive steady state is called "setting time" and here = $t_1 - t_0$.

- to make the LPF eject more noise we need to decrease it's bandwidth "$BW = f_c = \frac{1}{2\pi RC}$"
  So increase $RC\uparrow$, but as a result $\tau = RC \uparrow\uparrow$ which results to slow setting time "tradeoff"
- if noise ocures and the gain of VCO is high $K_{VCO}\uparrow\uparrow$ to get f_{eb}, it will be senstive to small variations of noise ⇝ then there'll be unstability. "tradeoff"