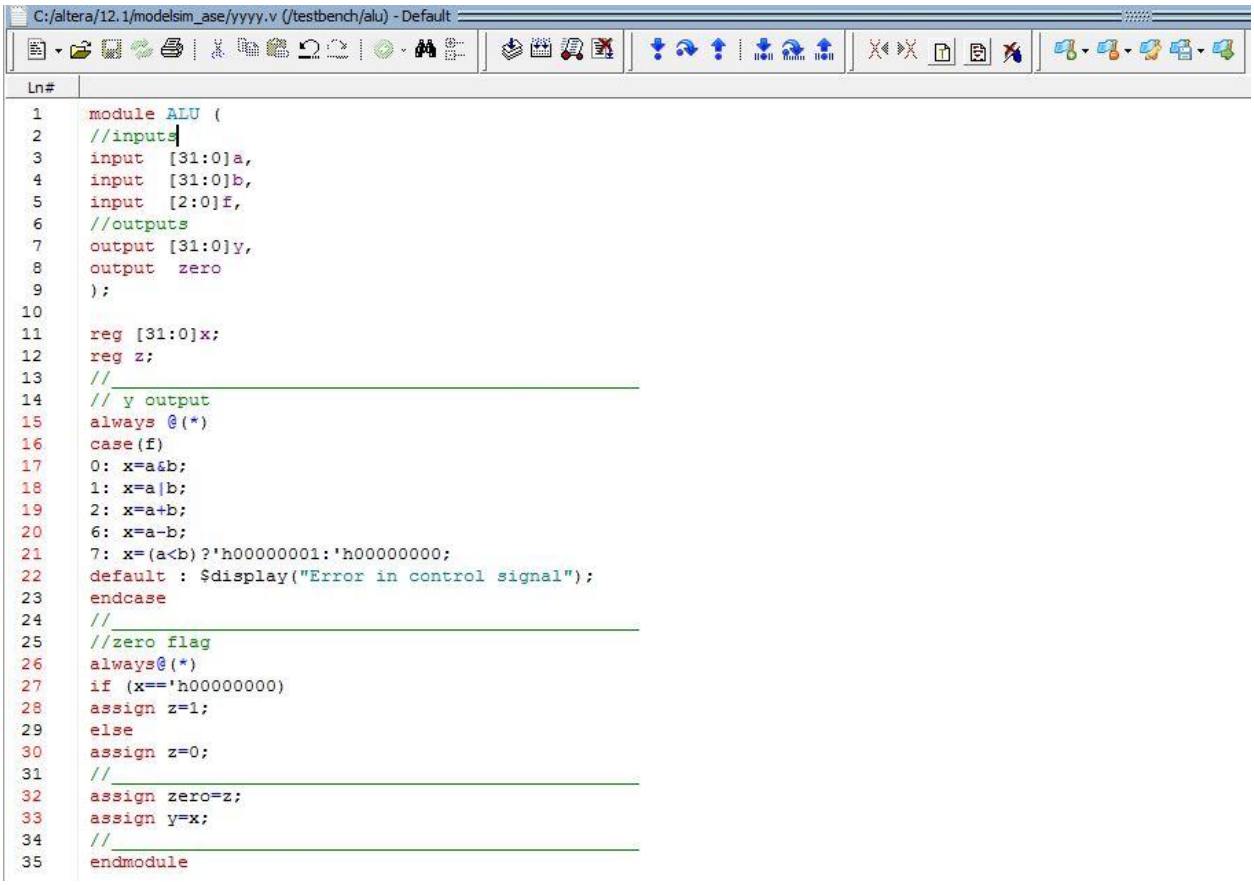
Name : **Eslam omar mohamed mohamed**

No: **51**

Lab 1

ALU 32 bit

ALU Code:



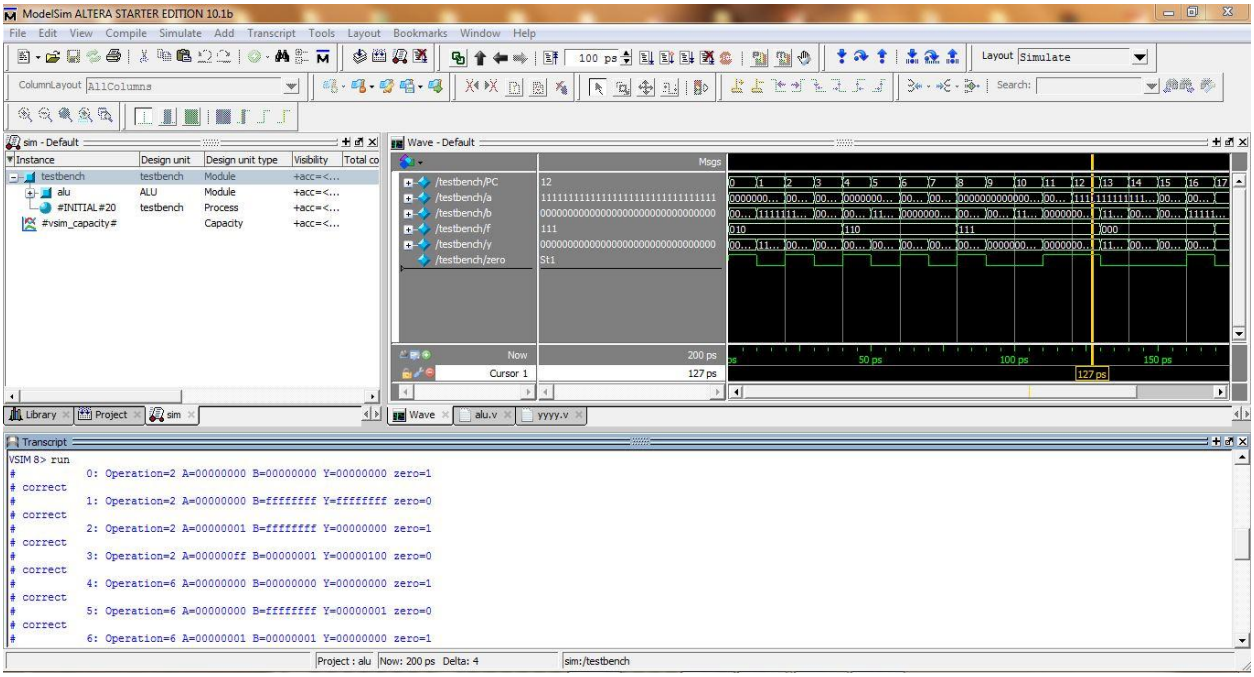

```
1   module ALU (
2   //inputs
3   input  [31:0]a,
4   input  [31:0]b,
5   input  [2:0]f,
6   //outputs
7   output [31:0]y,
8   output  zero
9   );
10
11  reg [31:0]x;
12  reg z;
13  //_____________________________________________
14  // y output
15  always @(*)
16  case(f)
17  0: x=a&b;
18  1: x=a|b;
19  2: x=a+b;
20  6: x=a-b;
21  7: x=(a<b)?'h00000001:'h00000000;
22  default : $display("Error in control signal");
23  endcase
24  //_____________________________________________
25  //zero flag
26  always@(*)
27  if (x=='h00000000)
28  assign z=1;
29  else
30  assign z=0;
31  //_____________________________________________
32  assign zero=z;
33  assign y=x;
34  //_____________________________________________
35  endmodule
```

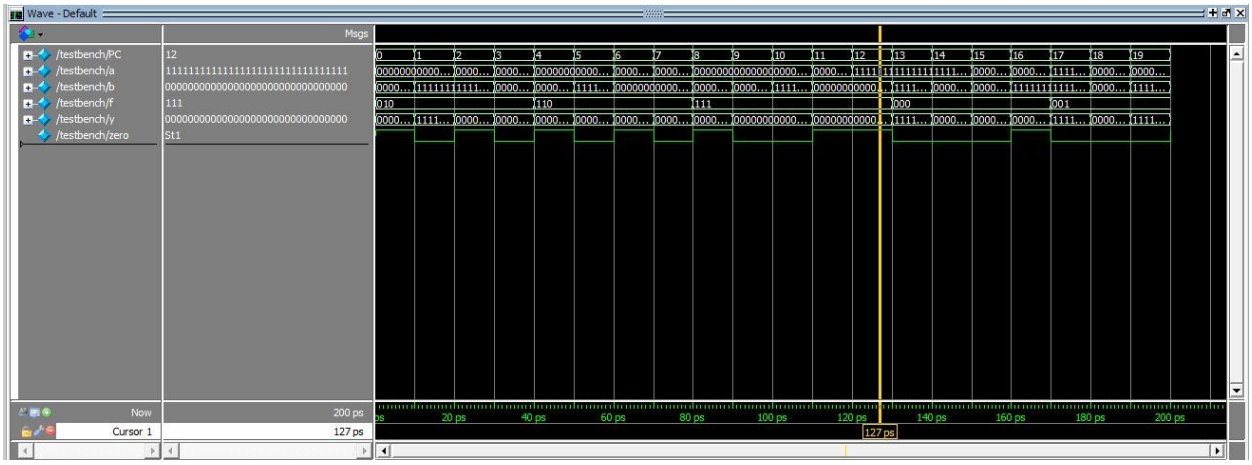
Test bench code:

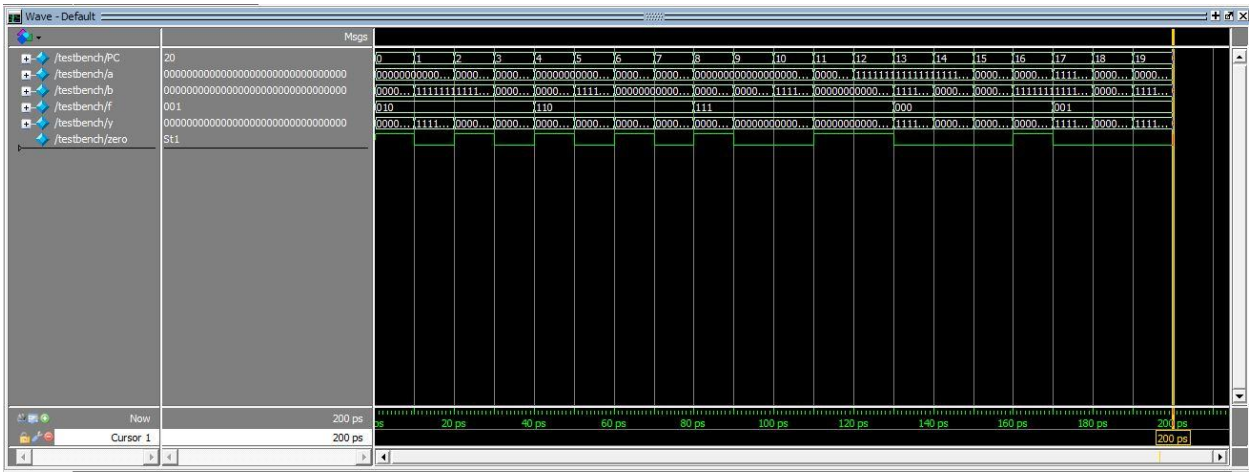
C:/altera/12.1/modelsim_ase/alu.v (/testbench) - Default

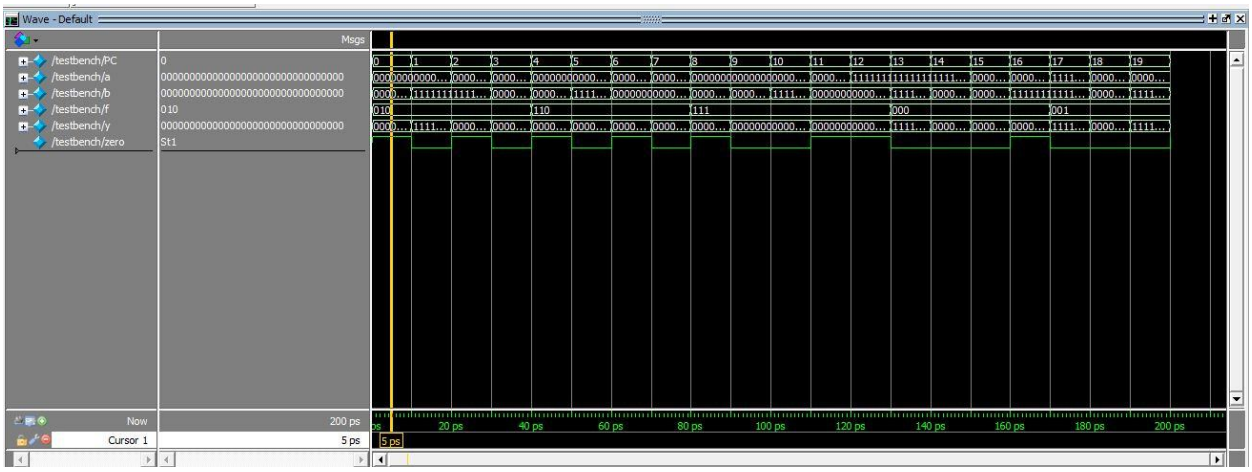
```
Ln#
 1  module testbench();
 2
 3  //memory file reg
 4  reg [103:0] Mem [0:20];
 5  integer PC;   //counter for memory swap
 6  //_____________________________________________
 7  //inputs
 8  reg  [31:0]a;
 9  reg  [31:0]b;
10  reg  [2:0]f;
11  //outputs
12  wire [31:0]y;
13  wire  zero;
14  //_____________________________________________
15  ALU alu (.a(a), .b(b), .f(f), .y(y), .zero(zero));
16  //_____________________________________________
17  initial $readmemh("data1.txt",Mem);
18
19  //_____________________________________________
20  initial begin
21
22  for (PC=0;PC<21;PC=PC+1)  begin
23  // Get inputs from memory
24          a=Mem[PC][99:68];    //A
25          b=Mem[PC][67:36];    //B
26          f=Mem[PC][102:100];  //control signal
27  //print the test case vector
28
29  $display("%d: Operation=%h A=%h B=%h Y=%h zero=%h",PC,Mem[PC][102:100],Mem[PC][99:68],Mem[PC][67:36],Mem[PC][35:4],Mem[PC][0:0]);
30
31  // check the correct input
32  #10;
33        if((y==Mem[PC][35:4])&(zero==Mem[PC][0:0]))
34        $display("correct");
35        else
36        $display("wrong");
37        end
38
39  end
40  //_____________________________________________
41  endmodule
42
```

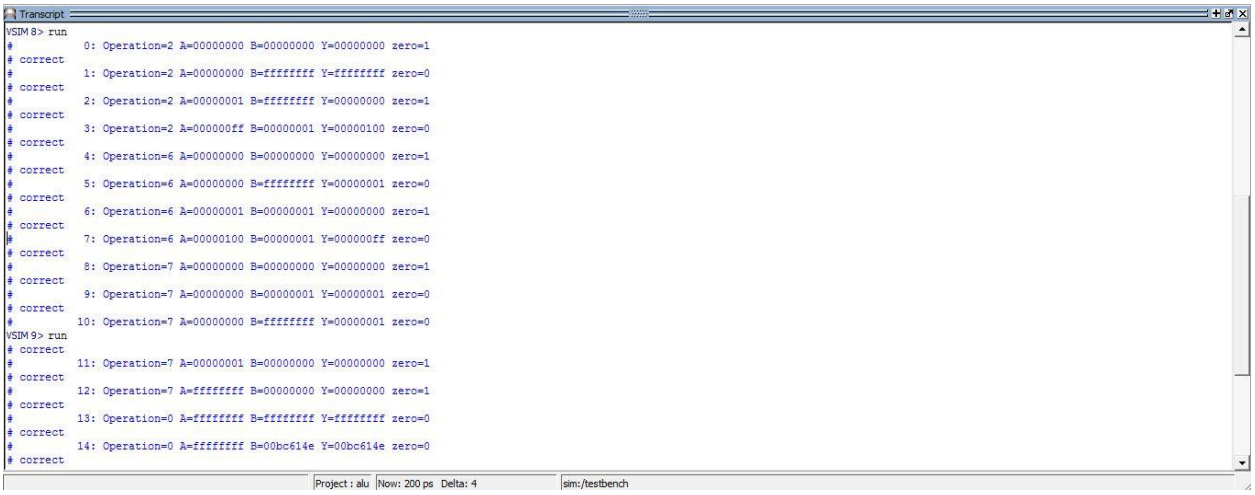
Test wave:

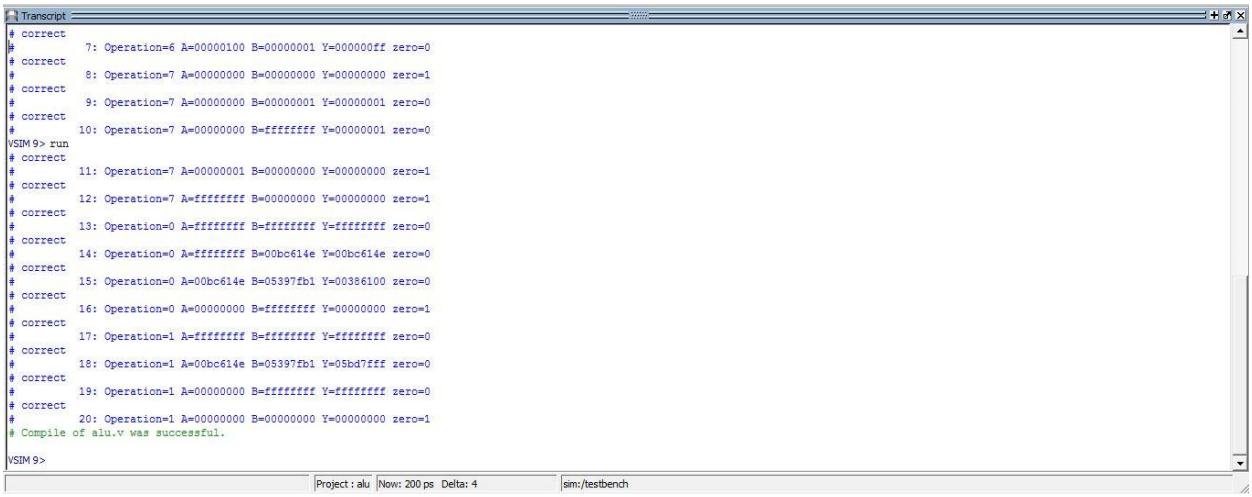

ModelSim ALTERA STARTER EDITION 10.1b
sim - Default
Wave - Default
Transcript
VSIM 8> run
0: Operation=2 A=00000000 B=00000000 Y=00000000 zero=1
correct
1: Operation=2 A=00000000 B=ffffffff Y=ffffffff zero=0
correct
2: Operation=2 A=00000001 B=ffffffff Y=00000000 zero=1
correct
3: Operation=2 A=000000ff B=00000001 Y=00000100 zero=0
correct
4: Operation=6 A=00000000 B=00000000 Y=00000000 zero=1
correct
5: Operation=6 A=00000000 B=ffffffff Y=00000001 zero=0
correct
6: Operation=6 A=00000001 B=00000001 Y=00000000 zero=1


Wave - Default
/testbench/PC
/testbench/a
/testbench/b
/testbench/f
/testbench/y
/testbench/zero
Now
Cursor 1


Wave - Default
Msgs
/testbench/PC
/testbench/a
/testbench/b
/testbench/f
/testbench/y
/testbench/zero
Now
Cursor 1


Wave - Default
Msgs
/testbench/PC
/testbench/a
/testbench/b
/testbench/f
/testbench/y
/testbench/zero
Now
Cursor 1


Transcript
VSIM 8> run
0: Operation=2 A=00000000 B=00000000 Y=00000000 zero=1
correct
1: Operation=2 A=00000000 B=ffffffff Y=ffffffff zero=0
correct
2: Operation=2 A=00000001 B=ffffffff Y=00000000 zero=1
correct
3: Operation=2 A=000000ff B=00000001 Y=00000100 zero=0
correct
4: Operation=6 A=00000000 B=00000000 Y=00000000 zero=1
correct
5: Operation=6 A=00000000 B=ffffffff Y=00000001 zero=0
correct
6: Operation=6 A=00000001 B=00000001 Y=00000000 zero=1
correct
7: Operation=6 A=00000100 B=00000001 Y=000000ff zero=0
correct
8: Operation=7 A=00000000 B=00000000 Y=00000000 zero=1
correct
9: Operation=7 A=00000000 B=00000001 Y=00000001 zero=0
correct
10: Operation=7 A=00000000 B=ffffffff Y=00000001 zero=0
VSIM 9> run
correct
11: Operation=7 A=00000001 B=00000000 Y=00000000 zero=1
correct
12: Operation=7 A=ffffffff B=00000000 Y=00000000 zero=1
correct
13: Operation=0 A=ffffffff B=ffffffff Y=ffffffff zero=0
correct
14: Operation=0 A=ffffffff B=00bc614e Y=00bc614e zero=0
correct
Project : alu
Now: 200 ps Delta: 4
sim:/testbench


Transcript
correct
7: Operation=6 A=00000100 B=00000001 Y=000000ff zero=0
correct
8: Operation=7 A=00000000 B=00000000 Y=00000000 zero=1
correct
9: Operation=7 A=00000000 B=00000001 Y=00000001 zero=0
correct
10: Operation=7 A=00000000 B=ffffffff Y=00000001 zero=0
VSIM 9> run
correct
11: Operation=7 A=00000001 B=00000000 Y=00000000 zero=1
correct
12: Operation=7 A=ffffffff B=00000000 Y=00000000 zero=1
correct
13: Operation=0 A=ffffffff B=ffffffff Y=ffffffff zero=0
correct
14: Operation=0 A=ffffffff B=00bc614e Y=00bc614e zero=0
correct
15: Operation=0 A=00bc614e B=05397fb1 Y=00386100 zero=0
correct
16: Operation=0 A=00000000 B=ffffffff Y=00000000 zero=1
correct
17: Operation=1 A=ffffffff B=ffffffff Y=ffffffff zero=0
correct
18: Operation=1 A=00bc614e B=05397fb1 Y=05bd7fff zero=0
correct
19: Operation=1 A=00000000 B=ffffffff Y=ffffffff zero=0
correct
20: Operation=1 A=00000000 B=00000000 Y=00000000 zero=1
Compile of alu.v was successful.
VSIM 9>
Project : alu
Now: 200 ps Delta: 4
sim:/testbench