Vsevolod Vinogradov
Preferred role: Machine Learning Engineer

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Education: M.Sc. in Communications Engineering (2012)
Citizenship: Russia
Residence: Copenhagen, DK, ready to relocate
Linked IN Blog

Background

I have 11 years of experience in computer hardware engineering. The key focus were DSP algorithms implementation win an FPGA and ASIC chips.

DSP (Digital Signal Processing) is a wide area that uses techniques from the applied math, analyses, statistics and statistical learning to proceed signals, like radio, voice, images, in a digital form. DSP gives theoretical and practical recipes to develop digital circuits for signal processing. ASIC is small pieces of silicon with integrated circuits of digital logic, that we often refer as microchip. Your dishwasher controller, GPU and CPU are ASICs. **ASIC** manufacturing process requires millions of $ of investment, so there's an option to assemble custom digital circuit from predefined building blocks "in-filed". **FPGA** (Filed Programmable Gate Array) is kind of a LEGO blocks set, from which an engineer may assemble digital circuits "in the field" by reconfiguring the firmware of the FPGA chip. FPGA and ASIC are consist of IP(Intellectual Property) Cores, sort of the functional block.

I switched to a Software Engineering Role to expand my area of the expertise and more widely utilize my theoretical skills

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Skill Set

Machine Learning

- Strong theoretical background in linear algebra, statistics and numerical methods
- Matlab, SciPy, RandomForest, XGBoost
- Deep Learning with TensorFlow, Keras
- Extensive data exploration and visualization skills

Software Engineering:

- Modern C++14/17/20 with for Linux and Windows
- DevOps: CI/CD, TDD, Jenkins, Gitlab, Doctest, GoogleTest, Bash, CMake

Computer Hardware

- Deep understanding of CPU and GPU architectures, DRAM/SRAM memory controllers, PCIe and network interfaces

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Work Experience

Alipes A/S Denmark

Quant Developer, *Aug.2020 - till now*

- Accelerate decision trees and DNN models on the FPGAs for financial applications .
- **Throughput accelerations Vitis Flow, Xilinx software oriented OpenCL-like system for Alveo cards series. For quantized model achieved ~30% performance in prediction/sec against GPU**
- Low latency application - full stack system design - HLS kernel development, low latency PCIe drivers and IP Core, project design in Vivado, Windows/Ubuntu cross-platform library, integration with existing computational framework. Reduced prediction latency on a 50% in comparison with GPU CUDA implementation

Widex A/S, Denmark

IC Specialist, Digital Design *Jan. 2019 — Aug.2020*

- Design and implementation of ultra-low-power DSP blocks for next-generation hearing aids for ASIC

with a strong focus on space and power usage optimization. Maintain and documentation of the existing legacy IP cores. Functional, integrations and code coverage testing

- I helped our team with the transition from SVN to Git and from hardware design language VHDL to System Verilog. Prepared training materials and held more than 10 workshops in a small groups for cross-border teams in Germany and Denmark.
- Working under FDA and EMEA regulation regarding the safety and reliability requirements for medical devices.

Cobham Satcom (ex. Thrane&Thrane), Denmark

FPGA Development Engineer in Aviator S-team *March 2018 — December 2018*

- Design, support and maintain IP Cores for Zynq SoC in Aviator S Smart Aircraft project
- Safety and security requirements writing and implementing, design test cases and specification for commercial airlines' avionics certification

Huawei Technologies, Russian Research Center, Moscow

Algorithm researcher in Nonlinear IRF sector *September 2015 —January 2018*

Key projects:

- Develop in Matlab and implement in the FPGA complex-arithmetic multilayer non-linear adaptive filtering system (DPD) for radio frequency applications in 4G+ base stations
- 4x4 MIMO Platform. Developed embedded platform software and Matlab API for communication over 1G Ethernet

Awards: Outstanding Contractor award 2016 of Russian R&D Center Member of Outstanding Team Award 2017

Digital Solutions, SPE, LLC Moscow

FPGA designer *September 2012 — September 2015*

Full-stack electronic design from small IP cores to device production.
Key Projects:

- Member of FPGA team on the Deep packet inspection (DPI) project
- Develop Error Correction Code for System-on-Chip ASIC

Research Institute of Precision Instruments, Moscow

FPGA designer *February 2010 — September 2012*

- Research satellite radio channel and develop error correction codes for space applications
- Develop FPGA based satellite hardware

Awards: Concatenation codes research project took the prize “Youth and future of aviation and space exploration 2012” of Russian Aerospace Agency [ru link]

Education

- M.Sc. in Communications Engineering. National Research University "MAI"(Aviation Institute) 2006-2012, 5.5 years
- Advanced specialization, 2 years, Information technology in electronic design - DSP, ARM, PCB design, FPGA, microcontrollers, amplifiers. Certificated, with honors
- Specialization “Advanced Machine Learning”[link] by NRE Higher School of Economics, 2020
    - Introduction to Machine learning 100%
    - Introduction to deep learning. 98.2% With Honor
    - Bayesian Methods for Machine Learning With Honor
    - Practical Reinforcement Learning, With Honors
    - Addressing Large Hadron Collider Challenges by Machine Learning
    - How to Win a Data Science Competition
    - Natural Language Processing
    - Deep Learning in Computer vision
- Online Courses:
    - EDX :Circuits & Electronics: MITx 6.002x MITx, 2012
    - Coursera: IBM: Databases and SQL for Data Science, 2020
    - Udemy Advanced C++Programming 2020