STM32F100x4, STM32F100x6, STM32F100x8, STM32F100xB errata sheet

STM32F100xx low and medium-density value line device limitations

Silicon identification

This errata sheet applies to the revision Z of the STMicroelectronics low and medium-density STM32F100xB value line products.
This family features an ARM™ 32-bit Cortex®-M3 core, for which an errata notice is also available (see *Section 1* for details).

Table 2 shows the full list of the value line part numbers concerned by these limitations.

The products are identifiable as shown in *Table 1*:

● by the Revision code marked below the sales type on the device package
● by the last three digits of the internal sales type printed on the box label

Table 1.   Device identification[1]

Sales type	Revision code[2] marked on device
STM32F100xxx[3]	"Z"

1. The REV_ID bits in the DBGMCU_IDCODE register show the revision code of the device (see the STM32F100xx reference manual for details on how to find the revision code).

2. Refer to *Appendix A: Revision code on device marking* for details on how to identify the Revision code on the different packages.

3. This document only applies to devices that have internal code B in their sales type.

Table 2.   Device summary

Reference	Part number
STM32F100x4	STM32F100C4, STM32F100R4
STM32F100x6	STM32F100C6, STM32F100R6
STM32F100x8	STM32F100C8, STM32F100R8, STM32F100V8
STM32F100xB	STM32F100CB, STM32F100RB, STM32F100VB

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1   ARM™ 32-bit Cortex®-M3 limitations

An errata notice of the STM32F100xx core is available from the following web address: *http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.eat0420a/.*
The direct link to the errata notice pdf is:
http://infocenter.arm.com/help/topic/com.arm.doc.eat0420a/Cortex-M3-Errata-r1p1-v0.2.pdf.
All the described limitations are minor and related to the revision r1p1-01rel0 of the Cortex-M3 core. *Table 3* summarizes these limitations and their implications on the behavior of medium-density STM32F100xx devices.

Table 3.   Cortex-M3 core limitations and impact on microcontroller behavior

ARM ID	ARM category	ARM summary of errata	Impact on medium-density STM32F100xx devices
602117	Cat 2	LDRD with base in list may result in incorrect base register when interrupted or faulted	Minor
563915	Cat 2	Event register is not set by interrupts and debug	Minor
531064	impl	SWJ-DP missing POR reset sync	No
511864	Cat 3	Cortex-M3 may fetch instructions using incorrect privilege on return from an exception	No
532314	Cat 3	DWT CPI counter increments during sleep	No
538714	Cat 3	Cortex-M3 TPIU clock domain crossing	No
548721	Cat 3	Internal write buffer could be active whilst asleep	No
463763	Cat 3	BKPT in debug monitor mode can cause DFSR mismatch	Minor
463764	Cat 3	Core may freeze for SLEEPONEXIT single instruction ISR	Minor
463769	Cat 3	Unaligned MPU fault during a write may cause the wrong data to be written to a successful first access	No

1.1   Cortex-M3 limitations description for STM32F100xx value line devices

Only the limitations described below have an impact, even though minor, on the implementation of STM32F100xx low and medium-density devices.

All the other limitations described in the ARM errata notice (and summarized in *Table 3* above) have no impact and are not related to the implementation of STM32F100xx low and medium-density devices (Cortex-M3 r1p1-01rel0).

1.1.1 Cortex-M3 LDRD with base in list may result in incorrect base register when interrupted or faulted

Description

The Cortex-M3 Core has a limitation when executing an LDRD instruction from the system-bus area, with the base register in a list of the form LDRD Ra, Rb, [Ra, #imm]. The execution may not complete after loading the first destination register due to an interrupt before the second loading completes or due to the second loading getting a bus fault.

Workarounds

1. This limitation does not impact the STM32F100xx code execution when executing from the embedded Flash memory, which is the standard use of the microcontroller.

2. Use the latest compiler releases. As of today, they no longer generate this particular sequence. Moreover, a scanning tool is provided to detect this sequence on previous releases (refer to your preferred compiler provider).

1.1.2 Cortex-M3 event register is not set by interrupts and debug

Description

When interrupts related to a WFE occur before the WFE is executed, the event register used for WFE wakeup events is not set and the event is missed. Therefore, when the WFE is executed, the core does not wake up from WFE if no other event or interrupt occur.

Workaround

Use STM32F100xx external events instead of interrupts to wake up the core from WFE by configuring an external or internal EXTI line in event mode.

1.1.3 Cortex-M3 BKPT in debug monitor mode can cause DFSR mismatch

Description

A BKPT may be executed in debug monitor mode. This causes the debug monitor handler to be run. However, the bit 1 in the Debug fault status register (DFSR) at address 0xE000ED30 is not set to indicate that it was originated by a BKPT instruction. This only occurs if an interrupt other than the debug monitor is already being processed just before the BKPT is executed.

Workaround

If the DFSR register does not have any bit set when the debug monitor is entered, this means that we must be in this "corner case" and so, that a BKPT instruction was executed in debug monitor mode.

1.1.4 Cortex-M3 may freeze for SLEEPONEXIT single instruction ISR

Description

If the Cortex-M3 SLEEPONEXIT functionality is used and the concerned interrupt service routine (ISR) contains only a single instruction, the core becomes frozen. This freezing may occur if only one interrupt is active and it is preempted by an interrupt whose handler only contains a single instruction.
However, any new interrupt that causes a preemption would cause the core to become unfrozen and behave correctly again.

Workaround

This scenario does not happen in real application systems since all enabled ISRs should at least contain one instruction. Therefore, if an empty ISR is used, then insert an NOP or any other instruction before the exit instruction (BX or BLX).

2 STM32F100xx silicon limitations

Table 4 gives quick references to all documented limitations.

Table 4.   Summary of silicon limitations

Links to silicon limitations	
Section 2.1: Voltage glitch on ADC input 0	
Section 2.2: Debugging Stop mode and system tick timer	
Section 2.3: Debugging Stop mode with WFE entry	
Section 2.4: Unique ID unavailability on devices with date code earlier than 045	
Section 2.5: Alternate function	*Section 2.5.1: SPI1 in slave mode and USART2 in synchronous mode*
	Section 2.5.2: SPI1 in master mode and USART2 in synchronous mode
	Section 2.5.3: SPI2 in slave mode and USART3 in synchronous mode
	Section 2.5.4: SPI2 in master mode and USART3 in synchronous mode
	Section 2.5.5: I2C2 with SPI2 and USART3
	Section 2.5.6: I2C1 with SPI1 remapped and used in master mode
	Section 2.5.7: I2C1 and TIM3_CH2 remapped
	Section 2.5.8: USARTx_TX pin usage limitation
Section 2.6: Boundary scan TAP: wrong pattern sent out after the "capture IR" state	
Section 2.7: Flash memory BSY bit delay versus STRT bit setting	
Section 2.8: I2C peripheral	*Section 2.8.1: Some software events must be managed before the current byte is being transferred*
	Section 2.8.2: SMBus standard not fully supported
	Section 2.8.3: Wrong behavior of I2C peripheral in master mode after a misplaced Stop
	Section 2.8.4: Mismatch on the "Setup time for a repeated Start condition" timing parameter
	Section 2.8.5: Data valid time (tVD;DAT) violated without the OVR flag being set
	Section 2.8.6: Wrong data read into data register
Section 2.9: USART peripheral	*Section 2.9.1: Idle frame is not detected if receiver clock speed is deviated*
	Section 2.9.2: In full duplex mode, the Parity Error (PE) flag can be cleared by writing the data register
	Section 2.9.3: Parity Error (PE) flag is not set when receiving in Mute mode using address mark detection
	Section 2.9.4: Break frame is transmitted regardless of nCTS input line status
	Section 2.9.5: nRTS signal abnormally driven low after a protocol violation

Table 4. **Summary of silicon limitations (continued)**

Links to silicon limitations	
Section 2.10: Timers	*Section 2.10.1: Missing capture flag*
	Section 2.10.2: Overcapture detected too early
	Section 2.10.3: General-purpose timer: regulation for 100% PWM
Section 2.11: LSI clock stabilization time	

2.1 Voltage glitch on ADC input 0

Description

A low-amplitude voltage glitch may be generated (on ADC input 0) on the PA0 pin, when the ADC is converting with injection trigger. It is generated by internal coupling and synchronized to the beginning and the end of the injection sequence, whatever the channel(s) to be converted.

The glitch amplitude is less than 150 mV with a typical duration of 10 ns (measured with the I/O configured as high-impedance input and left unconnected). If PA0 is used as a digital output, this has no influence on the signal. If PA0 is used has a digital input, it will not be detected as a spurious transition, providing that PA0 is driven with an impedance lower than 5 kΩ. This glitch does not have any influence on the remaining port A pin or on the ADC conversion injection results, in single ADC configuration.

When using the ADC in dual mode with injection trigger, and in order to avoid any side effect, it is advised to distribute the analog channels so that Channel 0 is configured as an injected channel.

Workaround

None.

2.2 Debugging Stop mode and system tick timer

Description

If the system tick timer interrupt is enabled during the Stop mode debug (DBG_STOP bit set in the DBGMCU_CR register), it will wakeup the system from Stop mode.

Workaround

To debug the Stop mode, disable the system tick timer interrupt.

2.3 Debugging Stop mode with WFE entry

Description

When the Stop debug mode is enabled (DBG_STOP bit set in the DBGMCU_CR register) this allows software debugging during Stop mode.

However, if the application software uses the WFE instruction to enter Stop mode, after wakeup some instructions could be missed if the WFE is followed by sequential instructions. This affects only Stop debug mode with WFE entry.

Workaround

To debug Stop mode with WFE entry, the WFE instruction must be inside a dedicated function with 1 instruction (NOP) between the execution of the WFE and the Bx LR.

Example: __asm void _WFE(void) {

WFE

NOP

BX lr }

2.4 Unique ID unavailability on devices with date code earlier than 045

Description

The unique ID information is not available on STM32F100xx devices with a date code earlier than 045. Reading the unique ID information from the part returns the vaue 0xFF.
Refer to Appendix A: Revision and date codes on device marking for the location of the date code device marking.

Workaround

None.

2.5 Alternate function

In some specific cases, some potential weakness may exist between alternate functions mapped onto the same pin.

2.5.1 SPI1 in slave mode and USART2 in synchronous mode

Conditions

●   SPI1 and USART2 are clocked
●   I/O port pin PA4 is configured as an alternate function output.

Description

USART2 cannot be used in synchronous mode (USART2_CK signal), if SPI1 is used in slave mode.

Workaround

None.

2.5.2 SPI1 in master mode and USART2 in synchronous mode

Conditions

- SPI1 and USART2 are clocked
- I/O port pin PA4 is configured as an alternate function output.

Description

USART2 cannot be used in synchronous mode (USART2_CK signal) if SPI1 is used in master mode and SP1_NSS is configured in software mode. In this case USART2_CK is not output on the pin.

Workaround

In order to output USART2_CK, the SSOE bit in the SPI1_CR2 register must be set to configure the pin in output mode.

2.5.3 SPI2 in slave mode and USART3 in synchronous mode

Conditions

- SPI2 and USART3 are clocked
- I/O port pin PB12 is configured as an alternate function output.

Description

USART3 cannot be used in synchronous mode (USART3_CK signal) if SPI2 is used in slave mode.

Workaround

None.

2.5.4 SPI2 in master mode and USART3 in synchronous mode

Conditions

- SPI2 and USART3 are clocked
- I/O port pin PB12 is configured as an alternate function output.

Description

USART3 cannot be used in synchronous mode (USART3_CK signal) if SPI2 is used in master mode and SP2_NSS is configured in software mode. In this case USART3_CK is not output on the pin.

Workaround

In order to output USART3_CK, the SSOE bit in the SPI2_CR2 register must be set to configure the pin in output mode,

2.5.5 I2C2 with SPI2 and USART3

Conditions

● I2C2 and SPI2 are clocked together or I2C2 and USART3 are clocked together

● I/O port pin PB12 is configured as an alternate function output

Description

● Conflict between the I2C2_SMBA signal (even if this function is not used) and SPI2_NSS in output mode.

● Conflict between the I2C2_SMBA signal (even if this function is not used) and USART3_CK.

● In these cases the I/O port pin PB12 is set to 1 by default if the I/O alternate function output is selected and I2C2 is clocked.

Workaround

I2C2_SMBA can be used as an output if SPI2 is configured in master mode with NSS in software mode.
I2C2_SMBA can be used in input mode if SPI2 is configured in master or slave mode with NSS managed by software.
SPI2 cannot be used in any other configuration when I2C2 is being used.

USART3 must *not* be used in synchronous mode when I2C2 is being used.

2.5.6 I2C1 with SPI1 remapped and used in master mode

Conditions

● I2C1 and SPI1 are clocked.

● SPI1 is remapped.

● I/O port pin PB5 is configured as an alternate function output.

Description

Conflict between the SPI1_MOSI signal and the I2C1_SMBA signal (even if SMBA is not used).

Workaround

Do not use SPI1 remapped in master mode and I2C1 together.

When using SPI1 remapped, the I2C1 clock must be disabled.

2.5.7 I2C1 and TIM3_CH2 remapped

Conditions

● I2C1 and TIM3 are clocked.

● I/O port pin PB5 is configured as an alternate function output.

Description

Conflict between the TIM3_CH2 signal and the I2C1_SMBA signal, (even if SMBA is not used).

In these cases the I/O port pin PB5 is set to 1 by default if the I/O alternate function output is selected and I2C1 is clocked. TIM3_CH2 cannot be used in output mode.

Workaround

To avoid this conflict, TIM3_CH2 can only be used in input mode.

2.5.8 USARTx_TX pin usage limitation

In USART receive-mode-only communication (TE = 0 in the USARTx_CR1 register), even when the USARTx_TX pin is not being used, the corresponding I/O port pin cannot be used to output another alternate function (in this mode the USARTx_TX output is set to 1 and thus no other alternate function output can be used).

This limitation applies to all USARTx_TX pins that share another alternate function output.

Workaround

Do not use the corresponding I/O port of the USARTx_TX pin in alternate function output mode. Only the input mode can be used (TE bit in the USARTx_CR1 has to be cleared).

2.6 Boundary scan TAP: wrong pattern sent out after the "capture IR" state

Description

After the "capture IR" state of the boundary scan TAP, the two least significant bits in the instruction register should be loaded with "01" for them to be shifted out whenever a next instruction is shifted in.
However, the boundary scan TAP shifts out the latest value loaded into the instruction register, which could be "00", "01", "10" or "11".

Workaround

The data shifted out, after the capture IR state, in the boundary scan flow should therefore be ignored and the software should check not only the two least significant bits (XXX01) but all register bits (XXXXX).

2.7 Flash memory BSY bit delay versus STRT bit setting

Description

When the STRT bit in the Flash memory control register is set (to launch an erase operation), the BSY bit in the Flash memory status register goes high one cycle later.

Therefore, if the FLASH_SR register is read immediately after the FLASH_CR register is written (STRT bit set), the BSY bit is read as 0.

Workaround

Read the BSY bit at least one cycle after setting the STRT bit.

2.8 I²C peripheral

2.8.1 Some software events must be managed before the current byte is being transferred

Description

When the EV7, EV7_1, EV6_1, EV6_3, EV2, EV8, and EV3 events are not managed before the current byte is being transferred, problems may be encountered such as receiving an extra byte, reading the same data twice or missing data.

Workarounds

When it is not possible to manage the EV7, EV7_1, EV6_1, EV6_3, EV2, EV8, and EV3 events before the current byte transfer and before the acknowledge pulse when changing the ACK control bit, it is recommended to:

● **Workaround 1**

Use the I2C with DMA in general, except when the Master is receiving a single byte.

● **Workaround 2**

Use I2C interrupts and boost their priorities to the highest one in the application to make them uninterruptible

● **Workaround 3** (only for EV6_1 and EV6_3 events used in method 2)

EV6_1 event (used in master receiver 2 bytes):

Stretch SCL line between ADDR bit is cleared and ACK is cleared:

a) ADDR=1

b) Configure SCL I/O as GPIO open-drain output low

c) Clear ADDR by reading SR1 register followed by reading SR3

d) Program ACK=0

e) Configure SCL I/O as Alternate Function open drain

EV6_3 event (used in master receiver 1 byte):

Stretch SCL line between ADDR bit is cleared and STOP bit programming:

a) ADDR=1

b) Program ACK=0

c) Configure SCL I/O as GPIO open-drain output low

d) Clear ADDR by reading SR1 register followed by reading SR3

e) Program STOP=1

f) Configure SCL I/O as Alternate Function open drain

2.8.2 SMBus standard not fully supported

Description

The I^{2}C peripheral is not fully compliant with the SMBus v2.0 standard since It does not support the capability to NACK an invalid byte/command.

Workarounds

A higher-level mechanism should be used to verify that a write operation is being performed correctly at the target device, such as:

1. Using the SMBA pin if supported by the host
2. the alert response address (ARA) protocol
3. the Host notify protocol

2.8.3 Wrong behavior of I2C peripheral in master mode after a misplaced Stop

Description

If a misplaced Stop is generated on the bus, the peripheral cannot enter master mode properly:

● If a void message is received (START condition immediately followed by a STOP): the BERR (bus error) flag is not set, and the I2C peripheral is not able to send a start condition on the bus after the write to the START bit in the I2C_CR2 register.

● In the other cases of a misplaced STOP, the BERR flag is set. If the START bit is already set in I2C_CR2, the START condition is not correctly generated on the bus and can create bus errors.

Workaround

In the I²C standard, it is allowed to send a Stop only at the end of the full byte (8 bits + acknowledge), so this scenario is not allowed. Other derived protocols like CBUS allow it, but they are not supported by the I²C peripheral.

In case of a noisy environment in which unwanted bus errors can occur, it is recommended to implement a timeout to ensure that after the START control bit is set, the SB (start bit) flag is set. In case the timeout has elapsed, the peripheral must be reset by setting the SWRST bit in the I2C_CR2 control register. It should also be reset in the same way if a BERR is detected while the START bit is set in I2C_CR2.

2.8.4 Mismatch on the "Setup time for a repeated Start condition" timing parameter

Description

In case of a repeated Start, the "Setup time for a repeated Start condition" (named Tsu;sta in the I²C specification) can be slightly violated when the I²C operates in Master Standard mode at a frequency between 88 kHz and 100 kHz.

The issue can occur only in the following configuration:

● in Master mode

● in Standard mode at a frequency between 88 kHz and 100 kHz (no issue in Fast-mode)

● SCL rise time:

    – If the slave does not stretch the clock and the SCL rise time is more than 300 ns (if the SCL rise time is less than 300 ns the issue cannot occur)

    – If the slave stretches the clock

The setup time can be violated independently of the APB peripheral frequency.

Workaround

Reduce the frequency down to 88 kHz or use the I²C Fast-mode if supported by the slave.

2.8.5 Data valid time ($t_{VD;DAT}$) violated without the OVR flag being set

Description

The data valid time (t_{VD};DAT, t_{VD};ACK) described by the I²C standard can be violated (as well as the maximum data hold time of the current data (t_{HD};DAT)) under the conditions described below. Moreover, if the data register is written too late and close to the SCL rising edge, an error can be generated on the bus (SDA toggles while SCL is high). These violations cannot be detected because the OVR flag is not set (no transmit buffer underrun is detected).

This issue can occur only under the following conditions:

● In Slave transmit mode

● With clock stretching disabled (NOSTRETCH=1)

● If the software is late in writing the DR data register, but not late enough to set the OVR flag (the data register is written before the SCL rising edge).

Workaround

If the master device allows it, use the clock stretching mechanism by programming the bit NOSTRETCH=0 in the I2C_CR1 register.

If the master device does not allow it, ensure that the software writes to the data register fast enough after TXE or ADDR events. For instance, use an interrupt on the TXE or ADDR flag and boost its priority to the higher level, or use DMA. Use this "NOSTRETCH" mode with a slow I2C bus speed.

Note: *The first data byte to transmit must be written in the data register after the ADDR flag is cleared, and before the next SCL rising edge, so that the time window for writing the first data byte in the data register is less than t_{LOW}.*

If this is not possible, a workaround can be used:

    Clear the ADDR flag

    Wait for the OVR flag to be set

    Clear OVR and write the first data byte.

Then the time window for writing the next data byte will be the time to transfer one byte. In this case, the master must discard the first received data byte.

2.8.6 Wrong data read into data register

In Master Receiver mode, when closing the communication using method 2, the content of the last read data can be corrupted. The following two sequences are concerned by the limitation:

● **Sequence 1:** Transfer sequence for master receiver when N = 2:

a) BTF = 1(Data N-1 in DR and Data N in shift register)

b) Program STOP = 1,

c) Read DR twice (Read Data N-1 and Data N) just after programming the STOP.

● **Sequence 2:** Transfer sequence for master receiver when N > 2:

a) BTF = 1 (Data N-2 in DR and Data N-1 in shift register)

b) Program ACK = 0,

c) Read DataN-2 in DR.

d) Program STOP = 1,

e) Read DataN-1.

If the user software is not able to read the data N-1 before the STOP condition is generated on the bus, the content of the shift register (data N) will be corrupted (data N is shifted 1-bit to the left).

Workarounds

● **Workaround 1**

Stretch the SCL line by configuring SCL I/O as a general purpose I/O, open-drain output low level, before the SET STOP in sequence 1 and before the READ Data N-2 in séquence 2. Then configure back the SCL I/O as alternate function open-drain after the READ Data N-1. The sequences become:

Sequence 1:

a) BTF = 1(Data N-1 in DR and Data N in shift register)

b) Configure SCL I/O as GPIO open-drain output low

c) Program STOP = 1

d) Read Data N-1

e) Configure SCL I/O as Alternate Function open drain

f) Read Data N

Sequence 2:

a)   BTF = 1 (Data N-2 in DR and Data N-1 in shift register)

b)   Program ACK = 0

c)   Configure SCL I/O as GPIO open-drain output low

d)   Read Data N-2 in DR.

e)   Program STOP = 1,

f)   Read Data N-1.

g)   Configure SCL I/O as Alternate Function open drain

● **Workaround 2**

Mask all active interrupts between the SET STOP and the READ data N-1 for sequence 1; and between the READ data N-2, the SET STOP and the READ data N-1 for Sequence 2.

● **Workaround 3**

Manage I2C RxNE events with DMA or interrupts with the highest priority level, so that the condition BTF = 1 never occurs.

2.9 USART peripheral

2.9.1 Idle frame is not detected if receiver clock speed is deviated

Description

If the USART receives an idle frame followed by a character, and the clock of the transmitter device is faster than the USART receiver clock, the USART receive signal falls too early when receiving the character start bit, with the result that the idle frame is not detected (IDLE flag is not set).

Workaround

None.

2.9.2 In full duplex mode, the Parity Error (PE) flag can be cleared by writing the data register

Description

In full duplex mode, when the Parity Error flag is set by the receiver at the end of a reception, it may be cleared while transmitting by reading the USART_SR register to check the TXE or TC flags and writing data in the data register.

Consequently, the software receiver can read the PE flag as '0' even if a parity error occurred.

Workaround

The Parity Error flag should be checked after the end of reception and before transmission.

2.9.3 Parity Error (PE) flag is not set when receiving in Mute mode using address mark detection

Description

The USART receiver is in Mute mode and is configured to exit the Mute mode using the address mark detection. When the USART receiver recognizes a valid address with a parity error, it exits the Mute mode without setting the Parity Error flag.

Workaround

None.

2.9.4 Break frame is transmitted regardless of nCTS input line status

Description

When CTS hardware flow control is enabled (CTSE = 1) and the Send Break bit (SBK) is set, the transmitter sends a break frame at the end of current transmission regardless of nCTS input line status.

Consequently, if an external receiver device is not ready to accept a frame, the transmitted break frame is lost.

Workaround

None.

2.9.5 nRTS signal abnormally driven low after a protocol violation

Description

When RTS hardware flow control is enabled, the nRTS signal goes high when a data is received. If this data was not read and a new data is sent to the USART anyway (protocol violation), the nRTS signal goes back to low level at the end of this new data. Consequently, the sender gets wrong information that the USART is ready to receive further data which is not really the case. On the USART side, an overrun is detected which indicates that some data has been lost.

Workaround

The lost data should be resent to the USART.

2.10 Timers

These limitations apply only to TIM1, TIM2, TIM3, TIM4 and TIM5.

2.10.1 Missing capture flag

Description

In capture mode, when a capture occurs while the CCRx register is being read, the capture flag (CCxIF) may be cleared without the overcapture flag (CCxOF) being set. The new data are actually captured in the capture register.

Workaround

An external interrupt can be enabled on the capture I/O just before reading the capture register (in the capture interrupt), and disabled just after reading the captured data. Possibly, a missed capture will be detected by the EXTI peripheral.

2.10.2 Overcapture detected too early

Description

In capture mode, the overcapture flag (CCxOF) can be set even though no data have been lost.

Conditions

If a capture occurs while the capture register is being read, an overcapture is detected even though the previously captured data are correctly read and the new data are correctly stored into the capture register.

The system is at the limit of an overcapture but no data are lost.

Workaround

None.

2.10.3 General-purpose timer: regulation for 100% PWM

Description

When the OCREF_CLR functionality is activated, the OCxREF signal becomes de-asserted (and consequently OCx is deasserted / OCxN is asserted) when a high level is applied on the OCREF_CLR signal. The PWM then restarts (output re-enabled) at the next counter overflow.

But if the PWM is configured at 100% (CCxR > ARR), then it does not restart and OCxREF remains de-asserted.

Workaround

None.

2.11 LSI clock stabilization time

Description

When the LSIRDY flag is set, the clock may still be out of the specified frequency range (f_{LSI} parameter, see LSI oscillator characteristics in the product datasheet).

Workaround

To have a fully stabilized clock in the specified range, a software temporization of 100 µs should be added.

Appendix A   Revision code on device marking

Figure 1, *Figure 2* and *Figure 3* show the marking compositions for the LQFP100, LQFP64 and LQFP48 packages, respectively. Only the Additional field containing the Revision code is shown.

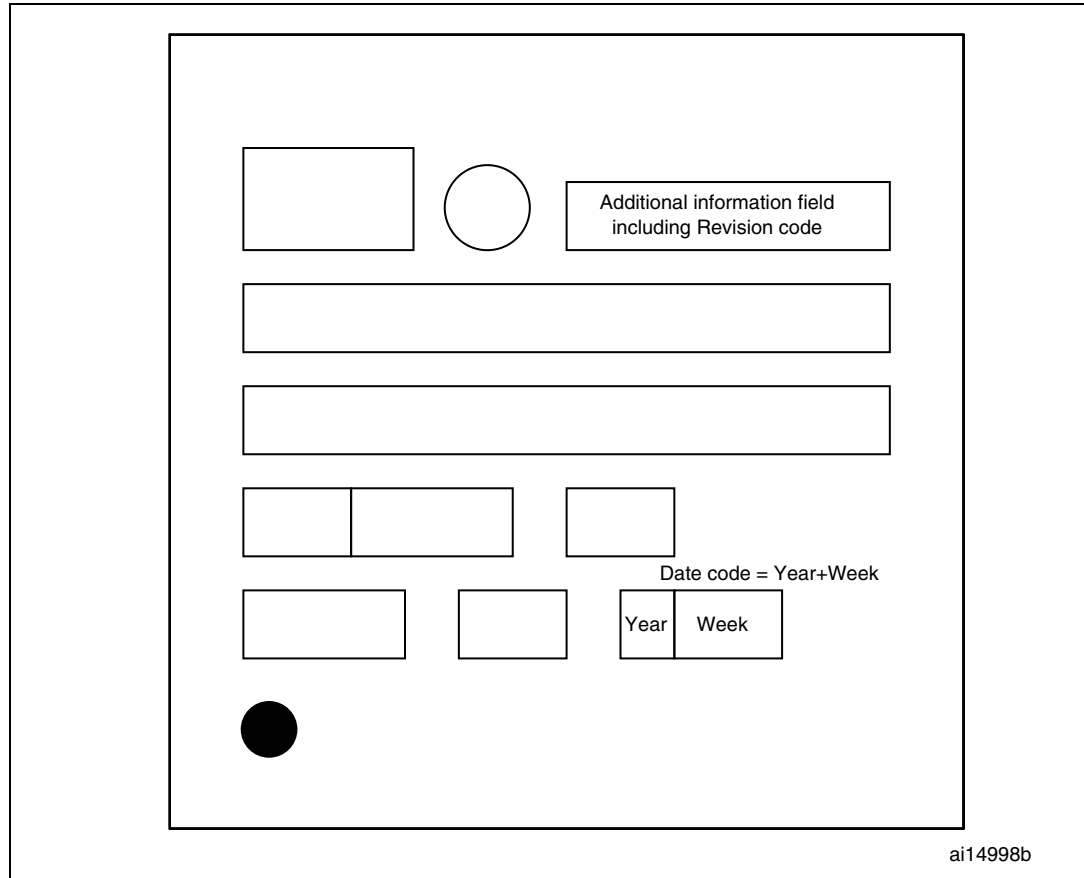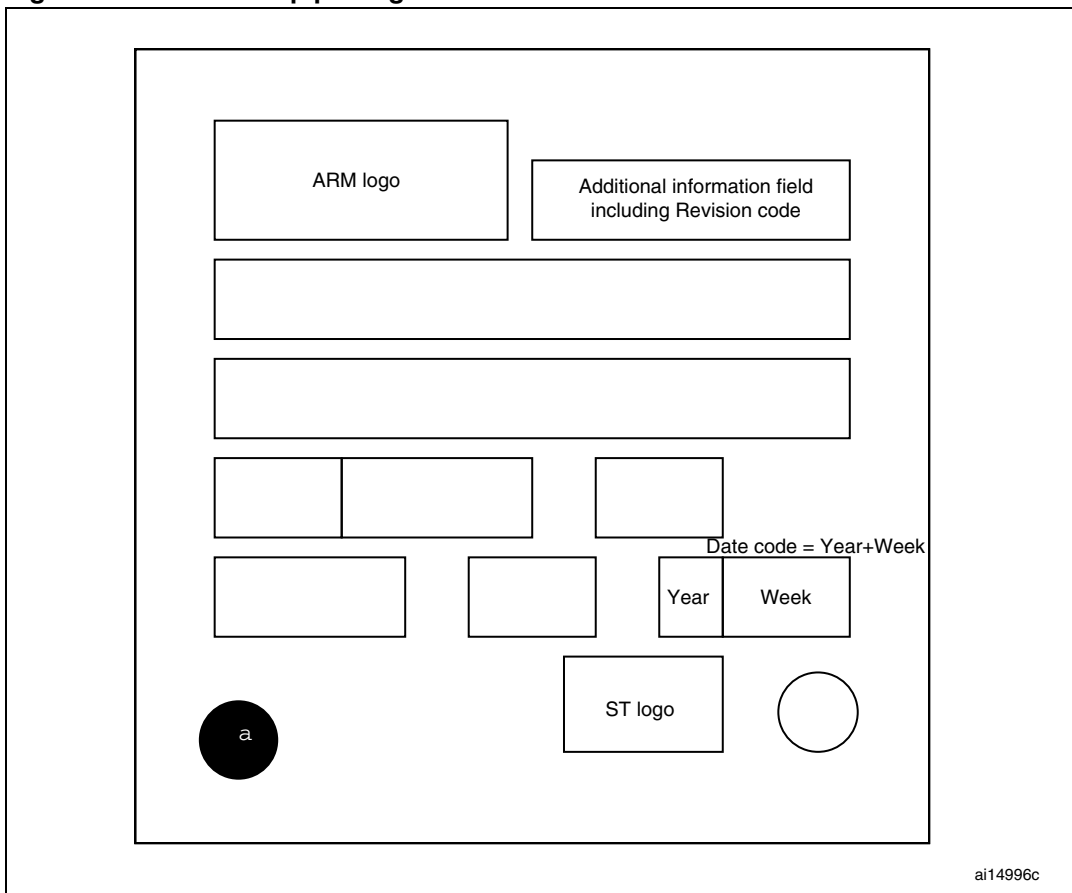**Figure 1.   LQFP100 top package view**

Figure 2. **LQFP64 top package view**

ARM logo

Additional information field
including Revision code

Date code = Year+Week

Year

Week

ST logo

a

ai14996c

Figure 3. LQFP48 top package view

Date code = Year+Week

Year | Week

Additional information field
including Revision code

ai14615c
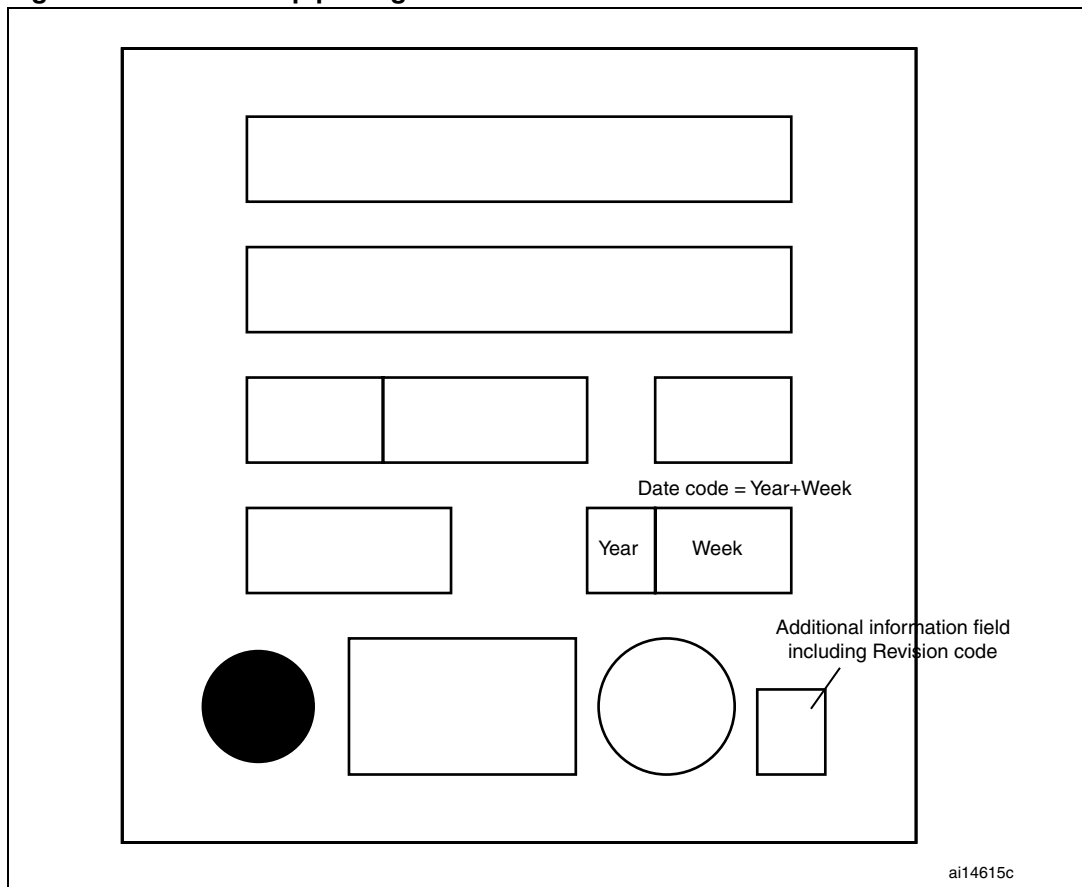
Revision history

Table 5.   Document revision history

Date	Revision	Changes
18-Dec-2009	1	Initial release.
03-May-2010	2	Updated for Rev Z. Removed section 2.8 "PB6 not 5 V-tolerant" Updated *Section 2.8: I2C peripheral*
18-Jun-2010	3	Added *Section 2.2: Debugging Stop mode and system tick timer* Added *Section 2.3: Debugging Stop mode with WFE entry* Modified *Section 2.10: Timers* Modified *Section 2.8.3: Wrong behavior of I2C peripheral in master mode after a misplaced Stop* Modified *Section 2.8.5: Data valid time (tVD;DAT) violated without the OVR flag being set* Added *Section 2.9: USART peripheral*
17-Dec-2010	4	Added *Section 2.4: Unique ID unavailability on devices with date code earlier than 045* Added *Section 2.9.5: nRTS signal abnormally driven low after a protocol violation*
22-Feb-2011	5	Updated workarounds in *Section 2.8.1: Some software events must be managed before the current byte is being transferred* and *Section 2.8.6: Wrong data read into data register*

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