r-type instructions

`add/and/or/slt/sub rd, rs, rt`

op 6 bits	rs 5 bits	rt 5 bits	rd 5 bits	shamt 5 bits	funct 6 bits
000000				00000	

funct field:

- `add: 100000`
- `and: 100100`
- `or: 100101`
- `slt: 101010`
- `sub: 100010`

---

i-type instructions

`lw/sw rt, imm($rs)`

`beq rs, rt, imm`

op 6 bits	rs 5 bits	rt 5 bits	immediate 16 bits

op field:

- `lw: 101011`
- `sw: 100011`
- `beq: 000100` (immediate is the number of instructions beyond the next one)

---

j-type instructions

op 6 bits	target address 26 bits
000010	

The target address field is the actual address divided by 4.