ES7210

High Performance Four Channels Audio ADC

FEATURES

- High performance multi-bit delta-sigma audio ADC
- 102 dB signal to noise ratio
- -85 dB THD+N
- 24-bit, 8 to 200 kHz sampling frequency
- I^2S/PCM master or slave serial data port
- Support TDM
- 256/384Fs, USB 12/24 MHz and other non standard audio system clocks
- Low power standby mode

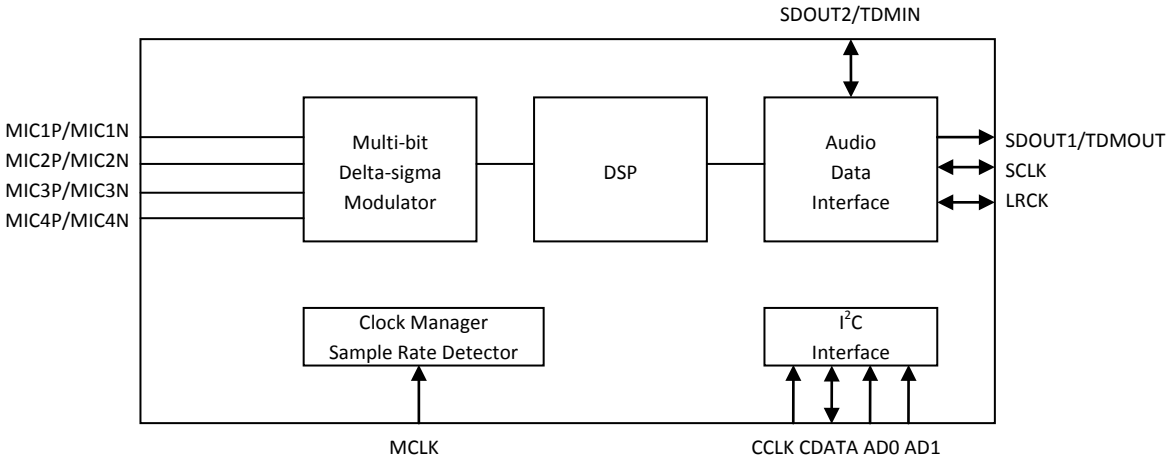
APPLICATIONS

- Mic array
- Smart speaker
- Far field voice capture

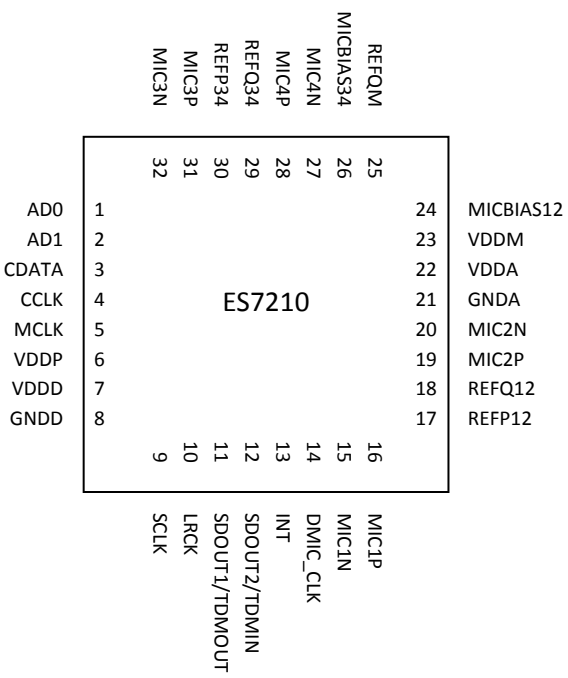
ORDERING INFORMATION

ES7210 -40°C ~ +85°C
QFN-32

BLOCK DIAGRAM

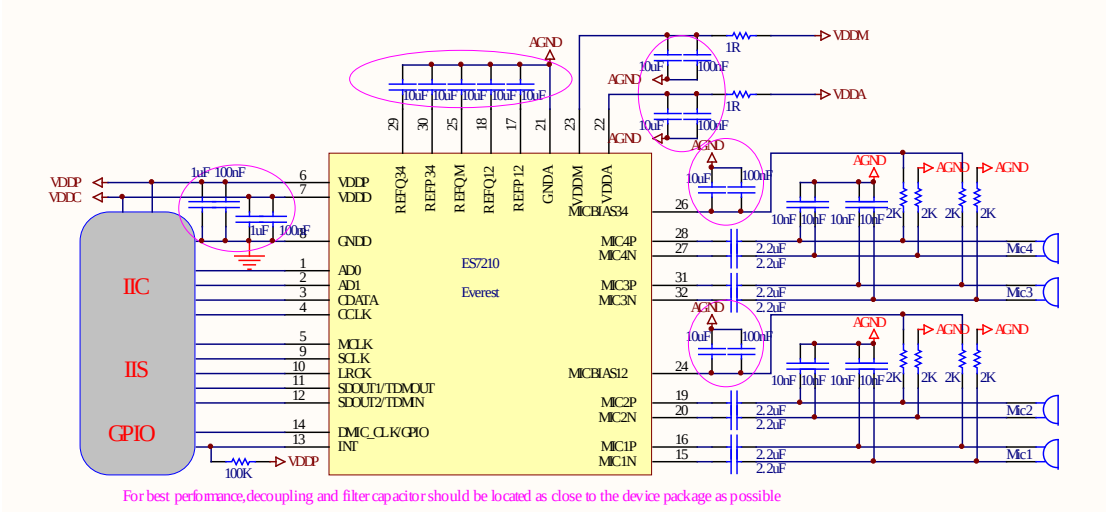


1. PIN OUT AND DESCRIPTION



Pin Name	Pin number	Input or Output	Pin Description
CCLK, CDATA	3, 4	I/O	I^2C clock and data
AD0, AD1	1, 2	I	I^2C address
MCLK	5	I	Master clock
SCLK	9	I/O	Serial data bit clock
LRCK	10	I/O	Serial data left and right channel frame clock
SDOUT1/TDMOUT SDOUT2/TDMIN	11 12	O I/O	Serial data output or TDM data input and output
INT	13	O	Interrupt
DMIC_CLK	14	I	Digital mic clock
MIC1P, MIC1N MIC2P, MIC2N MIC3P, MIC3N MIC4P, MIC4N	16, 15 19, 20 31, 32 28, 27	Analog	Mic input
MICBIAS12 MICBIAS34	24 26	Analog	Mic bias
VDDP	6	Analog	Power supply for the digital input and output
VDDD, GNDD	7, 8	Analog	Digital power supply
VDDA, GNDA	22, 21	Analog	Analog power supply
VDDM	23	Analog	Analog power supply
REFP12, REFP34	17, 30	Analog	Filtering capacitor connection
REFQ12, REFQ34	18, 29	Analog	Filtering capacitor connection
REFQM	25	Analog	Filtering capacitor connection

2. TYPICAL APPLICATION CIRCUIT



3. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and some common non standard audio clocks (25 MHz, 26 MHz, etc).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

4. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I^2C interface is a bi-directional serial bus that uses a serial data line (CDATA) and a serial clock line (CCLK) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1a and Figure 1b. Data are transmitted synchronously to CCLK clock on the CDATA line on a byte-by-byte basis. Each bit in a byte is sampled during CCLK high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the CDATA low. The transfer rate of this interface can be up to 400 kbps.

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at CDATA while CCLK is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at CDATA while CCLK is high.

In I^2C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I^2C Interface Mode

	Chip Address		R/W		Register Address		Data to be written		
start	001000	AD0	0	ACK	RAM	ACK	DATA	ACK	Stop

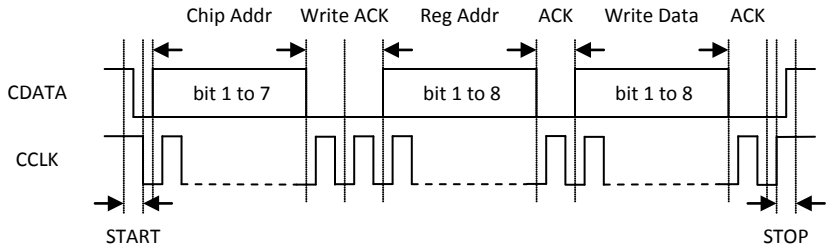


Figure 1a I^2C Write Timing

Table 2 Read Data from Register in I^2C Interface Mode

	Chip Address		R/W		Register Address		
Start	001000	AD0	0	ACK	RAM	ACK	
	Chip Address		R/W		Data to be read		
Start	001000	AD0	1	ACK	Data	NACK	Stop

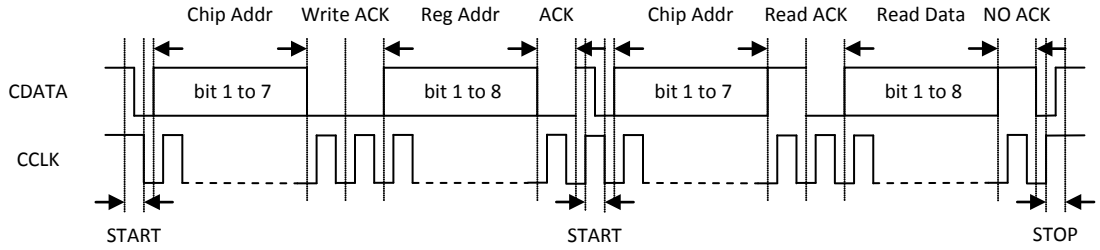


Figure 1b I^2C Read Timing

5. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the output from the ADC through LRCK, SCLK and SDOUT pins. These formats are I^2S, left justified, DSP/PCM mode and TDM. ADC data is out at SDOUT on the falling edge of SCLK. The relationships of SDOUT, SCLK and LRCK with these formats are shown through Figure 2a to Figure 2h. ES7210 can be cascaded up to 16-ch through single I^2S or TDM, please refer to the user guide for detail description.

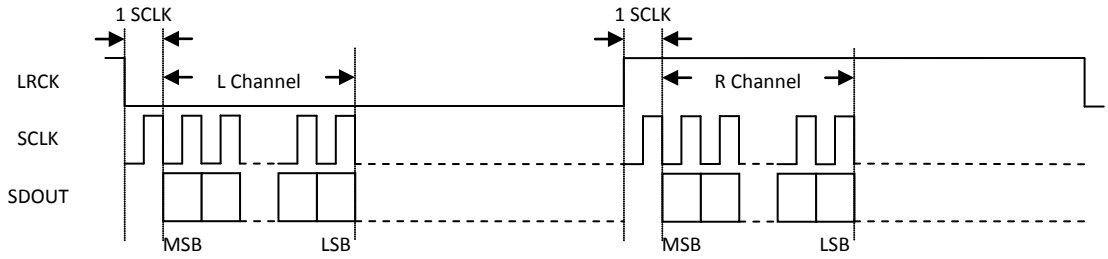


Figure 2a I^2S Serial Audio Data Format

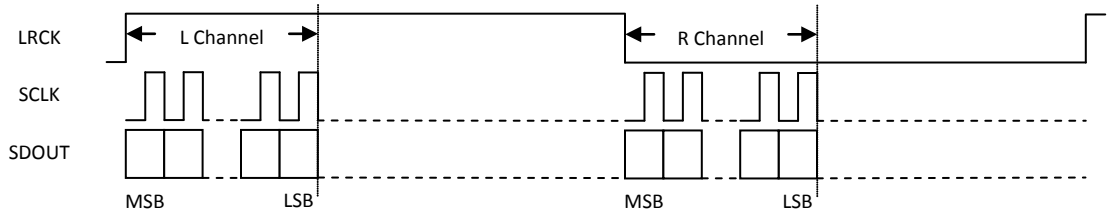


Figure 2b Left Justified Serial Audio Data Format

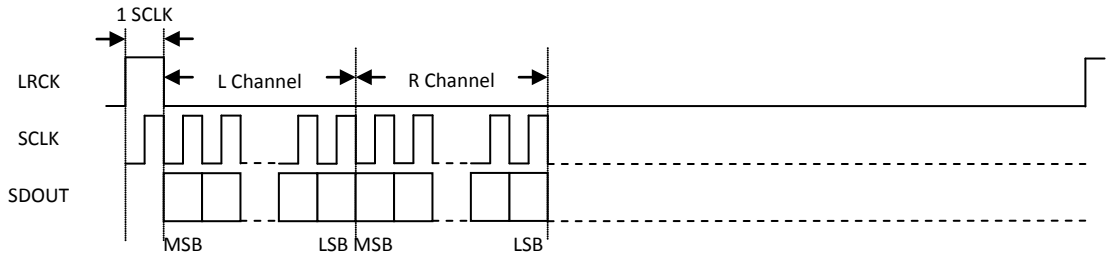


Figure 2c DSP/PCM Mode A Serial Audio Data Format

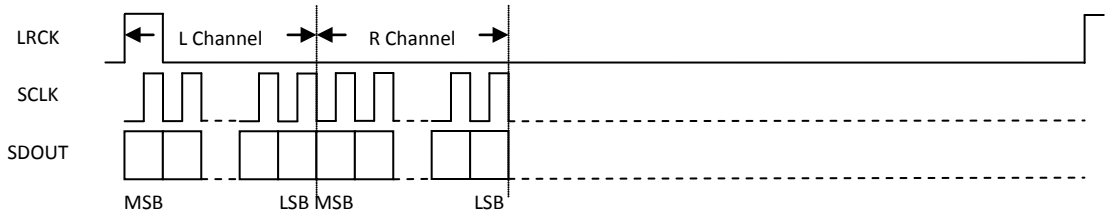


Figure 2d DSP/PCM Mode B Serial Audio Data Format

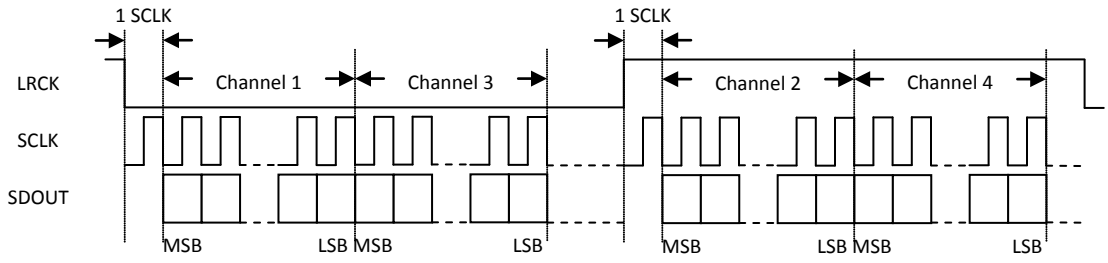


Figure 2e TDM I^{2}S Serial Audio Data Format

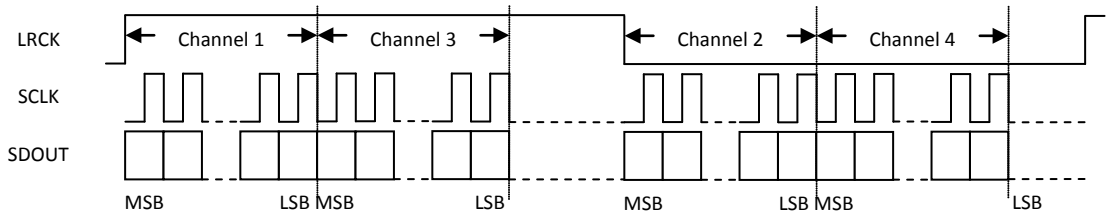


Figure 2f TDM Left Justified Serial Audio Data Format

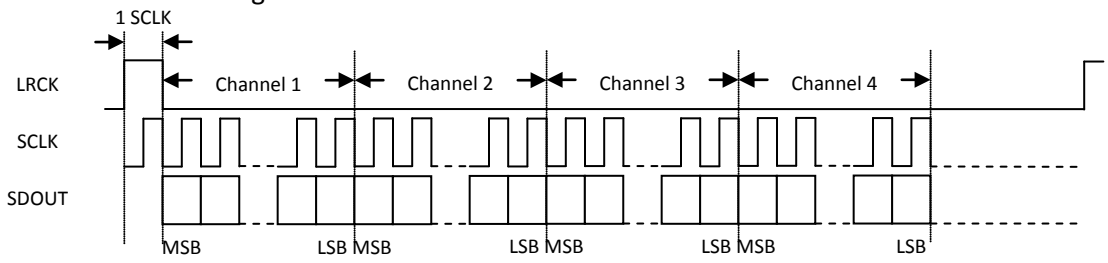


Figure 2g TDM DSP/PCM Mode A Serial Audio Data Format

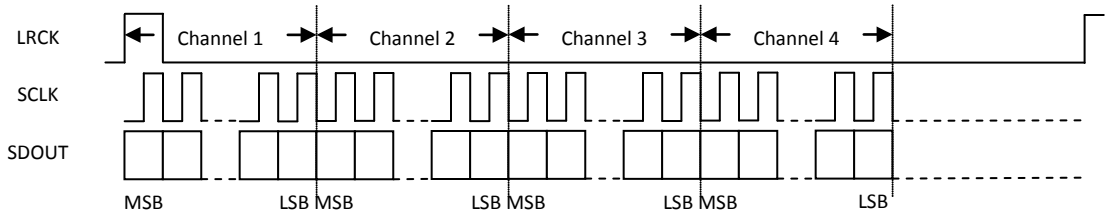


Figure 2h TDM DSP/PCM Mode B Serial Audio Data Format

6. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+5.0V
Digital Supply Voltage Level	-0.3V	+5.0V
Input Voltage Range	DGND-0.3V	DVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
VDDD	1.6	3.3	3.6	V
VDDP	1.6	3.3	3.6	V
VDDA	1.6	3.3	3.6	V
VDDM	1.6	3.3	3.6	V

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: VDDA=3.3V, VDDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	95	102	104	dB
THD+N	-88	-85	-75	dB
Channel Separation (1KHz)	95	100	105	dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
Filter Frequency Response – Quad Speed				
Passband	0		0.2083	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB

Stopband Attenuation	70			dB
Analog Input				
Full Scale Input Level		AVDD/3.3		Vrms
Input Impedance		6		KΩ

POWER CONSUMPTION CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
VDDD=3.3V, VDDP=3.3V, VDDA=3.3V		TBD		mA
Power Down Mode				
VDDD=3.3V, VDDP=3.3V, VDDA=3.3V		TBD		uA

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	T_{SCLKL}	15		ns
SCLK Pulse width high	T_{SCLKH}	15		ns
SCLK falling to LRCK edge	T_{SLR}	–10	10	ns
SCLK falling to SDOUT valid	T_{SDO}	0		ns

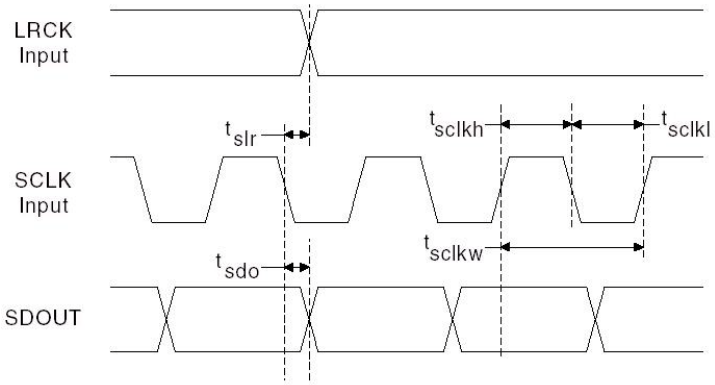


Figure 3 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		400	KHz
Bus Free Time Between Transmissions	T_{TWID}	1.3		us
Start Condition Hold Time	T_{TWSTH}	0.6		us
Clock Low time	T_{TWCL}	1.3		us
Clock High Time	T_{TWCH}	0.4		us
Setup Time for Repeated Start Condition	T_{TWSTS}	0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		900	ns
CDATA Setup time to CCLK Rising	T_{TWDS}	100		ns
Rise Time of CCLK	T_{TWR}		300	ns
Fall Time CCLK	T_{TWF}		300	ns

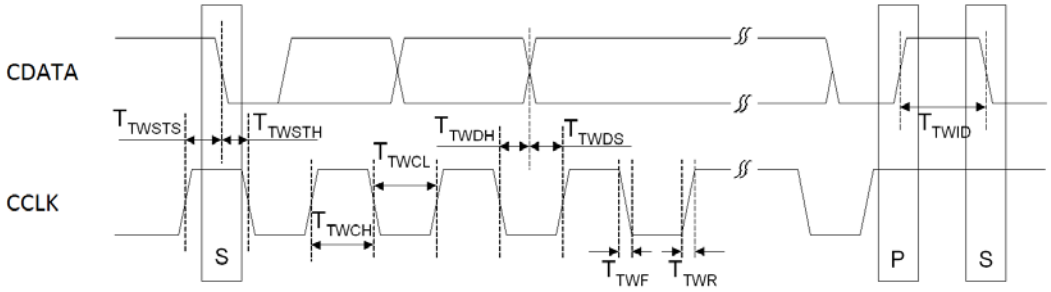


Figure 4 I²C Timing

7. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 – RESET CONTROL, DEFAULT 00110010

Bit Name	Bit	Description
Reserved	7	Reserved
RST_MSTGEN	6	0 – normal 1 – reset master mode LRCK and SCLK
RST_ADC34_DIG	5	0 – normal 1 – reset ADC34
RST_ADC12_DIG	4	0 – normal 1 – reset ADC12
SEQ_DIS	3	Auto power sequence 0 – enable 1 – disable
RST_REGS	2	0 – normal 1 – reset control registers (except this bit)
RST_DIG	1	0 – normal 1 – reset digital (except control registers)
CSM_ON	0	Chip state machine power down 0 – disable 1 – enable

REGISTER 0X01 – CLOCK OFF, DEFAULT 00100000

Bit Name	Bit	Description
Reserved	7	Reserved
EXT_SCLKLRCK_OFF	6	0 – turn on slave mode SCLK and LRCK internally 1 – turn off slave mode SCLK and LRCK internally
MASTER_CLK_OFF	5	0 – turn on master mode SCLK and LRCK 1 – turn off master mode SCLK and LRCK
ADC34_MCLK_OFF	4	0 – turn on ADC34 master clock 1 – turn off ADC34 master clock
ADC12_MCLK_OFF	3	0 – turn on ADC12 master clock 1 – turn off ADC12 master clock
ANA34_CLK_OFF	2	0 – turn on ADC34 analog clock 1 – turn off ADC34 analog clock
ANA12_CLK_OFF	1	0 – turn on ADC12 analog clock 1 – turn off ADC12 analog clock
MCLK_OFF	0	0 – turn on master clock 1 – turn off master clock

REGISTER 0X02 – MAIN CLOCK CONTROL, DEFAULT 00000010

Bit Name	Bit	Description
DLL_BYPASS	7	1 – bypass DLL 0 – not bypass DLL
CLKDBL_VALID	6	1 – use clock doubler 0 – not use clock doubler
Reserved	5	Reserved
CLK_ADC_DIV	4:0	ADC clock divide 0/1 – no divide 2 – divide by 2

		.... 31 – divide by 31

REGISTER 0X03 – MASTER CLOCK CONTROL, DEFAULT 00000100

Bit Name	Bit	Description
MSTCLK_SRCSEL	7	0 – MCLK from pad 1 – MCLK from clock doubler
M_SCLK_DIV	6:0	SCLK divide (use with MSTCLK_SRCSEL) 0/1 – no dived 2 – divide by 2 .... 127 – divide by 127

REGISTER 0X04 – MASTER LRCK DIVIDER 1, DEFAULT 00000001

Bit Name	Bit	Description
Reserved	7:4	Reserved
M_LRCK_DIVH	3:0	M_LRCK_DIV[11:8]

REGISTER 0X05 – MASTER LRCK DIVIDER 0, DEFAULT 00000000

Bit Name	Bit	Description
M_LRCK_DIVL	7:0	M_LRCK_DIV[7:0]

REGISTER 0X06 – POWER DOWN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:3	Reserved
DLL_POWER_DOWN	2	0 – normal 1 – power down DLL (stop MCLK first)
TDMIN_PDN_OFF	1	TDMIN pin internal pull down resister 1 – off 0 – on
PUPDN_OFF	0	Pin internal pull down resistors (except TDMIN pin) 1 – off 0 – on

REGISTER 0X07 – ADC OSR CONFIG, DEFAULT 00100000

Bit Name	Bit	Description
Reserved	7:6	Reserved
ADC_OSR	5:0	ADC over sampling ratio

REGISTER 0X08 – MODE CONFIG, DEFAULT 00010000

Bit Name	Bit	Description
LRCK_RATE_MODE	7:4	When set SDOUT_MODE=11 0/1 – 2 channels 2 – 4 channels 3 – 6 channels 4 – 8 channels 5 – 10 channels 6 – 12 channels 7 – 14 channels

		8 – 16 channels Other – reserved
SCLK_INV_MODE	3	0 – normal 1 – SCLK inverted
EQ_OFF	2	0 – EQ on 1 – EQ off
SPEED_MODE	1	0 – Single speed mode 1 – Double speed mode
MS_MODE	0	LRCK/SCLK clock mode 0 – slave mode 1 – master mode

REGISTER 0X09 – TIME CONTROL 0 FOR CHIP INITIALIZATION, DEFAULT 01000000

Bit Name	Bit	Description
CHIPINI_LGTH	7:0	Chip initial state period control: period=CHIPINI_LGTH/(LRCK frequency)*16

REGISTER 0X0A – TIME CONTROL 1 FOR CHIP INITIALIZATION, DEFAULT 01000000

Bit Name	Bit	Description
PWRUP_LGTH	7:0	Power up state period control: period=PWRUP_LGTH/(LRCK frequency)*16

REGISTER 0X0B – CHIP STATUS, DEFAULT 00000000

Bit Name	Bit	Description
CLEAR_RAM	7	0 – normal 1 – clear DSP ram
FORCE_CSM	6:4	Force chip state machine 100 – force to power down 101 – force to chip initial 110 – force to normal 111 – force to power up 0xx – no force
ADC34_MUTE_FLAG	3	0 – no automute 1 – ADC34 automute set by ADC34_AUTOMUTE_SEL
ADC12_MUTE_FLAG	2	0 – no automute 1 – ADC12 automute set by ADC12_AUTOMUTE_SEL
CSM_STATE	1:0	Chip state machine state

REGISTER 0X0C – INTERRUPT CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:4	Reserved
INT_PULSESIZE	3:2	00 – 256 LRCK 01 – 128 LRCK 10 – 32 LRCK 11 – 8 LRCK
INT_ENABLE[1]	1	0 – disable ADC34 interrupt 1 – enable ADC34 interrupt
INT_ENABLE[0]	0	0 – disable ADC12 interrupt 1 – enable ADC12 interrupt

REGISTER 0X0D – MISC. CONTROL, DEFAULT 00001001

Bit Name	Bit	Description
Reserved	7:6	Reserved
I2C_IBTHD_SEL	5	0 – normal I^2C input hysteresis 1 – larger I^2C input hysteresis
CLKDBL_PW_SEL	4	0 – normal clock doubler duty cycle 1 – smaller clock doubler duty cycle
CLKDBL_PATH_SEL	3	Clock doubler path select (internal use)
LRCK_EXTEND	2	0 – normal internal LRCK pulse width 1 – larger internal LRCK pulse width
DELAY_SEL	1:0	Internal delay cell delay select: 00 – 0ns 01 – 5ns 10 – 10ns 11 – 5ns

REGISTER 0X10 – DMIC CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC34_DMIC_ON	7	0 – DMIC off 1 – DMIC on
ADC12_DMIC_ON	6	0 – DMIC off 1 – DMIC on
ADC34_DMIC_GAIN	5:3	000 – 0dB gain 001 – 6dB gain 010 – 12dB gain 011 – 18dB gain 100 – 24dB gain 101 – 30dB gain 110 – 36dB gain 111 – 42dB gain
ADC12_DMIC_GAIN	2:0	000 – 0dB gain 001 – 6dB gain 010 – 12dB gain 011 – 18dB gain 100 – 24dB gain 101 – 30dB gain 110 – 36dB gain 111 – 42dB gain

REGISTER 0X11 – SDP INTERFACE CONFIG 1, DEFAULT 00000000

Bit Name	Bit	Description
SP_WL	7:5	000 – 24-bit 001 – 20-bit 010 – 18-bit 011 – 16-bit 100 – 32-bit
SP_LRP	4	I^2S/Left Justified: 0 – L/R normal polarity Left/Right=High/Low (Left Justified) Left/Right=Low/High (I^2S) 1 – L/R invert polarity

		Left/Right=Low/High (Left Justified) Left/Right=High/Low (I^2S) DSP/PCM mode: 0 – mode A 1 – mode B
Reserved	3:2	
SP_PROTOCAL	1:0	00 – I^2S 01 – Left Justified 10 – reserved 11 – DSP mode

REGISTER 0X12 – SDP INTERFACE CONFIG 2, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7	Reserved
ISCLKLRCK_SEL	6	0 – normal 1 – use master mode SCLK/LRCK to power up
SP_SDOUT2_TRI	5	0 – normal 1 – SDOUT2 tri state
SP_SDOUT1_TRI	4	0 – normal 1 – SDOUT1 tri state
SCLKLRCK_TRI	3	0 – normal 1 – SCLK/LRCK tri state
CASCADE_CHIPFLAG	2	When set SDOUT_MODE=11 0 – last ES7210 in TDM 1 – not the last ES7210 in TDM
SDOUT_MODE	1:0	00 – ADC12 to SDOUT1, ADC34 to SDOUT2 01 – TDM DSP/PCM 10 – TDM I^2S/Left Justified 11 – multiple LRCK TDM

REGISTER 0X13 – ADC AUTOMUTE CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:4	Reserved
AUTOMUTE_ADC34_MUTE	3	0 – normal 1 – auto mute ADC34
AUTOMUTE_ADC12_MUTE	2	0 – normal 1 – auto mute ADC12
ADC_AUTOMUTE_SIZE	1:0	auto mute window size 00 – 2048 LRCK 01 – 4096 LRCK 10 – 8192 LRCK 11 – 16384 LRCK

REGISTER 0X14 – ADC34 MUTE CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC34_AUTOMUTE_NG	7:4	ADC auto mute noise gate 0000 – -96dB 0001 – -90dB 0010 – -84dB 0011 – -78dB

		0100 – -72dB 0101 – -66dB 0110 – -60dB 0111 – -54dB 1000 – -51dB 1001 – -48dB 1010 – -45dB 1011 – -42dB 1100 – -39dB 1101 – -36dB 1110 – -33dB 1111 – -30dB
ADC34_AUTOMUTE_SEL	3:2	00 – normal 10 – select left data as left channel automute 01 – select right data as right channel automute 11 – select stereo automute
ADC4_SWMUTE_SEL	1	0 – normal 1 – mute ADC4 output to all 0
ADC3_SWMUTE_SEL	0	0 – normal 1 – mute ADC3 output to all 0

REGISTER 0X15 – ADC12 MUTE CONTROL, DEFAULT 00000000

Bit Name	Bit	Description
ADC12_AUTOMUTE_NG	7:4	ADC auto mute noise gate 0000 – -96dB 0001 – -90dB 0010 – -84dB 0011 – -78dB 0100 – -72dB 0101 – -66dB 0110 – -60dB 0111 – -54dB 1000 – -51dB 1001 – -48dB 1010 – -45dB 1011 – -42dB 1100 – -39dB 1101 – -36dB 1110 – -33dB 1111 – -30dB
ADC12_AUTOMUTE_SEL	3:2	00 – normal 10 – select left data as left channel automute 01 – select right data as right channel automute 11 – select stereo automute
ADC2_SWMUTE_SEL	1	0 – normal 1 – mute ADC2 output to all 0
ADC1_SWMUTE_SEL	0	0 – normal 1 – mute ADC1 output to all 0

REGISTER 0X16 – ALC SELECT, DEFAULT 00000000

Bit Name	Bit	Description

Reserved	7:4	Reserved
ALC34_SEL	3:2	ADC34 ALC select 00 – ALC off 10 – left channel ALC 01 – right channel ALC 11 – stereo ALC
ALC12_SEL	1:0	ADC12 ALC select 00 – ALC off 10 – left channel ALC 01 – right channel ALC 11 – stereo ALC

REGISTER 0X17 – ALC COMMON CONFIG 1, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7	Reserved
ALC_AUTOMUTE_GAIN	6:4	ALC gain control when automute happen 000 – 0dB 001 – -4dB 010 – -8dB 011 – -12dB 100 – -16dB 101 – -20dB 110 – -24dB 111 – -28dB
ALC_RAMP_RATE	3:0	ADC VC/ALC ramp rate 0 – 0.25dB/2LRCK 1 – 0.25dB/4LRCK 2 – 0.25dB/8LRCK ..... 14 – 0.25dB/32768LRCK 15 – 0.25dB/65536LRCK

REGISTER 0X18 – ADC34 ALC LEVEL, DEFAULT 11110111

Bit Name	Bit	Description
ALC34_MAXLEVEL	7:4	ALC max level 15 – -6.0 dB 14 – -6.6 dB 13 – -7.2 dB 12 – -7.8 dB 11 – -8.5 dB 10 – -9.3 dB 9 – -10.1dB 8 – -11.0dB 7 – -12.0dB 6 – -13.2dB 5 – -14.5dB 4 – -16.1dB 3 – -18.1dB 2 – -20.6dB 1 – -24.1dB 0 – -30.1dB

ALC34_MINLEVEL	3:0	ALC min level 15 – -6.0 dB 14 – -6.6 dB 13 – -7.2 dB 12 – -7.8 dB 11 – -8.5 dB 10 – -9.3 dB 9 – -10.1dB 8 – -11.0dB 7 – -12.0dB 6 – -13.2dB 5 – -14.5dB 4 – -16.1dB 3 – -18.1dB 2 – -20.6dB 1 – -24.1dB 0 – -30.1dB

REGISTER 0X19 – ADC12 ALC LEVEL, DEFAULT 11110111

Bit Name	Bit	Description
ALC12_MAXLEVEL	7:4	ALC max level 15 – -6.0 dB 14 – -6.6 dB 13 – -7.2 dB 12 – -7.8 dB 11 – -8.5 dB 10 – -9.3 dB 9 – -10.1dB 8 – -11.0dB 7 – -12.0dB 6 – -13.2dB 5 – -14.5dB 4 – -16.1dB 3 – -18.1dB 2 – -20.6dB 1 – -24.1dB 0 – -30.1dB
ALC12_MINLEVEL	3:0	ALC min level 15 – -6.0 dB 14 – -6.6 dB 13 – -7.2 dB 12 – -7.8 dB 11 – -8.5 dB 10 – -9.3 dB 9 – -10.1dB 8 – -11.0dB 7 – -12.0dB 6 – -13.2dB 5 – -14.5dB 4 – -16.1dB 3 – -18.1dB 2 – -20.6dB

		1 – -24.1dB 0 – -30.1dB

REGISTER 0X1A – ALC COMMON CONFIG2, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7	Reserved
DIRECT_RAMP_RATE	6:4	ALC current gain to automute gain or direct dB (ALC off) soft ramp 0 – off 1 – 0.5dB/4LRCK 2 – 0.5dB/8LRCK ..... 7 – 0.5dB/256LRCK
Reserved	3:2	Reserved
ADC34_SAME_GAINON	1	0 – ADC3 and ADC4 use independent direct DB setting 1 – ADC3 and ADC4 use ADC3 direct DB setting
ADC12_SAME_GAINON	0	0 – ADC3 and ADC4 use independent direct dB setting 1 – ADC3 and ADC4 use ADC3 direct dB setting

REGISTER 0X1B – ADC4 MAX GAIN, DEFAULT 10111111

Bit Name	Bit	Description
ADC4_DIRECT_DB	7:0	ADC4 direct dB (ALC off) or ALC max gain 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X1C – ADC3 MAX GAIN, DEFAULT 10111111

Bit Name	Bit	Description
ADC3_DIRECT_DB	7:0	ADC3 direct dB (ALC off) or ALC max gain 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X1D – ADC2 MAX GAIN, DEFAULT 10111111

Bit Name	Bit	Description
ADC2_DIRECT_DB	7:0	ADC2 direct dB (ALC off) or ALC max gain 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X1E – ADC1 MAX GAIN, DEFAULT 10111111

Bit Name	Bit	Description
ADC1_DIRECT_DB	7:0	ADC1 direct dB (ALC off) or ALC max gain 00h – -95.5dB 01h – -95dB …… BFh – 0dB …… FFh – +32dB

REGISTER 0X20 – ADC34 HPF2, DEFAULT 00100110

Bit Name	Bit	Description
ADC34_CROSS	7:6	00 – normal 01 – left channel to both left and right channels 10 – right channel to both left and right channels 11 – left and right channel output switch
ADC34_USE_ADC12SW	5	0 – ADC34 use its own offset freeze control 1 – ADC34 use ADC12's offset refresh control
ADC34_HPF_COEF2	4:0	HPF filter coefficient 2 5'b00110 – fast setting 5'b01101 – slow setting

REGISTER 0X21 – ADC34 HPF1, DEFAULT 00100110

Bit Name	Bit	Description
ADC34_4_POLARINV	7	0 – normal 1 – output invert
ADC34_3_POLARINV	6	0 – normal 1 – output invert
ADC34_OFFSET_REFRESHSW	5	0 – ADC HPF offset auto update 1 – ADC HPF offset freeze
ADC34_HPF_COEF1	4:0	HPF filter coefficient 1 5'b00110 – fast setting 5'b01101 – slow setting

REGISTER 0X22 – ADC12 HPF1, DEFAULT 00000110

Bit Name	Bit	Description
ADC12_CROSS	7:6	00 – normal 01 – left channel to both left and right channels 10 – right channel to both left and right channels 11 – left and right channel output switch
Reserved	5	0 – ADC34 use its own offset freeze control 1 – ADC34 use ADC12's offset refresh control
ADC12_HPF_COEF2	4:0	HPF filter coefficient 2 5'b00110 – fast setting 5'b01101 – slow setting

REGISTER 0X23 – ADC12 HPF2, DEFAULT 00100110

Bit Name	Bit	Description
ADC12_2_POLARINV	7	0 – normal 1 – output invert

ADC12_1_POLARINV	6	0 – normal 1 – output invert
ADC12_OFFSET_REFRESHSW	5	0 – ADC HPF offset auto update 1 – ADC HPF offset freeze
ADC12_HPF_COEF1	4:0	HPF filter coefficient 1 5'b00110 – fast setting 5'b01101 – slow setting

REGISTER 0X24 TO 3X37 – EQ COEFFICIENTS AUTOMATICLLY GENERATED BY MATLAB

REGISTER 0X3D – CHIP ID1, DEFAULT 01110010

Bit Name	Bit	Description
Chip_number_id1	7:0	Chip ID

REGISTER 0X3E – CHIP ID0, DEFAULT 00010000

Bit Name	Bit	Description
Chip_number_id0	7:0	Chip ID

REGISTER 0X3F – CHIP VERSION, DEFAULT 00000000

Bit Name	Bit	Description
Chip_version_id1	7:4	Version ID
Chip_version_id0	3:0	Version ID

REGISTER 0X40 – ANALOG SYSTEM, DEFAULT 10000000

Bit Name	Bit	Description
PDN_ANA	7	0 – normal 1 – power down analog
VX2OFF	6	Internal voltage selection 0 – turn on 1 – turn off (recommended when VDDA=3.3V
VX1SEL	5	Internal voltage selection 0 – 1.45x2 1 – 1.65 (recommended when VDDA=1.8V)
Reserved	4	Reserved
VMIDLOW	3:2	Lower Vmid option 00 – VDDA/2 01 – (0.9-0.075) V, when VDDA=1.8V 10 – (0.9-0.125) V, when VDDA=1.8V 01 – (0.9-0.175) V, when VDDA=1.8V
VMIDSEL	1:0	00 – Vmid disabled 01 – 50 kΩ divider enabled 10 – 500 kΩ divider enabled 11 – 5 kΩ divider enabled

REGISTER 0X41 – MIC1/2 BIAS, DEFAULT 01110001

Bit Name	Bit	Description
Reserved	7	Reserved
LVL_MICBIAS12	6:4	111 – 2.87V (VDDM=3.3V) 110 – 2.78V

		101 – 2.66V 100 – 2.55V 011 – 2.45V 010 – 2.36V 001 – 2.26V 000 – 2.18V
Reserved	3	Reserved
PGA12BIAS_SWH	2	0 – reference bias current 12.5uA 1 – reference bias current 15uA
ADC12BIAS_SWH	1:0	00 – reference bias current x1 01 – reference bias current x1.5 10 – reference bias current x1.25 11 – reference bias current x1.125

REGISTER 0X42 – MIC3/4 BIAS, DEFAULT 01110001

Bit Name	Bit	Description
Reserved	7	Reserved
LVL_MICBIAS34	6:4	111 – 2.87V (VDDM=3.3V) 110 – 2.78V 101 – 2.66V 100 – 2.55V 011 – 2.45V 010 – 2.36V 001 – 2.26V 000 – 2.18V
Reserved	3	Reserved
PGA34BIAS_SWH	2	0 – reference bias current 12.5uA 1 – reference bias current 15uA
ADC34BIAS_SWH	1:0	00 – reference bias current x1 01 – reference bias current x1.5 10 – reference bias current x1.25 11 – reference bias current x1.125

REGISTER 0X43 – MIC1 GAIN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC1	4	0 – deselect 1 – select MIC1P and MIC1N as input
MIC1GAIN_SETTING	3:0	0 – 0dB 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB 11 – 33dB 12 – 34.5dB

		13 – 36dB 14 – 37.5dB

REGISTER 0X44 – MIC2 GAIN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC2	4	0 – deselect 1 – select MIC2P and MIC2N as input
MIC2GAIN_SETTING	3:0	0 – 0dB 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB 11 – 33dB 12 – 34.5dB 13 – 36dB 14 – 37.5dB

REGISTER 0X45 – MIC3 GAIN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC3	4	0 – deselect 1 – select MIC3P and MIC3N as input
MIC3GAIN_SETTING	3:0	0 – 0dB 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB 11 – 33dB 12 – 34.5dB 13 – 36dB 14 – 37.5dB

REGISTER 0X46 – MIC4 GAIN, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
SELMIC4	4	0 – deselect 1 – select MIC4P and MIC4N as input
MIC4GAIN_SETTING	3:0	0 – 0dB

		1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB 11 – 33dB 12 – 34.5dB 13 – 36dB 14 – 37.5dB

REGISTER 0X47 – MIC1 LOW POWER, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:6	Reserved
LP_VRP12	5	0 – normal 1 – low power
LP_PGA1OUT	4	0 – normal 1 – low power
LP_PGA1	3	0 – normal 1 – low power
LP_VCMMOD1	2	0 – normal 1 – low power
LP_FLASH1	1	0 – normal 1 – low power
LP_INT11	0	0 – normal 1 – low power

REGISTER 0X48 – MIC2 LOW POWER, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
LP_PGA2OUT	4	0 – normal 1 – low power
LP_PGA2	3	0 – normal 1 – low power
LP_VCMMOD2	2	0 – normal 1 – low power
LP_FLASH2	1	0 – normal 1 – low power
LP_INT12	0	0 – normal 1 – low power

REGISTER 0X49 – MIC3 LOW POWER, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:6	Reserved
LP_VRP34	5	0 – normal 1 – low power

LP_PGA3OUT	4	0 – normal 1 – low power
LP_PGA3	3	0 – normal 1 – low power
LP_VCMMOD3	2	0 – normal 1 – low power
LP_FLASH3	1	0 – normal 1 – low power
LP_INT13	0	0 – normal 1 – low power

REGISTER 0X4A – MIC4 LOW POWER, DEFAULT 00000000

Bit Name	Bit	Description
Reserved	7:5	Reserved
LP_PGA4OUT	4	0 – normal 1 – low power
LP_PGA4	3	0 – normal 1 – low power
LP_VCMMOD4	2	0 – normal 1 – low power
LP_FLASH4	1	0 – normal 1 – low power
LP_INT14	0	0 – normal 1 – low power

REGISTER 0X4B – MIC1/2 POWER DOWN, DEFAULT 11111111

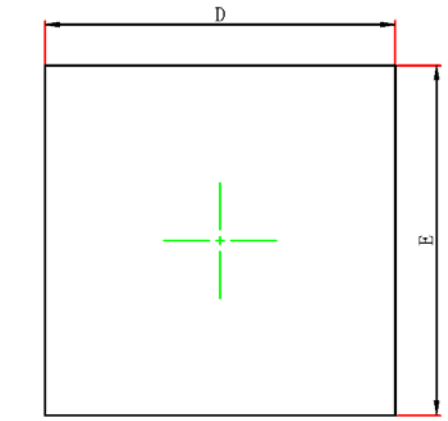
Bit Name	Bit	Description
PDN_ADC12VREFGEN	7	0 – normal 1 – MIC1/2 reference power down
PDN_MICBIAS12	6	0 – normal 1 – MICBIAS12 power down
PDN_PGA2	5	0 – normal 1 – PGA2 power down
PDN_PGA1	4	0 – normal 1 – PGA1 power down
PDN_MOD2	3	0 – normal 1 – ADC2 power down
PDN_MOD1	2	0 – normal 1 – ADC1 power down
MODTOP2_RST	1	0 – normal 1 – reset ADC2 state machine to power down state
MODTOP1_RST	0	0 – normal 1 – reset ADC1 state machine to power down state

REGISTER 0X4C – MIC3/4 POWER DOWN, DEFAULT 11111111

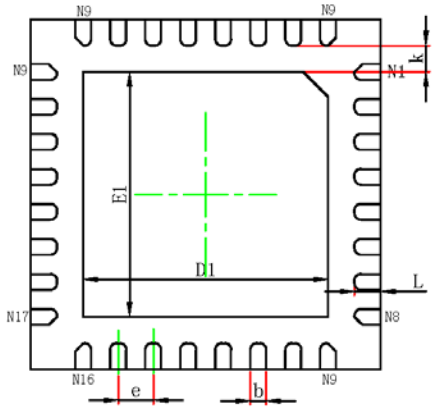
Bit Name	Bit	Description
PDN_ADC34VREFGEN	7	0 – normal 1 – MIC3/4 reference power down
PDN_MICBIAS34	6	0 – normal 1 – MICBIAS34 power down

PDN_PGA4	5	0 – normal 1 – PGA4 power down
PDN_PGA3	4	0 – normal 1 – PGA3 power down
PDN_MOD4	3	0 – normal 1 – ADC4 power down
PDN_MOD3	2	0 – normal 1 – ADC3 power down
MODTOP4_RST	1	0 – normal 1 – reset ADC4 state machine to power down state
MODTOP3_RST	0	0 – normal 1 – reset ADC3 state machine to power down state

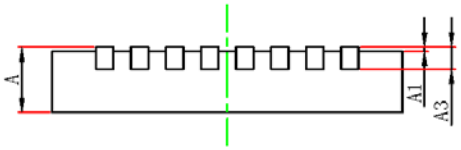
8. PACKAGE



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.700	2.900	0.106	0.114
E1	2.700	2.900	0.106	0.114
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
L	0.224	0.376	0.009	0.015

9. CORPORATE INFORMATION

Everest Semiconductor Co., Ltd.

No. 1355 Jinjihu Drive, Suzhou Industrial Park, Jiangsu, P.R. China, Zip Code 215021

苏州工业园区金鸡湖大道 1355 号国际科技园, 邮编 215021

Email: info@everest-semi.com

单击下面可查看定价，库存，交付和生命周期等信息

>>Everest-Semi(顺芯)