



CSE7759 User's manual

Rev.1.1

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History modify records

time	recording	version number
<u>2012-10-22</u> Original	Issue	1.0
2016-09-28 1. increase V1P , V1N with V2P pin Foot Description Description	2. modify V1P , V1N with V2P Limit Ratings	1.1

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1 Chip Function

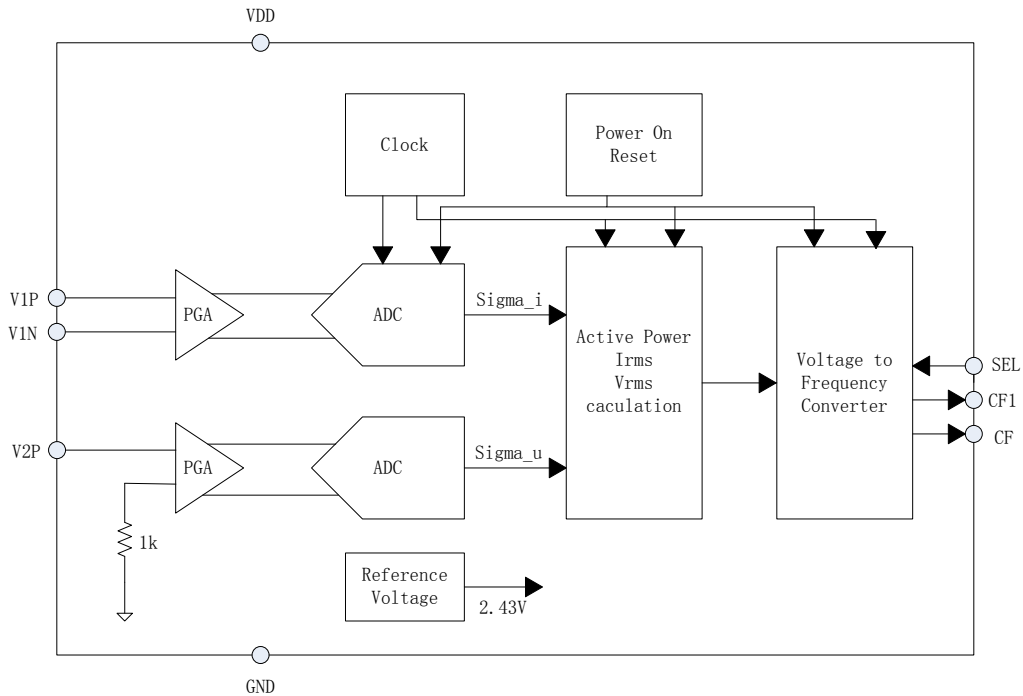
CSE7759 Single phase multi-function measurement chip, which provides high frequency pulses CF High frequency electrical energy for metering and CF1 For indicating a current or voltage rms rms. The chips SOP8 Package.

1.1 The main characteristics of the chip functions

1. High-frequency pulse CF Indicating active power, meet 50 / 60Hz IEC 687/1036 Standard accuracy requirements, 1000: 1 Within a range of up to $\pm 0.2\%$ Accuracy.
2. High-frequency pulse CF1 , May be configured to output current effective value or RMS voltage, in 500: 1 Within a range of up to $\pm 0.5\%$ Accuracy.
3. Built-in power supply monitoring circuit when the low power supply voltage to the 4V When the chip enters the reset state.
4. Internal 2.43V A voltage reference source.
5. 5V Single supply current is less than 3mA .
6. The main application areas: the need to measure the voltage, current and power applications, such as a single-phase multi-function meter, the metering plug Block, DRO like.

1.2 Chip structure described

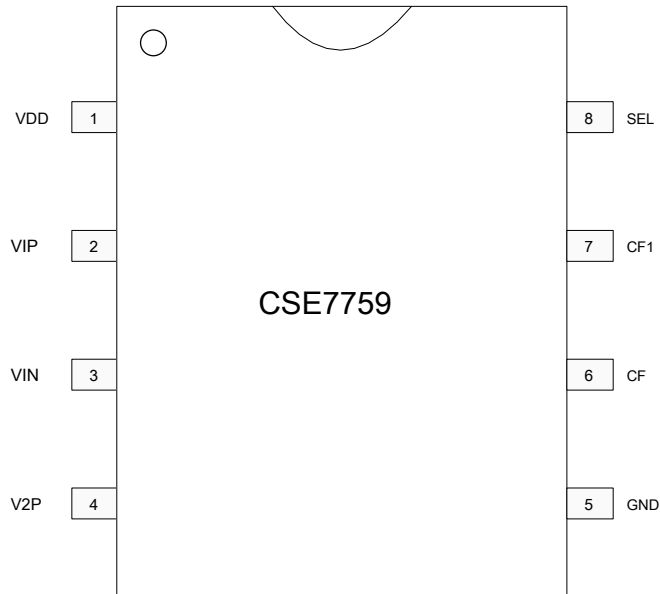
CSE7759 Functional block diagram of FIG. 1 Fig.



Map 1 Chip Functional Block Diagram

1.3 Chip Pin Description

CSE7759 use SOP8 Package.



Map 2 Chip pin map

table 1 CSE7759 Pin Description

Pin Number	Pin Name	input Output	Explanation
1	VDD	Chip power supply	Chip power supply
2, 3	V1P, V1N	Entry	Current differential signal input terminal, the maximum differential input signal $\pm 43.75\text{mV}$ NOTE: When not in use a current signal, V1P with V1N To receive short GND
4	V2P	Entry	Voltage signal having a positive input terminal. The maximum input signal $\pm 700\text{mV}$ NOTE: When a voltage signal is not used, V2P To receive short GND
5	GND	Chip ground	Chip ground
6	CF	Export	Active high-frequency pulse output, the duty cycle 50%
7,	CF1	Export	SEL = 0 Rms output current, the duty cycle 50% ; SEL = 1 , RMS output voltage, the duty cycle 50% ;
8	SEL	Entry	RMS output pin configuration, with pulldown

2 Chip Feature Description

Recommended operating conditions

parameter	Symbol	Min	Typ	Max	Units
Positive supply	VDD	4.5	5.0	5.5	V
temperature range	T _A	-40	-	+85	°C

2.1 Analog Features

VDD = 5 V ± 10%; GND = 0 V;

parameter	Symbol	Min	Typ	Max	Units
Accuracy					
Active Power Full range input gain range 0.1% ~ 100% P _{Active}	P _{Active}	-	±0.2	-	%
RMS current Full range input gain range From 0.2% to 100%	I _{RMS}	-	±0.5	-	%
RMS voltage Full range input gain range 0.2% ~ 100% V _{RMS}	V _{RMS}	-	±0.5	-	%
Analog input (all channels)					
Common mode signal		-1	-	1	V
Analog Input					
Crosstalk voltage channel full scale (50, 60Hz)		-	-100	-	dB
Input capacitance	IC	-	6.4	-	pF
Equivalent input impedance: Current Channel	EII		500	-	kΩ
Voltage Channel			6	-	MΩ
Equivalent Input Noise	N _I	Current	-	-	2 μVrms
Channel Voltage Channel			-	-	20 μVrms
Power supply					
Current consumption IA + ID + (VDD = 5 V)			3	-	mA mA
Power (VDD = 5 V)	PC	-	15		mW
Brownout detector threshold a low pressure	PMLO	-	4	-	V
Brownout detector threshold a high pressure	PMHI	-	4.3	-	V

Built-in reference voltage

parameter	Symbol	Min	Typ	Max	Units
The reference voltage	VREF	+2.3	+2.43	+2.55	V
Drift	TC_{VREF}	-	25	-	ppm/°C

2.2 Digital features

VDD = 5 V , GND = 0 V

parameter	Symbol	Min	Typ	Max	Units
Master Clock					
Master clock frequency	MCLK	3.04	3.579	4.12	MHz
Master clock duty cycle		30	50	70	%
filter					
Input sample rate (DCLK = MCLK / K)		-	DCLK/4	-	Hz
Digital filter output rate	OWR	-	DCLK/128	-	Hz
A high-pass filter corner (- 3dB)frequency		-	0.543	-	Hz
input Output					
High-level input voltage VDD = 5V	V_{IH}	0.8VDD	-	-	V
Low level input voltage VDD = 5V,	V_{IL}	-	-	0.8	V
High-level output voltage Iout = +5 mA	V_{OH}	VDD-0.5	-	-	V
Low Output Voltage Iout = -5 mA	V_{OL}	-	-	0.5	V
Input leakage current	I_{in}	-	± 10	-	μA
Digital output pin capacitance	C_{OUT}	-	5	-	pF

2.3 Switching Characteristics

SEL Is an input port, CF , CF1 Output pulse duty cycle of 50% .

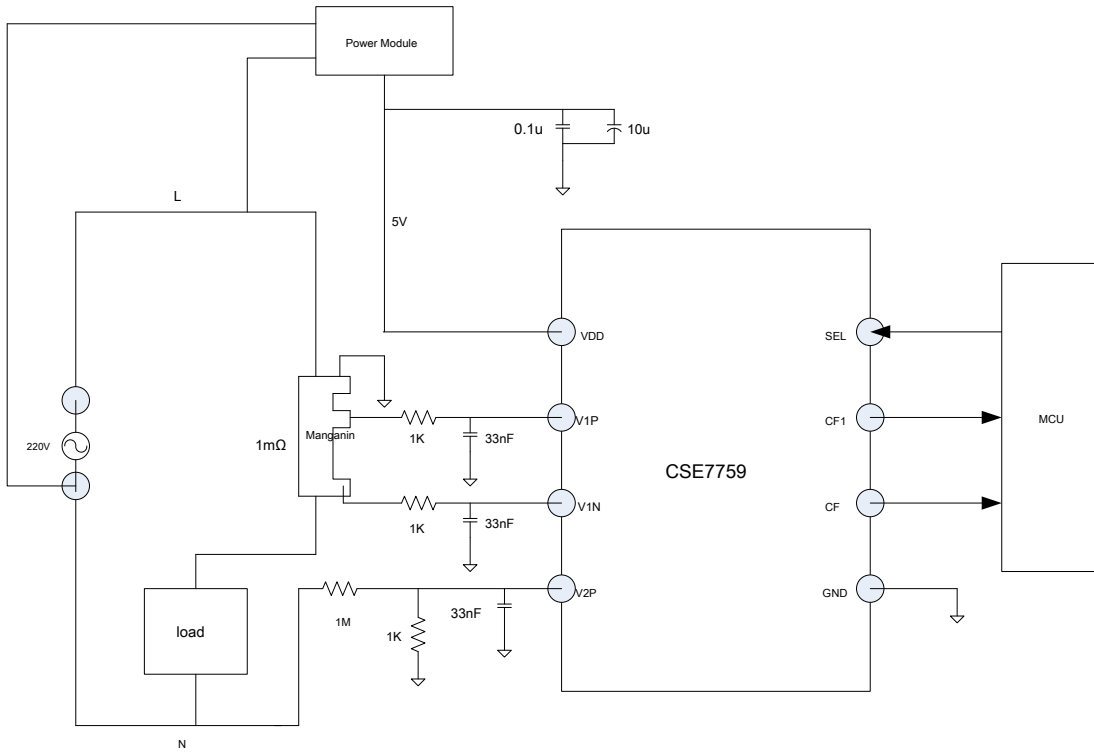
2.4 Limit Ratings

parameter	Symbol	Min	Typ	Max	Units
Digital Power	VDD	-0.3	-	+6.0	V
Analog supply	VDD	-0.3	-	+6.0	V
VDD to GND		-0.3	-	+6.0	V
V1P, V1N, V2P		-1		+1	V
Analog Input Voltage	V_{INA}	-0.3	-	VDD+0.3	V
Digital input voltage	V_{IND}	-0.3	-	VDD+0.3	V
Digital output voltage	V_{OUTD}	-0.3	-	VDD+0.3	V
Working temperature	T_A	-40	-	85	°C
storage temperature	T_{stg}	-65	-	150	°C

3 Chip applications

3.1 CSE7759 typical application

Figure 4 Shown in FIG. CSE7759 Supply terminal, two small capacitors to be connected in parallel to filter out high frequency and low frequency noise from the power grid. Manganin current signal through sampling resistor access CSE7759 , Through the voltage signal input to the resistor network CSE7759 . CF , SEL Direct access to the CPU An input terminal, by computing CF , CF1 Pulse period value to calculate the power, RMS voltage, and RMS current magnitude.



Map 3 : CSE7759 typical application

3.2 CF , CF1 Frequency of

CSE7759 internal DSP Having a certain gain after the frequency conversion module, active power, RMS voltage, and RMS current output frequency is calculated by the following equation:

$$F_{CF} = \frac{V1 \times V2 \times 48}{V_{REF}^2} \times \frac{f_{osc}}{128}$$

$$F_{CF1} = \frac{V1 \times 24}{V_{REF}} \times \frac{f_{osc}}{512}$$

$$F_{CFU} = \frac{V2 \times 2}{V_{REF}} \times \frac{f_{osc}}{512}$$

V1 : The voltage on the pin current path;

V2 : The voltage signal the voltage on the pin channel;

: Built-in oscillator, typically a frequency of about 3.579MHz ;

: Internal reference source voltage is typically 2.43V ; Note: Due CSE7759 Noise is present, in the absence of an input signal, indicative of the current, RMS voltage magnitude

CF1 Pin on there 2Hz Right and left output signal (this signal can CF Analyzing creep pulse frequency masked), in order to ensure correct measurement RMS magnitude, is applied in the channel V1P \ V1N RMS current not be less than 40uv , Applied to the channel V2P RMS voltage is not less than 480uv . In use, please contact our support technology.

3.3 Chip startup threshold creep prevention

CSE7759 The use of anti-creep new algorithm, as long as the power value of the input signal is greater than the noise level inside the metering module begins normal dosing.

3.4 Built-in oscillator

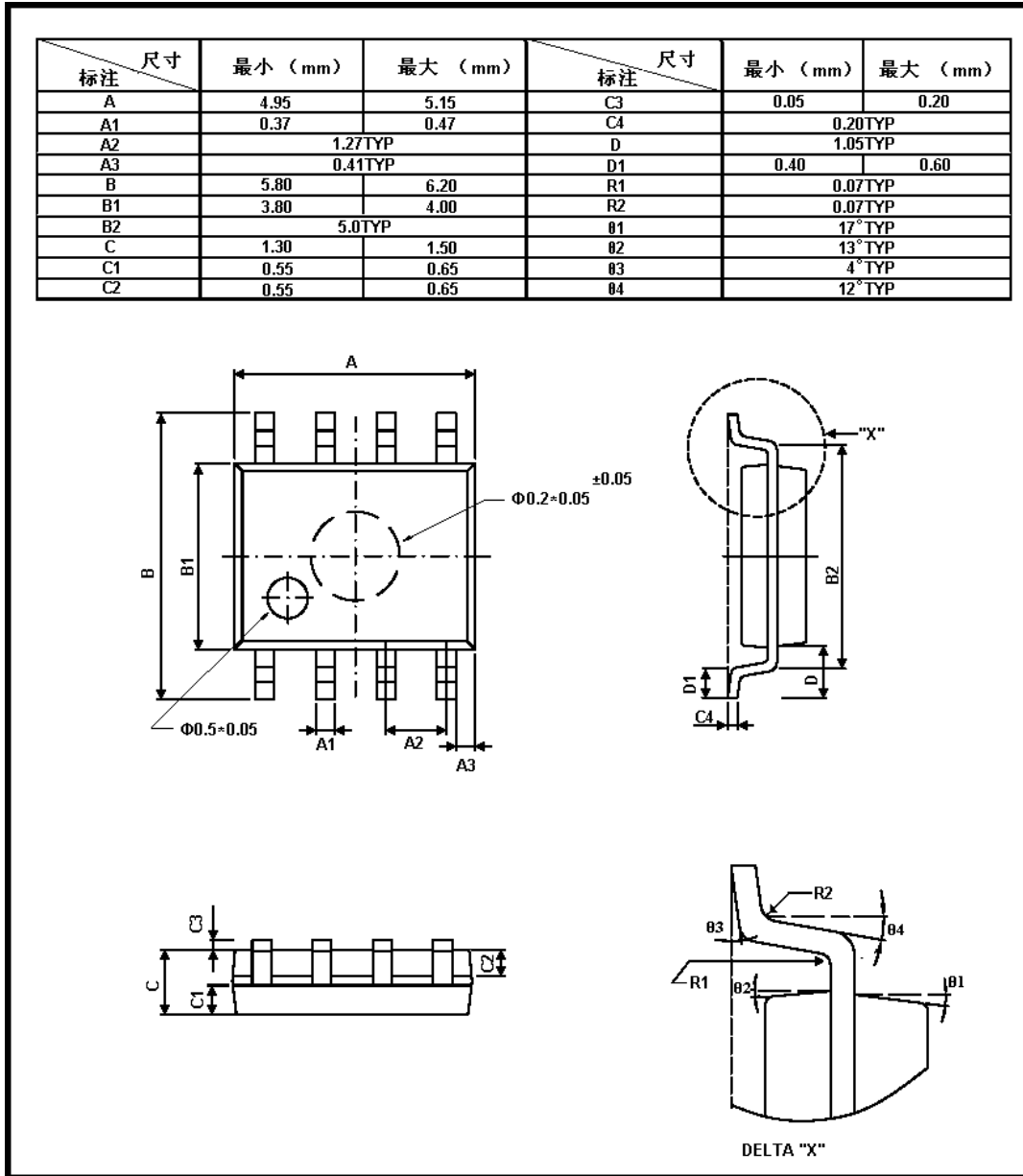
CSE7759 Frequency of the oscillator used in about 3.579M , PSRR is $< 0.01 / V$.

3.5 Built-in reference source

CSE7759 Typical built precision bandgap reference voltage source, the output of the reference source 2.43V .

4 CSE7759 Package

CSE7759 use SOP8 Package, package specific information as shown below:



Map 4 : CSE7759 FIG Package Information