ES8311 User Guide

(Rev 1.00)

OVERVIEW

The ES8311 is a low-power mono audio codec with fully differential output and headphone amplifier, as well as analog inputs that are programmable in fully differential configurations.

The record path of the ES8311 contains one fully differential input, analog digitally controlled mono microphone preamplifier, and automatic gain control (ALC). Programmable filters are available during record which can remove audible noise.

The playback path includes a mono DAC, through programmable volume controls, to the fully differential output. The fully differential output of ES8311 has a capability to drive 16Ω or 32Ω headphone load.

ES8311 is optimized for voice playback/record, so that it is very suitable for surveillance and voice application, such as car DV, IP CAMERNA, DVR, NVR, Baby monitor, intelligent toy, intelligent Robert, etc..

FEATURES

1. One I2S/PCM digital serial audio port with Master or Slave mode, it can support I2S, Left Justified and DSP-A/B formats.
2. 2C

ADC RECORD FUNCTIONS

3. 100dB SNR, -88dB THD+N
4. Differential analog input
5. Low noise PGA for analog line in or microphone in
6. Noise reduction filters
7. ALC with Noise gate
8. Supports analog and digital microphone interface

DAC PLAYBACK FUNCTIONS

9. 110dB SNR, -85dB THD+N
10. Dynamic Range Compression for analog output
11. Differential Line Out with 16 Ω/32 Ω headphone driver
12. Pop and click noise suppression
13. ADC data can be routed to DAC.
14. DAC data can be routed to Digital Serial Output Port

ES8311 User Guide

1 ES8311 BLOCK DIAGRAM

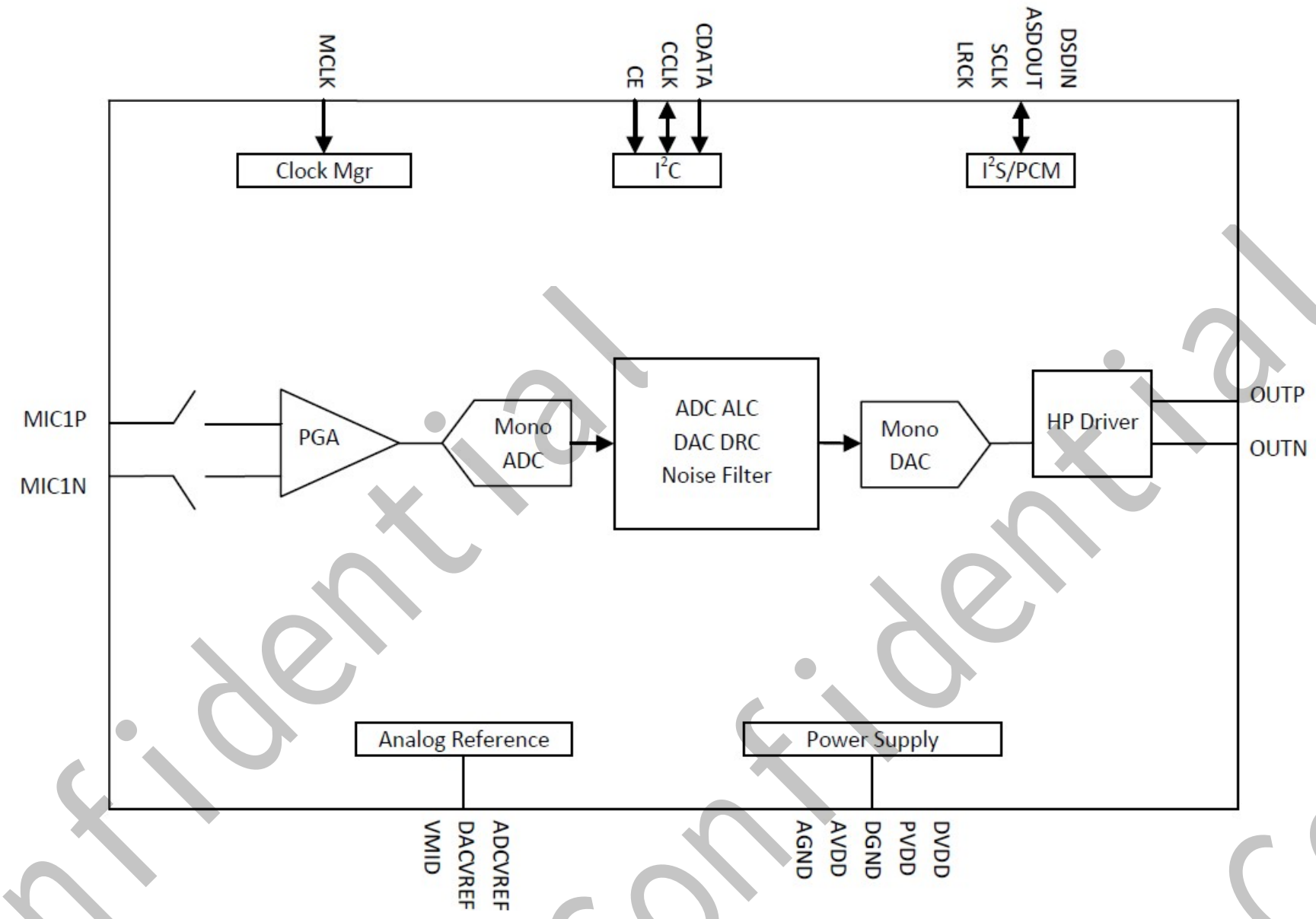

Figure 1. Block Diagram

ANALOG INPUT PATH

The analog input path of the ES8311 contains one fully differential analog input, analog mono microphone preamplifier with gain range from 0dB to +30dB. The analog differential input signal on MIC1P and MIC1N is boosted by the preamplifier.

The output signal of PGA enters into a high-quality mono ADC for analog-to-digital conversion.

DIGITAL OUTPUT SIGNAL PATH

ES8311 has a mono ADC which is a complete analog-to-digital converter for digital audio systems. It performs sampling, analog-to-digital conversion, anti-alias filtering and ALC (Automatically Level Control), generating 24-bit values for mono inputs. The digital signal is outputted at ASDOUT pin in serial form at sample rates up to 96 kHz.

The data bits of DAC also can be routed to digital serial output port. It is very helpful for echo cancellation application.

ANALOG OUTPUT SIGNAL PATH

The analog output path includes mono DAC, programmable volume control, a fully differential output and headphone amplifier. The mono audio DAC supports sampling rates from 8 kHz to 96 kHz and includes programmable digital filtering and Dynamic Range Compression in the DAC path.

The data of ADC also can be routed to DAC path. It is helpful for user test mode.

2 RECOMMENDED OPERATING CONDITION

PARAMETER	MIN	TYP	MAX	UNIT
Analog Supply Voltage Level AVDD	1.7	3.3	3.6	V
Digital Supply Voltage Level PVDD	1.6	3.3	3.6	V
Digital Supply Voltage Level DVDD	1.6	3.3	3.6	V

3 TYPICAL APPLICATION CIRCUIT FOR ELECTRET MICRPHONE INPUT

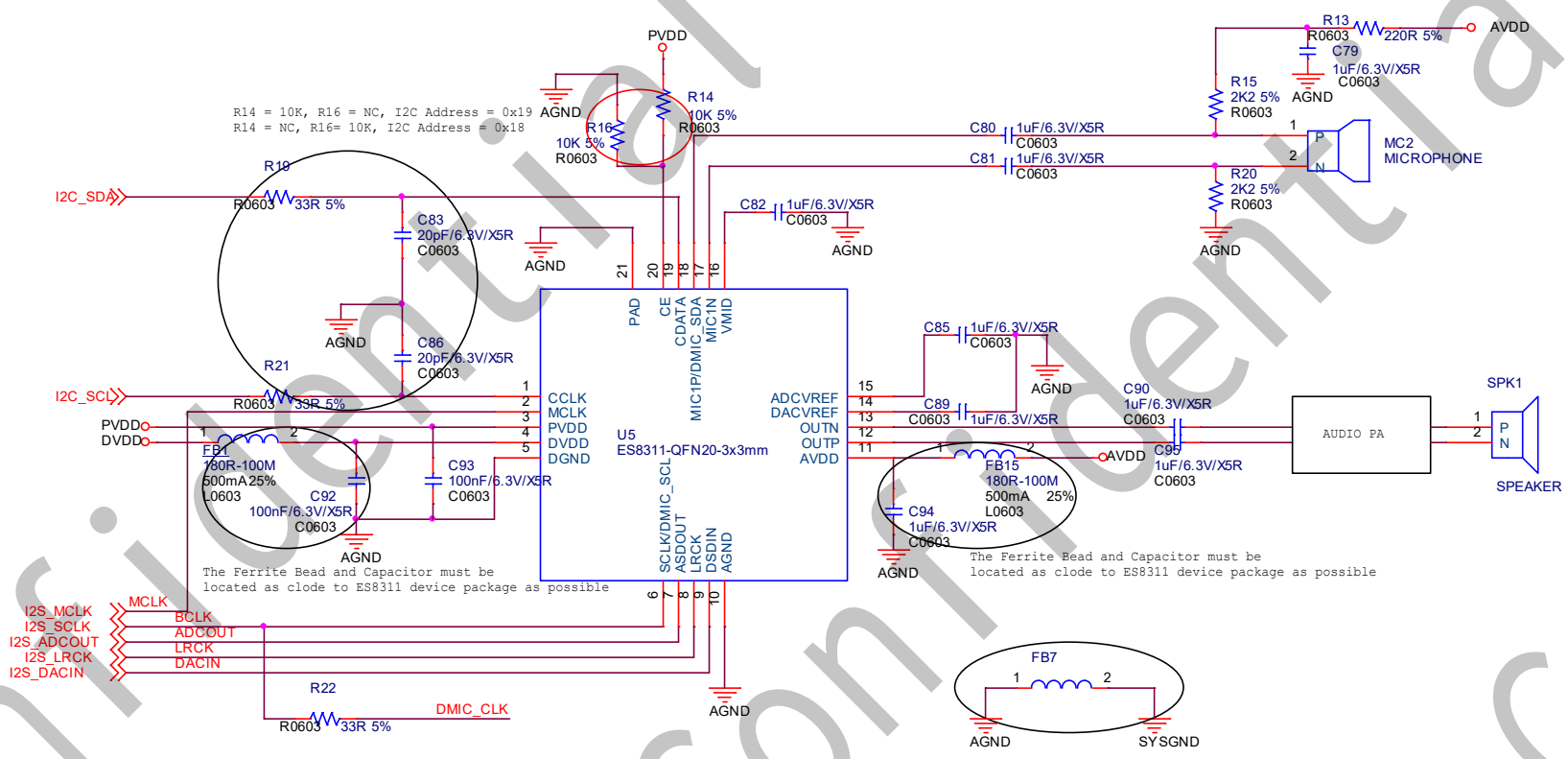

Figure 2. Application Circuit for ECM

4 TYPICAL APPLICATION CIRCUIT FOR DIGITAL MICROPHONE INPUT

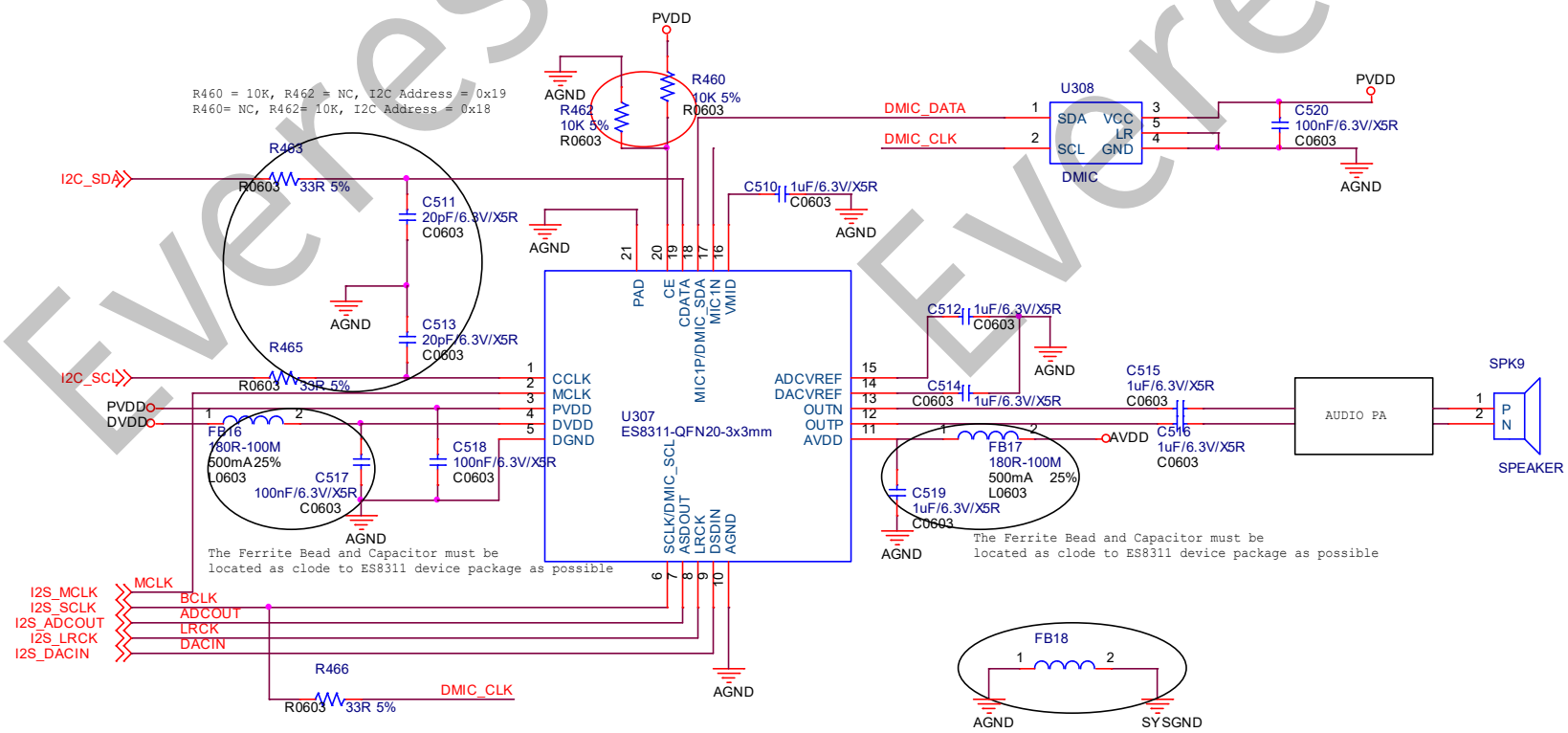

Figure 3. Application Circuit for DMIC

5 CIRCUIT AND PCB LAYOUT GUIDE

As with any high-resolution converter, designing with the ES8311 requires careful attention to PCB layout if its potential performance is to be realized.

5.1 POWER SUPPLY, GROUNDING AND DECOUPLING

Figure 4 shows the recommended power arrangements, with AVDD and DVDD connected to a clean supply. A ferrite bead on DVDD and AVDD is used to minimize EMI especially in the case where FM radio is an option. Decoupling capacitors and ferrite bead should be located as close to the ES8311 as possible, with the low value ceramic capacitor being the nearest.

All signals, especially clocks, should be kept away from the ADCVRE, DACVREF, and VMID pins in order to avoid unwanted coupling into the modulators. The ADCVRE, DACVREF and VMID decoupling capacitors, particularly the 0.1µF, must be positioned to minimize the electrical path from these reference pins to GND.

The following shows recommending value for the decoupling and filter capacitors

Pins	At Minimum	Recommended
AVDD, DVDD, PVDD	0.1uF, Ceramic Capacitor	0.1uF, Ceramic Capacitor.
DACVREF, ADCVREF, VMID	0.47uF, Ceramic Capacitor	1uF, Ceramic Capacitor

The ground pins of ES8311, AGND and DGND, must be connected to audio ground plane. The audio ground is connected to system ground in single-point grounding topology.

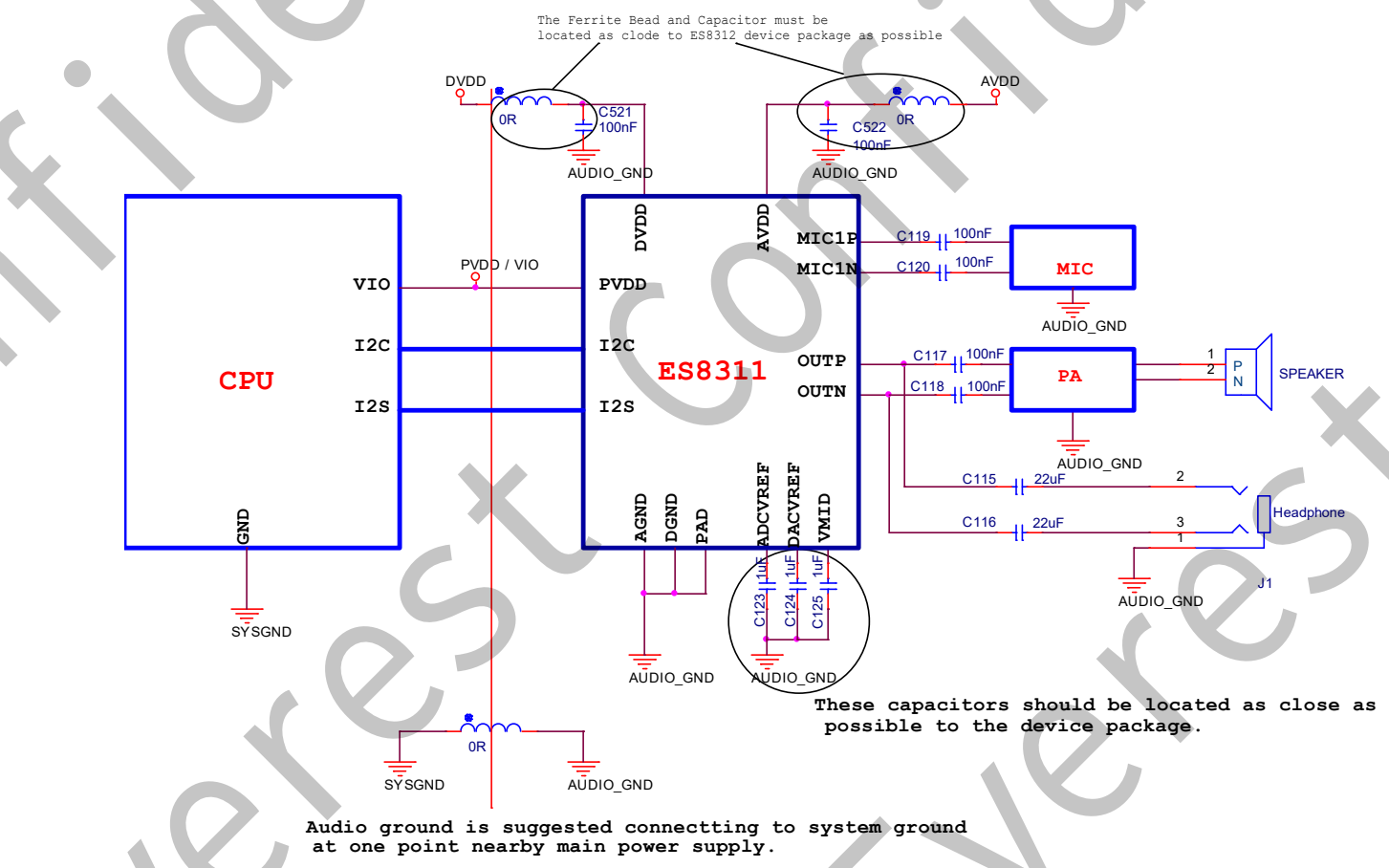

Figure 4. Power Supply and Ground Arrangement

The following picture shows an example for AVDD and DVDD decoupling capacitors and ferrite bead placement.

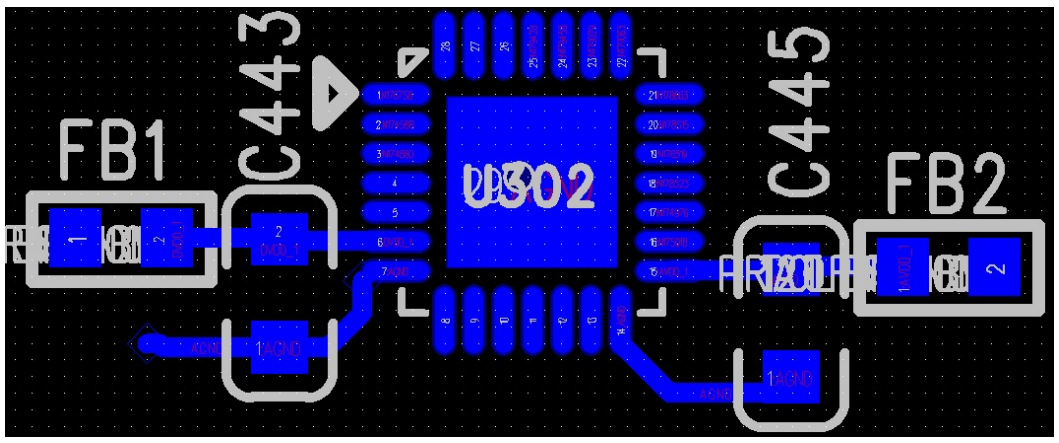

Figure 5. The AVDD and DVDD decoupling capacitors and ferrite bead placement

There is a thermal pad at the bottom of ES8311 package. This thermal pad must be connected to audio ground.

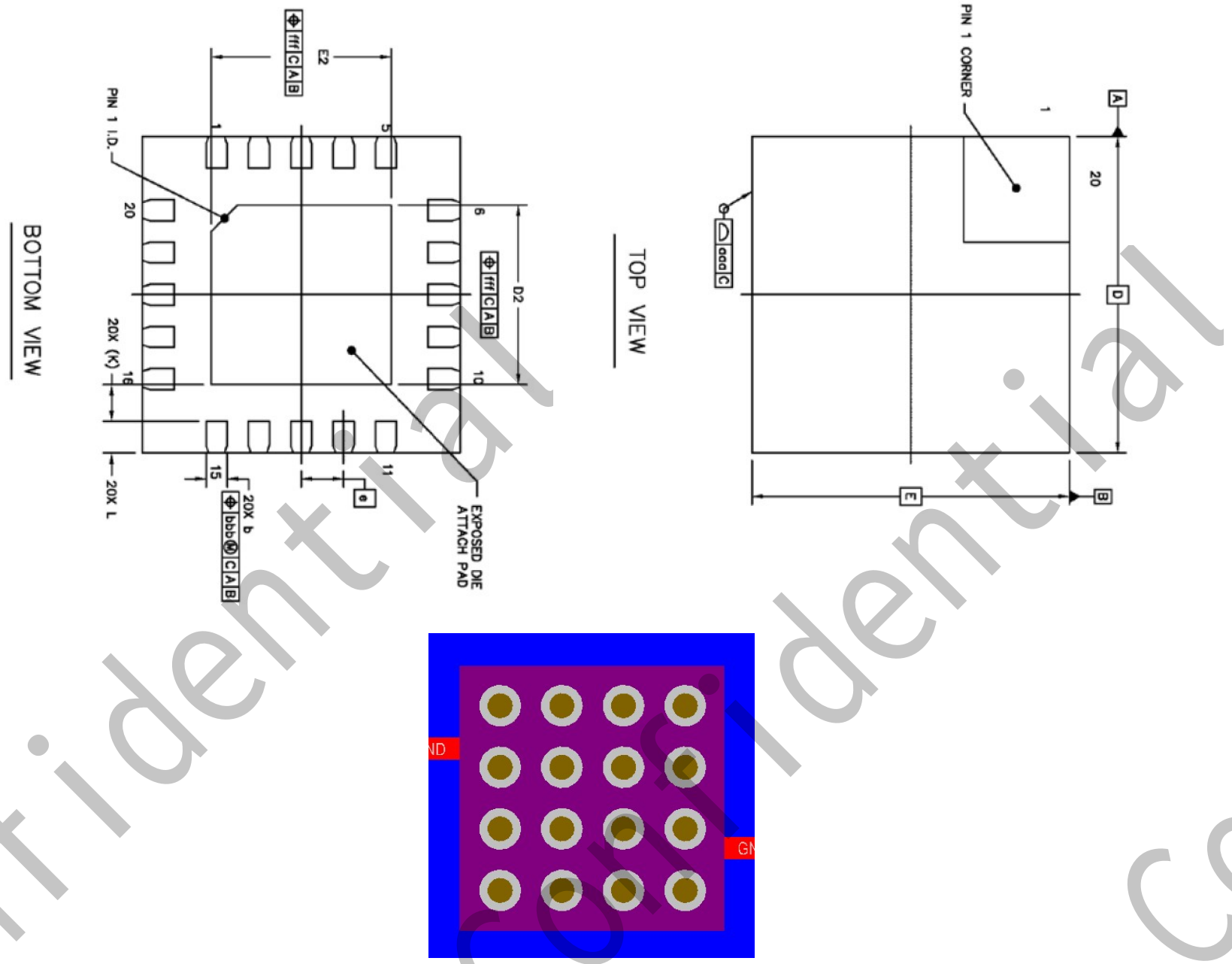

Figure 6. Thermal PAD

5.2 THE CIRCUIT SCHEMATIC FOR I2C

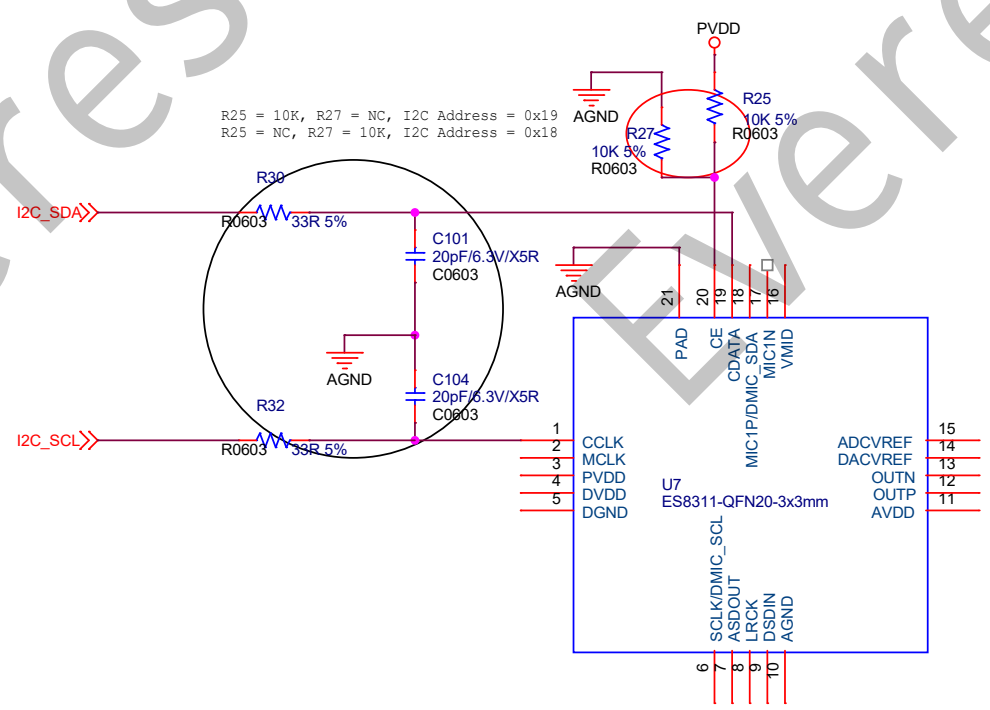

Figure 7. I2C Circuit

R-C low pass filter is strongly suggested to be used onto I2C DAT and I2C CLK. The I2C route must be shielded by ground.

5.3 THE CIRCUIT SCHEMATIC FOR I2S

If the length of I2S clock is larger than 10cm, please use 30pF capacitors between I2S clock route and ground. For example,

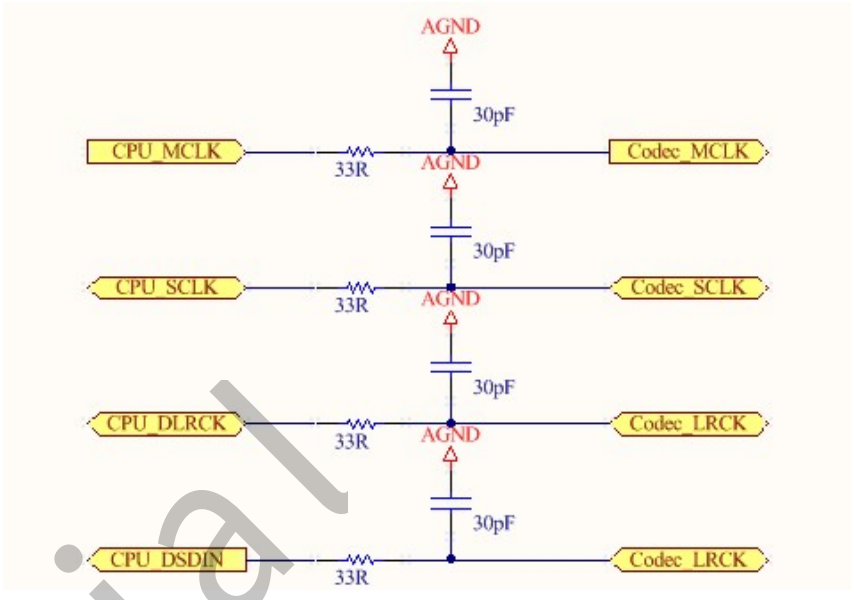

Figure 8. I2S Circuit

5.4 THE CIRCUIT SCHEMATIC FOR OUTPUT

Below application circuit shows how to connect OUTP/N of ES8311 to the differential input of audio power amplifier.

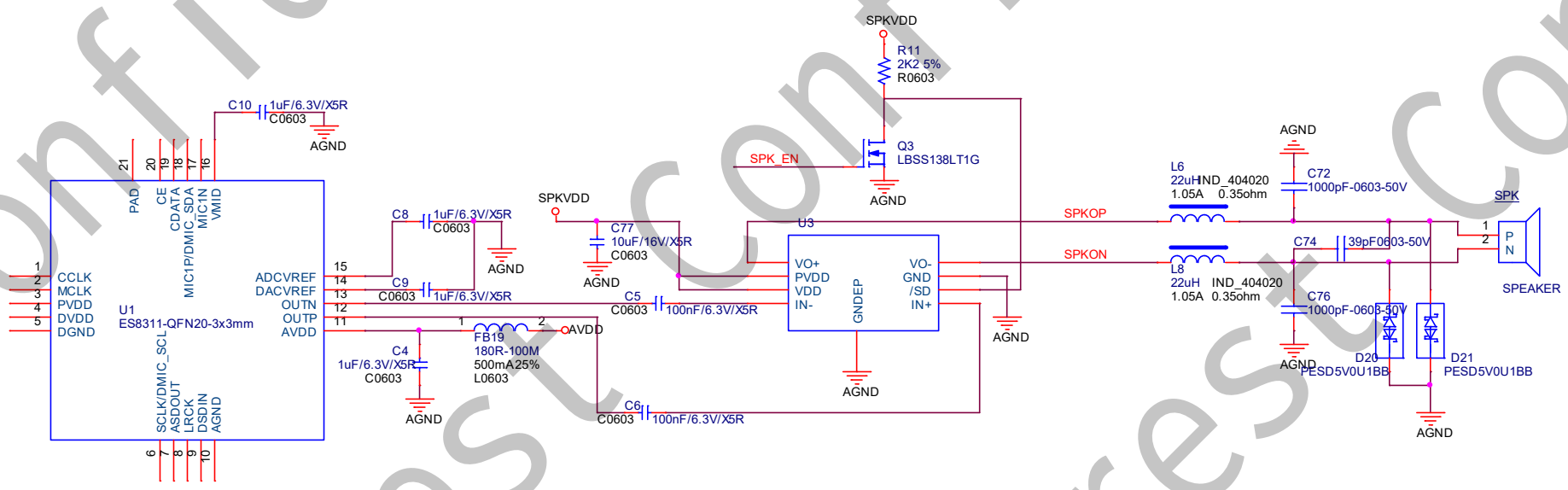

Figure 9. differential out and speaker out Circuit

5.5 THE CIRCUIT SCHEMATIC FOR ELECTRETS MICROPHONE INPUT

In this example, the microphone has been configured as fully differential output. ES8311 doesn't have bias voltage for microphone, so the power supply on AVDD pin of ES8311 can be used as microphone bias supply. It is suggested that one R-C low pass filter, with 220 Ω resister and 1uF capacitor, should be used in the path of microphone bias supply. This low pass filter can attenuate the high frequency noise of microphone bias, and will be helpful for improving of recording performance.

The microphone signal is sensitive to noise so that a differential route with ground shielding is suggested for the path of MIC1P&MIC1N. Here, C80, C81, C70, R15, R20 and R13 is suggested to located close to electrets microphone.

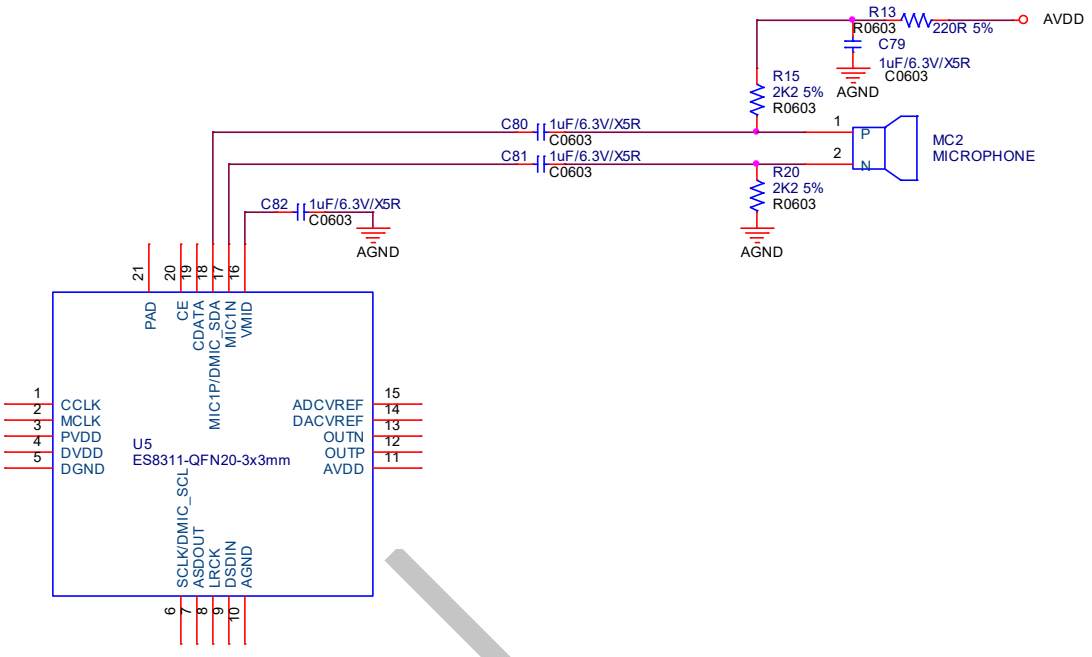

Figure 10. electrets microphone Circuit

5.6 THE CIRCUIT SCHEMATIC FOR DIGITAL MICROPHONE INPUT

ES8311 has a PDM digital microphone interface which can be used to connect only one PDM microphone. In ES8311, there is an internal register for selecting the data from left or right digital microphone. The L/R pin of digital microphone can be high or low level according to the internal register selecting for left or right PDM microphone.

ES8311 doesn't have clock signal for PDM digital microphone, so the BCLK signal is used for clock of PDM microphone. Also, ES8311 doesn't provide Bias voltage for PDM microphone, please use the power supply on PVDD of ES8311 as digital microphone power supply. MIC1P of ES8311 is multiplex pin for analog input and PDM digital microphone input.

ES8311 provides PDM interface, volume control and filters, and outputs the recording data on ASDOUT pin in I2S, Left Justified or DSP format according to the internal register setting of digital serial port format.

Below application circuit shows how to connect PDM microphone to ES8311.

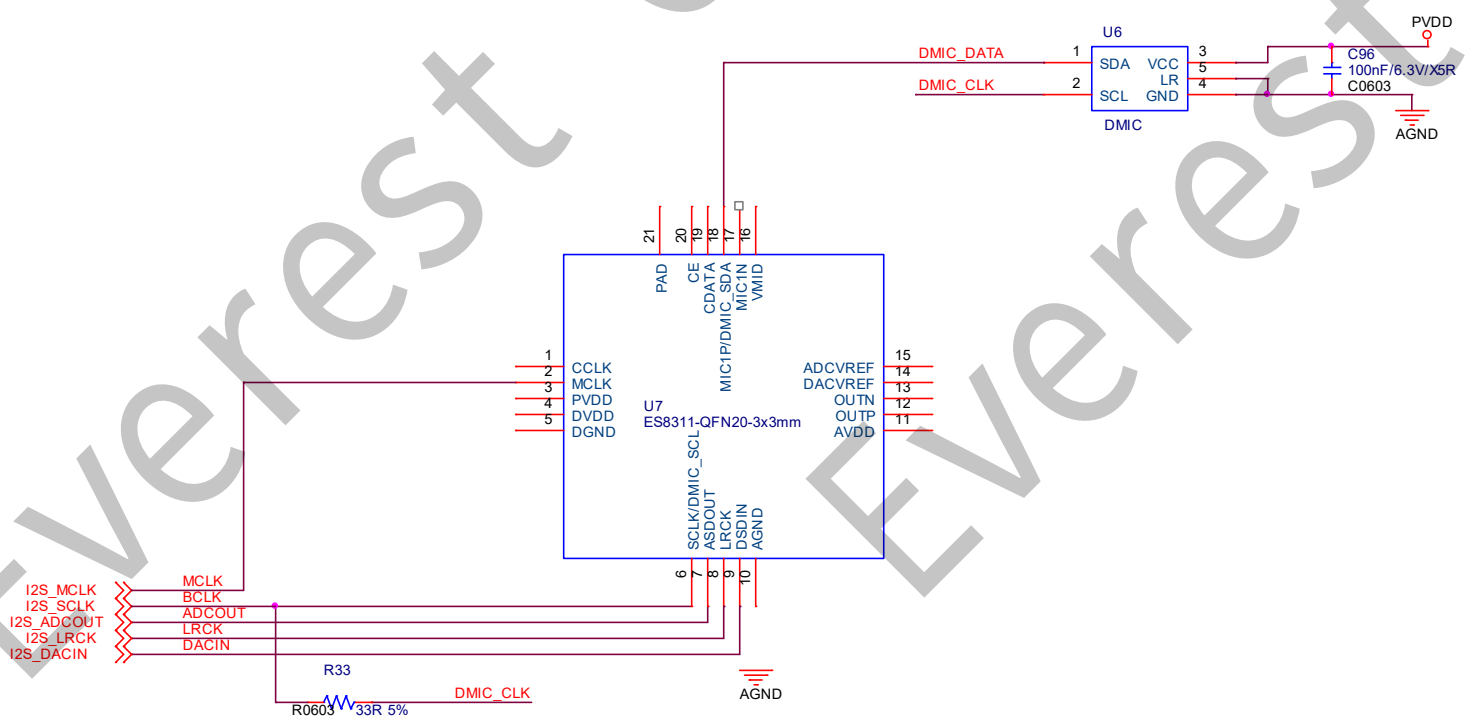

Figure 11. digital microphone circuit

6 I2C INTERFACE

ES8311 supports I2C interface to write or read internal register. The CE pin of ES8311 is the chip address pin for I2C. Two pull up resisters, with the range from 1KΩ to 4.7KΩ, is used for pull-up resister on I2C CCLK and I2C CDATA pin.

The transfer rate of I2C interface is lower than 400kbps.

The I2C chip address is decided by the level on CE pin, the following table shows the chip address definition.

ES8311 CE PIN	I2C Chip Address(Bin/Hex)
Pulled down to ground with 10kΩ resister	001 1000 / 0x18(7 bits address)
Pulled up to PVDD with 10kΩ resister	001 1001 / 0x19 (7 bits address)

The following drawing illustrates I2C timing

	Chip Address	R/W		Register Address		Data to be written		
start	0011 00 CE	0	ACK	RAM	ACK	DATA	ACK	Stop

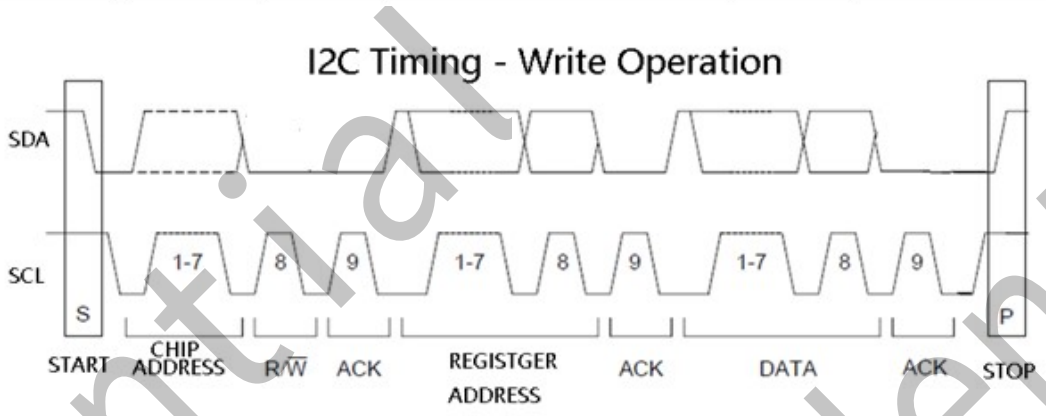

Figure 12. I2C Write timing

	Chip Address		R/W		Register Address	
start	0011 00	CE	0	ACK	RAM	ACK
	Chip Address		R/W		Data to be read	
start	0011 00	CE	1	ACK	DATA	NAK Stop

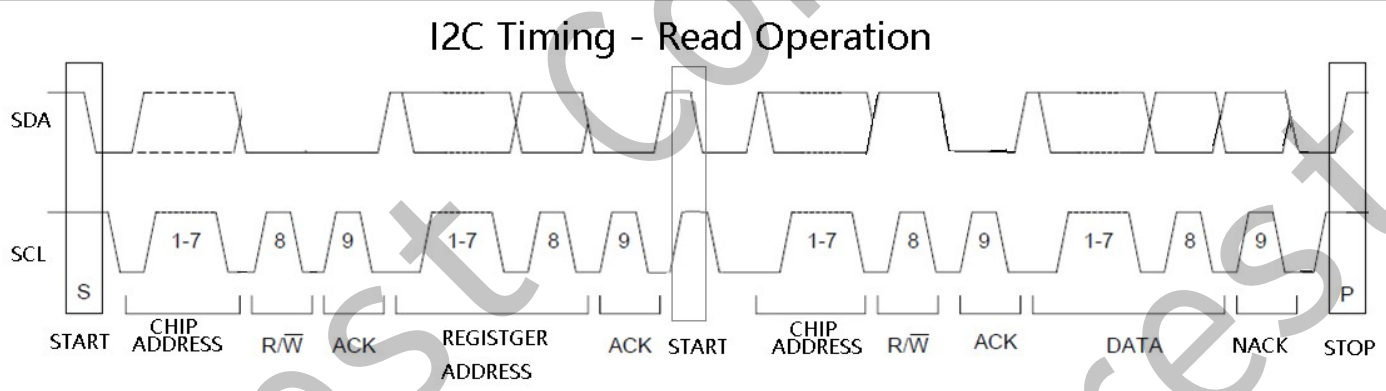

Figure 13. I2C Read timing

7 DIGITAL AUDIO INTERFACE

ES8311 provides four formats of serial digital audio interface to the input of DAC or output from ADC through LRCK, SCLK, ADCDAT and DACDAT pins.

- ADCDAT : ADC data output
- DACDAT : DAC data input
- LRCK : Left/Right data alignment clock
- SCLK : Bit clock, for synchronisation

ES8311 supports four audio data formats:

- I2S
- Left Justified

- DSP mode A
- DSP mode B

The below diagram shows the timing of I2S, Left Justified, DSP-A and DSP-B mode. All of these four formats are MSB first.

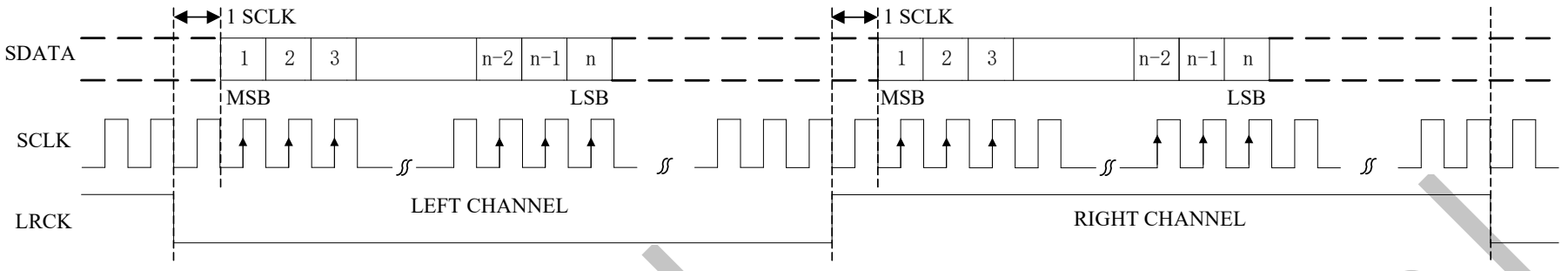

Figure 14. I²S Serial Audio Data Format Up To 24-bit

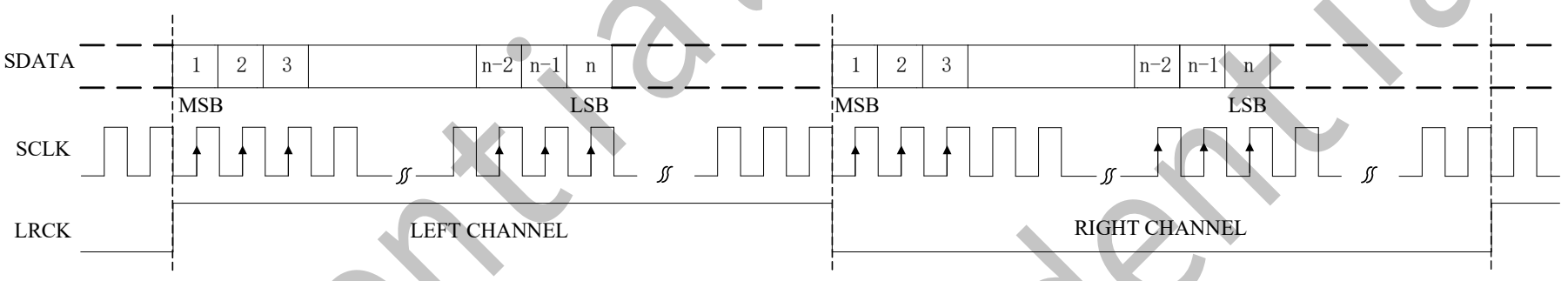

Figure 15. Left Justified Serial Audio Data Format Up To 24-bit

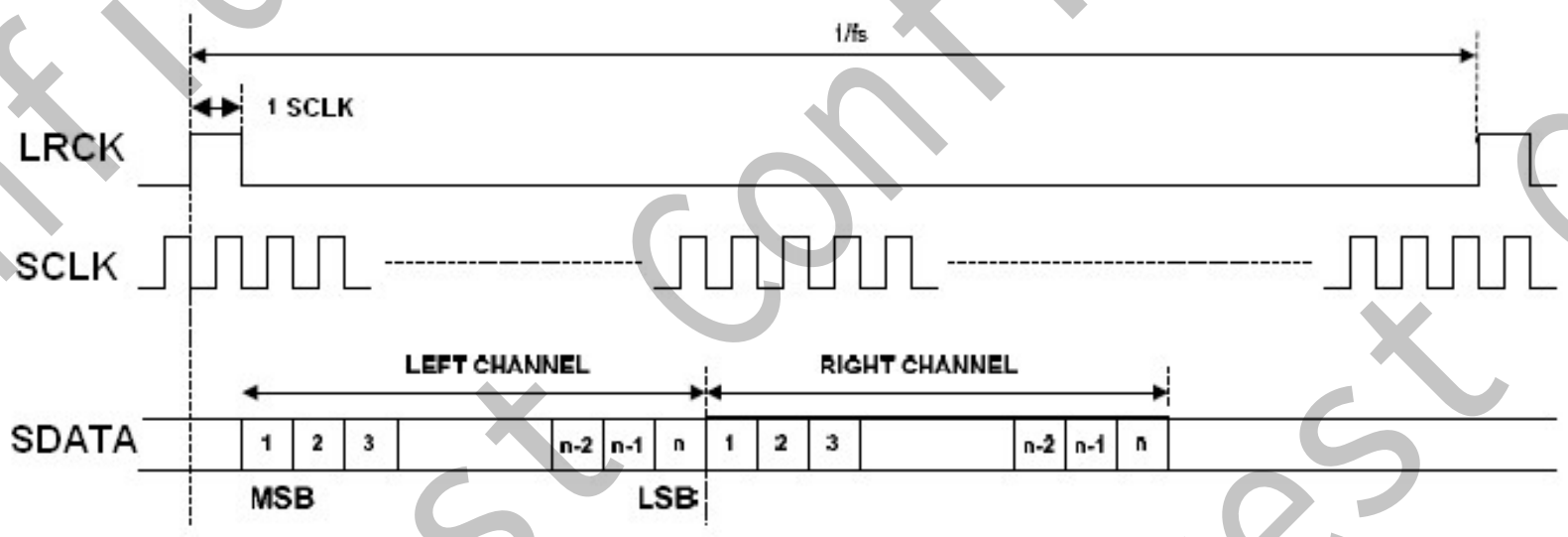

Figure 16. DSP/PCM Mode A

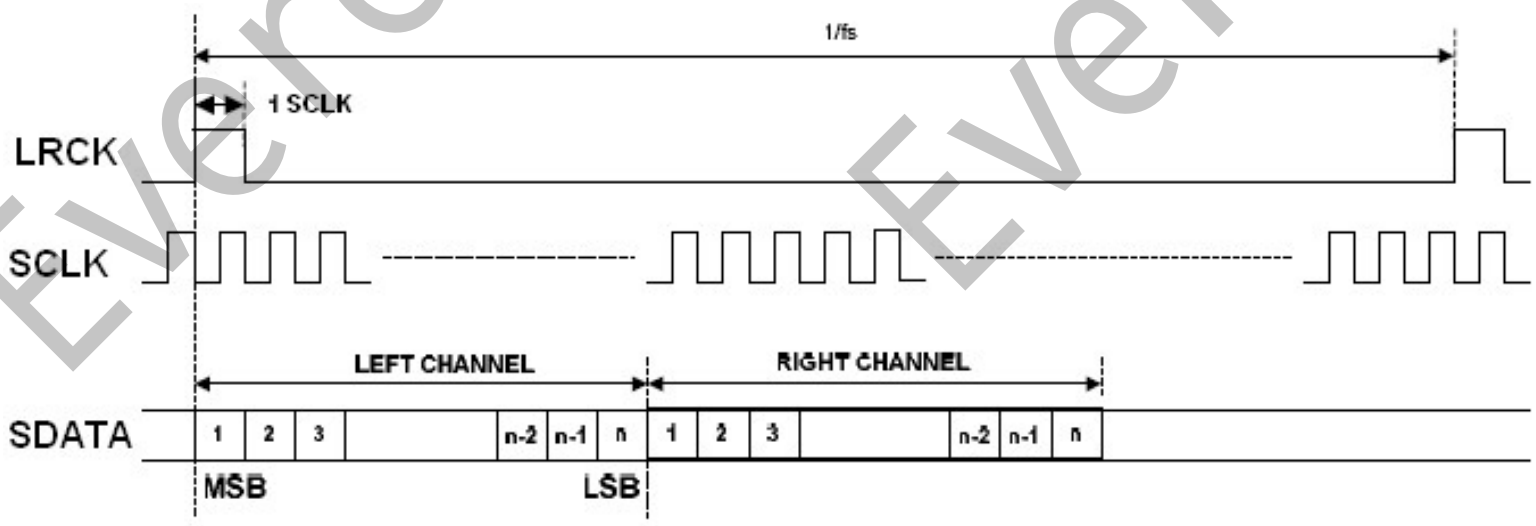

Figure 17. DSP/PCM Mode B

Register 0x09 and register 0x0A are used to select DAC and ADC formats. The following is the definition of register 0x09 and register 0x0A.

- register 0x09 : SDP, Default 0000 0000

Bit Name	Bit	Description

SDP_IN_SEL	7	SDP in data select 0 – Left channel data to DAC(default) 1 – right channel data to DAC
SDP_IN_MUTE	6	SDP in mute 0 – unmute (default) 1 – mute
SDP_IN_LRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity(default) 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after LRCK rising edge(default) 1 – MSB is available on 1st BCLK rising edge after LRCK rising edge
SDP_IN_WL	4:2	000 – 24-bit serial audio data word length(default) 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
SDP_IN_FMT	1:0	00 – I2S serial audio data format(default) 01 – left justify serial audio data format 10 – reserve 11 – DSP/PCM mode serial audio data format

- register 0x0A : SDP, Default 0000 0000

Bit Name	Bit	Description
SDP_OUT_MUTE	6	SDP out mute 0 – unmute (default) 1 – mute
SDP_ OUT_LRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity(default) 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after LRCK rising edge(default) 1 – MSB is available on 1st BCLK rising edge after LRCK rising edge
SDP_OUT_WL	4:2	000 – 24-bit serial audio data word length(default) 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
SDP_OUT_FMT	1:0	00 – I2S serial audio data format(default) 01 – left justify serial audio data format 10 – reserve 11 – DSP/PCM mode serial audio data format

8 MASTER/SLAVE MODE AND INTERNAL CLOCK DIAGRAM

ES8311 can work in either master or slave mode. In master mode, LRCK and SCLK are output pins and they are derived internally from internal master clock (IMCLK). In slave mode, LRCK and SCLK are input pins and they are supplied externally. MCLK is always input pin in either master or slave mode.

8.1 INTERNAL CLOCK DIAGRAM

Below diagram illustrates the internal clock management.

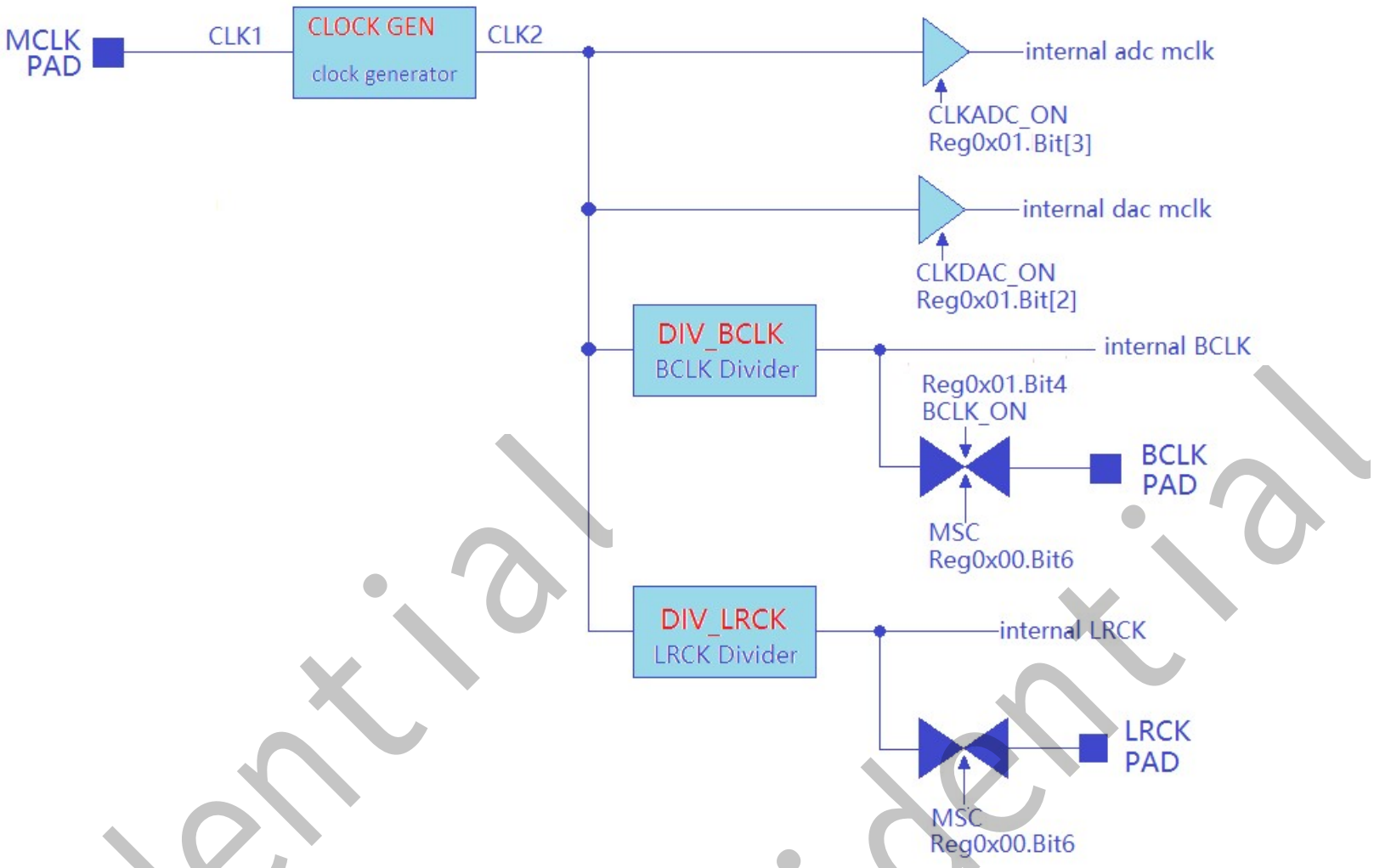

Figure 18. Clock Diagram

8.2 MASTER OR SLAVE MODE

The Bit6(MSC) of register 0x00 selects Master or Slave mode. MSC bit = "1" selects master mode, and "0" selects slave mode. By default, ES8311 will be in slave mode after power up reset.

The Bit[5:4](TRI) of register 0x07 is used to set BCLK, LRCK, ADCDAT to tri-state mode.

- Register 0x00 – Reset, Default 0001 1111

Bit Name	Bit	Description
CSM_ON	7	Chip current state machine control 0 – csm power down(default) 1 – csm power on
MSC	6	0 – slave serial port mode(default) 1 – master serial port mode

- Register 0x07 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
TRI_BLRCK	5	BCLK/LRCK tri-state control 0 – normal (default) 1 – BCLK and LRCK tri-state output
TRI_ADCDAT	4	ADCDAT tri-state control 0 – normal (default) 1 – ADCDAT tri-state output

Below diagram shows the direction of LRCK, SCLK and MCLK in master and slave mode.

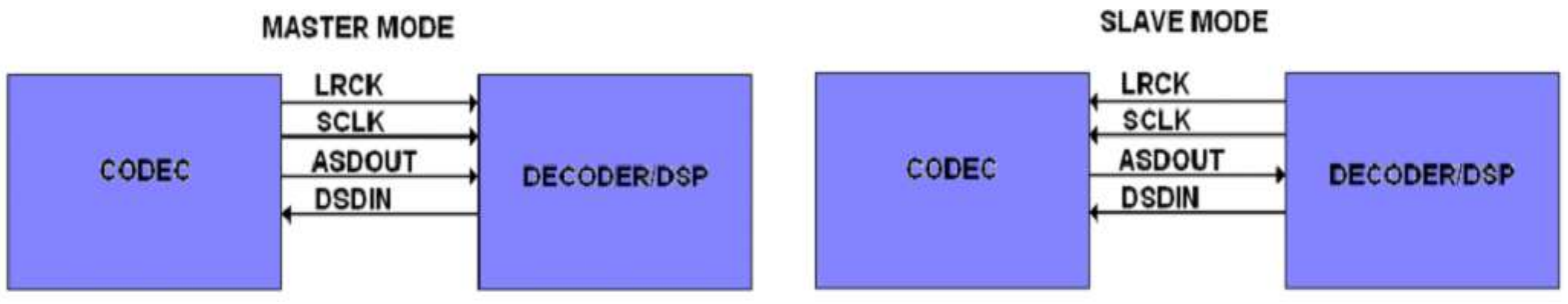

Figure 19. Master / Slave Mode

8.3 THE CLOCK SOURCE OF MASTER CLOCK (MCLK)

The clock signal on MCLK pin or SCLK pin can be used as master clock of ES8311. An internal multiplexer controlled by MCLK_SEL (Reg0x00.Bit[7]) is used for the clock source selection of internal master clock. MCLK_SEL bit = '1' selects clock on SCLK pin for internal master clock, and '0' selects clock on MCLK pin for internal master clock.

MCLK_ON(Reg0x01.Bit[5]) is ON/OFF switch for the clock on MCLK pin. If it is set to '1', the switch is on and the clock on MCLK pin can be used as source of internal multiplexer. If it is set '0', the switch is off, and the MCLK clock can't be used. The state of MCLK_ON has nothing to do with the clock of SCLK pin.

An internal logic inverter controlled by MCLK_INV(Reg0x01.Bit[6]) is used for inversion of clock. If the clock on SCLK pin is used as the source of internal master clock, MCLK_INV = '1' can only invert the master clock, not invert SCLK.

- Register 0x01 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
MCLK_SEL	7	Mclkin select 0 – from MCLK(default) 1 – from BCLK
MCLK_INV	6	Mclkin invert control 0 – normal MCLK(default) 1 – MCLK invert
MCLK_ON	5	MCLK in control 0 – MCLK off(default) 1 – MCLK on

8.4 INTERNAL MASTER CLOCK

A clock divider and a clock multiplier are used to generate internal master clock from the output of multiplexer. The clock divider controlled by DIV_PRE (Reg0x02.Bit[7:5]) provides divider ratio from 1 to 8. The clock multiplier controlled by MULTI_PRE (Reg0x02.Bit[4:3]) provides ratio 1, 2, 4 and 8.

There is a restriction about the output frequency of clock divider. If DVDD is 1.8V, the output frequency of clock divider must be lower than 4.5MHZ. If DVDD is 3.3V, the output frequency of clock divider must be lower than 10MHZ.

The clock signal output from multiplier is referred as internal master clock.

- Register 0x02 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DIV_PRE	7:5	Pre-divide mclk control Mclk_prediv=mclk/(DIV_PRE+1)
MULT_PRE	4:3	Pre-multiply mclk_prediv 0 – dig_mclk=mclk_prediv*1 (default) 1 – dig_mclk=mclk_prediv*2 2 – dig_mclk=mclk_prediv*4 3 – dig_mclk=mclk_prediv*8

8.5 INTERNAL ADC CLOCK AND INTERNAL DAC CLOCK

There are two independent clock dividers to get internal clock for ADC and DAC. The DIV_CLKADC clock divider controlled by BIT[7:4] of register 0x05 is the ADC divider. The clock from ADC clock divider is referred as internal ADC clock. The DIV_CLKDAC clock divider controlled by BIT[3:0] of register 0x05 is the DAC divider. The clock from DAC clock divider is

referred as internal DAC clock.

The following is the equation of internal ADC/DAC clock.

$$\text{Internal ADC clock} = \text{internal master clock} \div [\text{DIV\_CLKADC} + 1]$$

$$\text{Internal DAC clock} = \text{internal master clock} \div [\text{DIV\_CLKDAC} + 1]$$

The frequency of internal ADC clock and internal DAC clock shouldn't be higher than 13MHZ if DVDD is 1.8V, and the frequency shouldn't be higher than 35MHZ if DVDD is 3.3V.

In normal mode, the ADC can work single speed mode or double speed mode. In single speed mode, the ratio between internal ADC clock and LRCK must be equal or greater than 256 (EQ enabled) or 240 (EQ disabled), and this ratio must be integral multiple of sixteen. In double speed, the ratio must be equal or greater than 128, and this ratio must be integral multiple of eight.

The DAC only works in single speed mode. the ratio between internal DAC clock and LRCK must be equal or greater than 256, and this ratio must be integral multiple of sixteen.

There also have two control bits in register 0x01 to switch on / off the internal ADC or DAC clock. CLKADC_ON (Reg0x01.Bit[3]) is the on/off control bit for internal ADC clock. CLKDAC_ON (Reg0x01.Bit[2]) is the on/off control bit for internal DAC clock. If the on / off control bit set to 1, the ADC or DAC clock is on, otherwise the ADC or DAC clock is off.

The following table shows the clock ratio for ADC and DAC.

Speed mode	The ratio between internal ADC/DAC clock and LRCK
ADC in single speed mode	240/256/272/288/384/512/768/1024/1536…….
ADC in double speed mode	128/136/144/192/256/272/288/384/512/768/1024/1536…….
DAC in single speed mode	256/272/288/384/512/768/1024/1536…….

The following examples show how to set the configuration registers to get a proper clock ratio.

- Example 1. MCLK = 12.288MHZ, LRCK = 48KHZ, here MCLK is the clock signal on MCLK pad, and LRCK is the clock signal on LRCK pad.
  1. Get MCLK / LRCK ratio, 12288000÷48000 = 256
  2. Set DIV_PRE to 0, and set MULT_PRE to 1, so that the internal master clock is equal to 12288000Hz, where 12288000Hz = MCLK ÷1×1.
  3. Set DIV_CLKADC to 0. Set DIV_CLKDAC to 0, too. Now the internal ADC clock and internal DAC clock are all equal to 12288000Hz, and the clock ratio is 256.
- Example 2. MCLK = 12.288MHZ, LRCK = 8KHZ, here MCLK is the clock signal on MCLK pad, and LRCK is the clock signal on LRCK pad.
  1. Get MCLK / LRCK ratio, 12288000÷8000 = 1536
  2. Set DIV_PRE to 5, and set MULT_PRE to 1 so that the internal master clock is equal to 2048000Hz, where 2048000Hz = MCLK ÷6×1.
  3. Set DIV_CLKADC to 0. Set DIV_CLKDAC to 0, too. Now the internal ADC clock and internal DAC clock are all equal to 2048000Hz, and the clock ratio is 256.
- Example 3. MCLK = 18.432MHZ, LRCK = 16KHZ, here MCLK is the clock signal on MCLK pad, and LRCK is the clock signal on LRCK pad.
  1. Get MCLK / LRCK ratio, 18432000÷16000 = 1152
  2. Set DIV_PRE to 2, and set MULT_PRE to 0, so that the internal master clock is equal to 2048000Hz, where 6144000 = MCLK ÷3×1.

3. Set DIV_CLKADC to 0. Set DIV_CLKDAC to 0, too. Now the internal ADC clock and internal DAC clock are all equal to 6144000, and the clock ratio is 384.

Below Table shows the register configurations about some frequently-used clock condition.

MCLK(MHz)	LRCK(kHz)	Reg 0x02(hex)	Reg 0x05(hex)	Reg 0x16(hex)	Reg 0x03(hex)	Reg 0x04(hex)
24.576	32	0x40	0x00	0x04	0x10	0x10
24.576	48	0x20	0x00	0x04	0x10	0x10
12.288	32	0x48	0x00	0x04	0x10	0x10
12.288	48	0x00	0x00	0x04	0x10	0x10
18.432	32	0x20	0x00	0x03	0x12	0x12
18.432	48	0x48	0x00	0x04	0x10	0x10
11.2896	44.1	0x00	0x00	0x04	0x10	0x10
12	32	0x00	0x00	0x02	0x17	0x17
12	44.1	0x00	0x00	0x03	0x11	0x11
12	48	0x98	0x00	0x01	0x19	0x19
26	32	0x40	0x00	0x04	0x10	0x10
12	32	0x58	0x43	0x01	0x59	0x0F
12	44.1	0x00	0x10	0x03	0x51	0x11
12	48	0x98	0x10	0x01	0x59	0x19
3	32	0x18	0x41	0x23	0x52	0x17
25	32	0x48	0x21	0x22	0x55	0x10
25	48	0x28	0x21	0x22	0x55	0x10

8.6 BIT CLOCK

The clock signal on SCLK pin is bit clock of ES8311. SCLK pin is a bi-direction pin. It is input pin while MSC(Reg0x00.Bit[6]) is set to 0, and it is output pin while MSC(Reg0x00.Bit[6]) is set to 1.

BCLK_ON controlled by Reg0x01.Bit[4] is the on/off control bit for bit clock. If BCLK_ON is set to '1', the bit clock is on.

If MSC is set to 1, ES8311 will work in master mode and SCLK pin will be an output pin. BCLK divider controlled by DIV_BCLK(Reg0x06.Bit[4:0]), with divider ratio from 1 to 72, is used to generate SCLK clock signal in master mode. In master mode, codec can decide to output bit clock continuously or transmit bit clock only when data transmission, according to the setting of BCLK_CON (Reg0x06.Bit[6]). BCLK divider and BCLK_CON all are inactive in slave mode.

One internal logic invertor controlled by BCLK_INV(Reg0x06.Bit[5]) is used for bit clock inversion.

- Register 0x01 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
BCLK_ON	4	SDP bit clock control 0 – BCLK off(default) 1 – BCLK on

- Register 0x06 – CLOCK MANAGER, DEFAULT 0000 0011

Bit Name	Bit	Description
BCLK_CON	6	BCLK out control when master mode 0 – normal continual BCLK out(default) 1 – stop BCLK out when data transfer finished
BCLK_INV	5	BCLK invert 0 – normal (default) 1 – BCLK invert
DIV_BCLK	4:0	BCLK divider at master mode 0~19 – dig_mclk/(DIV_BCLK+1) (default 3) 20 –dig_mclk /22 21 –dig_mclk /24 22 –dig_mclk /25 23 –dig_mclk /30 24 –dig_mclk /32

		25 –dig_mclk /33 26 –dig_mclk /34 27 –dig_mclk /36 28 –dig_mclk /44 29 –dig_mclk /48 30 –dig_mclk /66 31 –dig_mclk /72

8.7 FRAME CLOCK

The clock signal on LRCK pin is frame clock of ES8311. LRCK pin is a bi-direction pin. It is input pin while MSC(Reg0x00.Bit[6]) is set to 0, and it is output pin while MSC(Reg0x00.Bit[6]) is set to 1.

If MSC is set to 1, ES8311 will work in master mode and LRCK pin will be an output pin. LRCK divider controlled by DIV_LRCK(Reg0x07.Bit[3:0] and Reg0x08[7:0]) is used to generate LRCK clock signal in master mode. In master mode, the duty of LRCK clock depends on the setting of SDP_OUT_FMT (Reg0x0A.Bit[1:0]).

In slave mode, LRCK divider is inactive and ES8311 will detect MCLK/LRCK ratio automatically.

- Register 0x07 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
TRI_BLRCK	5	BCLK/LRCK tri-state control 0 – normal (default) 1 – BCLK and LRCK tri-state output
TRI_ADCDAT	4	ADCDAT tri-state control 0 – normal (default) 1 – ADCDAT tri-state output
DIV_LRCK[11:8]	3:0	Master LRCK divider bit 11 to bit 8 LRCK(master)=dig_mclk/(LRCK_DIV+1)

- Register 0x08 – CLOCK MANAGER, DEFAULT 1111 1111

Bit Name	Bit	Description
DIV_LRCK[7:0]	7:0	Master LRCK divider bit 11 to bit 8 LRCK(master)=dig_mclk/(LRCK_DIV+1)

9 CHIP CONTROL AND POWER MANAGEMENT

ES8311 has an internal power-on reset (POR) circuit to monitor voltage on DVDD pin. It automatically releases an internal reset signal when voltage on DVDD pin reaches the defined thresholds. No external clocks are required for the POR circuit.

ES8311 is a low power codec and it has some control registers to do digital circuit reset and power control.

9.1 RESET CONTROL

Register 0x00 is used to reset the internal digital circuit. The power consumption in reset mode is much lower than that in normal mode.

- Register 0x00 –Reset, Default 0001 1111

Bit Name	Bit	Description
CSM_ON	7	Chip current state machine control 0 – csm power down(default) 1 – csm power on
RST_DIG	4	Digital reset 0 – not reset 1 – reset digital except control port block(default)
RST_CMG	3	Clock manager block reset 0 – not reset

		1 – reset clock manager block(default)
RST_MST	2	Master block reset 0 – not reset 1 – reset master block(default)
RST_ADC_DIG	1	ADC digital block reset 0 – not reset 1 – reset ADC digital block (default)
RST_DAC_DIG	0	DAC digital block reset 0 – not reset 1 – reset DAC digital block(default)

CSM_ON (Reg0x00.Bit[7]) is the control bit for internal state machine. The state machine is in power down state while codec power up. CSM_ON must be set to '1' to start up state machine in normal mode.

RST_DIG controlled by Reg0x00.Bit[4] is used to reset internal digital circuit except for I2C control port. Set RST_DIG to '1' will assert reset signal for internal digital circuit.

RST_CMG controlled by Reg0x00.Bit[3] is used to reset internal clock manager. Set RST_CMG to '1' will assert reset signal.

Set RST_ADC_DIG (Reg0x00.Bit[1]) to '1' will reset digital circuit of ADC, and Set RST_DAC_DIG(Reg0x00.Bit[0]) to '1' will reset digital circuit of DAC.

Set RST_MST (Reg0x00.Bit[2]) to '1' will reset the circuit which works in master mode. RST_MST must be '0' when codec works in master mode. If codec works in slave mode, it is suggested to be '1' for the minimum power consumption.

It is suggested that releasing a software reset operation to clear the internal state while codec power up. The following is proposal procedure of software reset operation: set the reset bits to '1' to release reset signal and clear CSM_ON to '0' to power down state machine, then delay a short time, such as several milliseconds, clear reset bits to '0' and set CMS_ON to '1' at last.

Please set all reset bits to '1' and clear CSM_ON to '0' to minimize the power consumption when codec is ready for standby or sleep.

9.2 POWER UP / POWER DOWN CONTROL

Register 0x0D is used for power management.

- Register 0x0D – ***SYSTEM, DEFAULT 1111 1100***

Bit Name	Bit	Description
PDN_ANA	7	0 – enable analog circuits 1 – power down analog circuits
PDN_IBIASGEN	6	0 – enable analog bias circuits 1 – power down analog bias circuits
PDN_ADCBIASGEN	5	0 – enable analog ADC bias circuits 1 – power down analog ADC bias circuits
PDN_ADCVERFGEN	4	0 – enable analog ADC reference circuits 1 – power down analog ADC reference circuits
PDN_DACVREFGEN	3	0 – enable analog DAC reference circuits 1 – power down analog DAC reference circuits
PDN_VREF	2	0 – disable internal reference circuits 1 – enable reference circuits
VMIDSEL	1:0	00 – power down 01 – start up vmid normal speed charge 10 – normal vmid operation 11 – start up vmid fast speed charge

When codec is ready for standby or sleep, the controls bits in register 0x0D should be set to '1' to minimize the power

consumption. The power consumption in standby or sleep mode is much lower than that in normal mode. In this user guide, there is a reference code for power down sequence.

9.3 LOW POWER CONTROL

In normal mode, the power consumption will be decreased signally if low power control is set. The audio performance, for example THD+N and SNR, will be slightly decreased.

- Register 0x0F– ***SYSTEM, DEFAULT 0000 0000***

Bit Name	Bit	Description
LPDAC	7	0 – normal mode 1 – low power mode for DAC
LPPGA	6	0 – normal mode 1 – low power mode for PGA
LPPGAOUT	5	0 – normal mode 1 – low power mode for PGA output
LPVCMMOD	4	0 – normal mode 1 – low power mode for ADC
LPADCVRP	3	0 – normal mode 1 – low power mode for ADC reference
LPDACVRP	2	0 – normal mode 1 – low power mode for DAC reference
LPFLASH	1	0 – normal mode 1 – low power mode for ADC
LPINT1	0	0 – normal mode 1 – low power mode for ADC

10 ANALOG INPUT AND ADC

The capture path of ES8311 includes differential input, PGA, mono ADC and digital serial port. ES8311 only has one fully differential analog input as microphone input. The analog input signal will be boosted by internal PGA and then be fed into mono ADC. The digital output from ADC is fed into a DATA multiplexer which can select input signal for DSP block between ADC output and DMIC data. The feature of DSP block includes filter, volume controls, ALC and equalizer. Then, the output of DSP block will be combined with the data from DSDIN pin, and the data bits will output serially on ASDOUT pin.

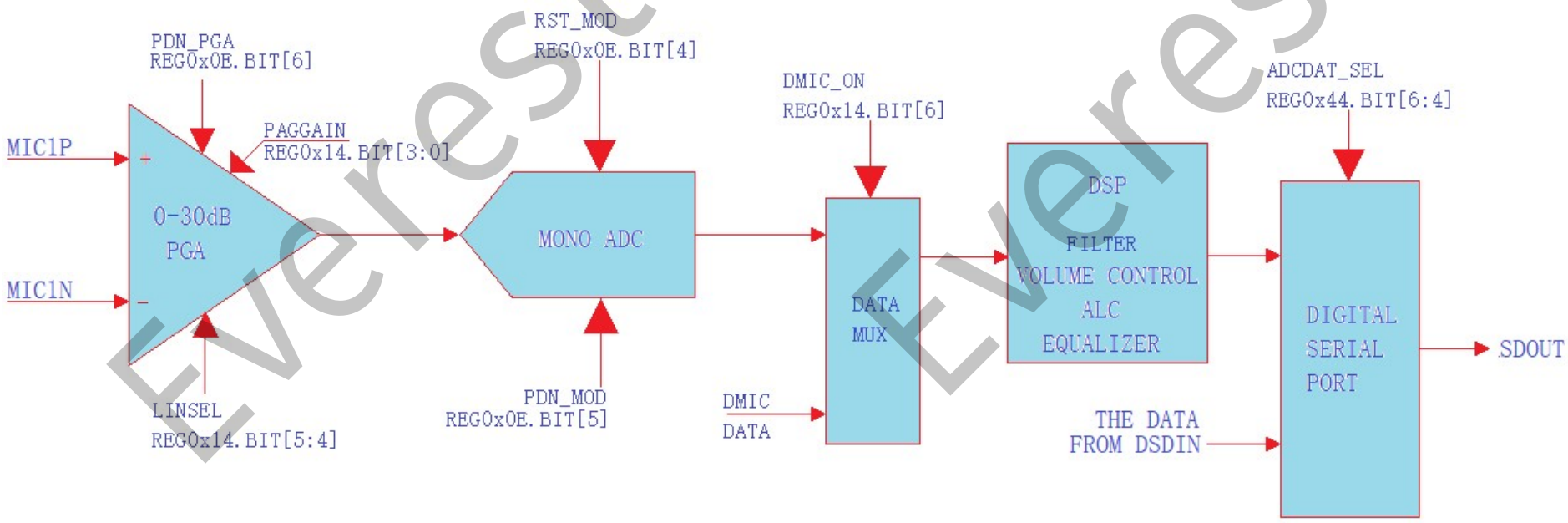

Figure 20. Analog input and output Diagram

10.1 DIFFERENTIAL INPUT AND PGA

The input path of ES8311 includes one fully differential input and a PGA with 0dB to 30dB gain range. LINSESL controlled by Reg0x14.Bit[5:4] selects this differential input. PDN_PGA controlled by Reg0x0E.Bit[6] enable or disable this PGA. PGAGAIN controlled by Reg0x14.Bit[3:0] selects gain for PGA.

➢ Register 0x0E – ***SYSTEM, DEFAULT 0110 1010***

Bit Name	Bit	Description
PDN_PGA	6	0 – enable analog PGA circuits 1 – power down analog PGA circuits(default)

➢ Register 0X14 – ***SYSTEM, DEFAULT 0001 0000***

Bit Name	Bit	Description
DMIC_ON	6	DMIC SDA slection 0 – no DMIC 1 – select DMIC and DMIC_SDA from MIC1P
LINSEL	5:4	0 – no input selection 1 – select Mic1p-Mic1n 2 – select Mic2p-Mic2n 3 – select both pairs of Mic1 and Mic2
PGAGAIN	3:0	ADC PGA gain 0 – 0dB 1 – 3dB 2 – 6dB 3 – 9dB 4 – 12dB 5 – 15dB 6 – 18dB 7 – 21dB 8 – 24dB 9 – 27dB 10 – 30dB

The fully differential input is microphone interface, and it isn't recommended for line input. Below circuit illustrates how to connect microphone to differential input of ES8311. ES8311 doesn't have MICBIAS pin for microphone, so the analog power supply of ES8311 must be used for microphone bias voltage.

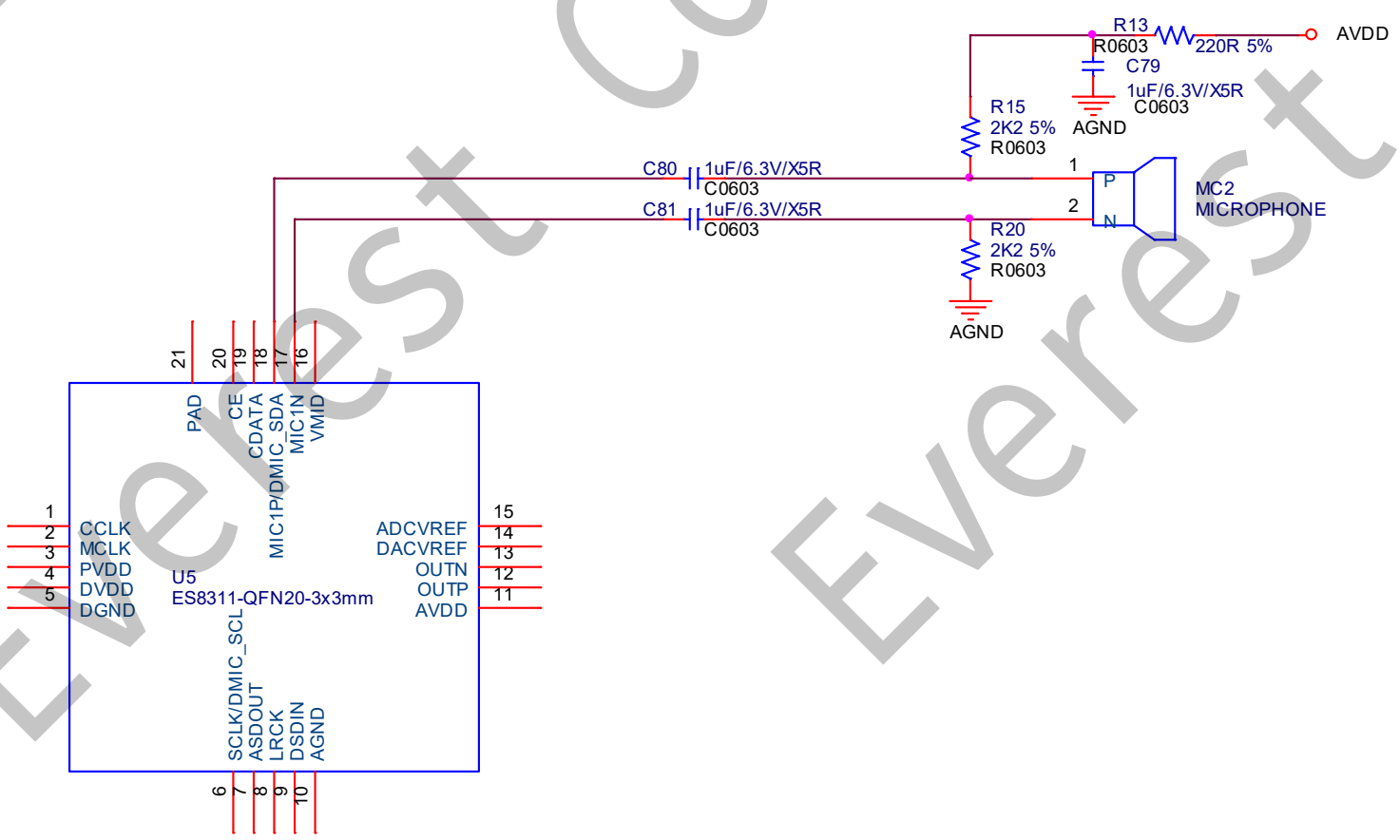

Figure 21. Application Circuit for ECM

The PGA of ES8311 is a low noise PGA with excellent noise performance, and its noise only increases slightly even if gain of PGA is set to maximum.

10.2 MONO ADC AND DATA MUX

PDN_MOD controlled by Reg0x0E.Bit[5] is the power control for mono ADC. PDN_MOD = '1' will power down ADC modulator.

RST_MOD controlled by Reg0x0E.Bit[4] is the reset of mono ADC. RST_MOD = '1' will reset ADC modulator.

Please set PDN_MOD and RST_MOD to '1' to minimize power consumption when ADC or Codec is ready for standby or sleep.

- Register 0x0E – ***SYSTEM, DEFAULT 0110 1010***

Bit Name	Bit	Description
PDN_MOD	5	0 – enable analog ADC modulator 1 – power down analog ADC modulator(default)
RST_MOD	4	0 – disable(default) 1 – reset modulator

10.3 HIGH PASS FILTER, VOLUME CONTROLS, ALC AND EQUALIZER

The digital output of mono ADC is fed into a DSP block which has features including high pass filter, volume control, ALC and equalizer.

10.3.1 HIGH PASS FILTER

ADC_HPF controlled by Reg0x1C.Bit[5] is used to freeze or active internal high pass filter. This high pass filter can cancel the DC offset in digital domain. ADC_HPFS1 and ADC_HPFS2 is the coefficient of high pass filter. The frequency response of this filter will be updated if the coefficient has been changed. This high pass filter can be used to attenuate low-frequency noise if the suitable coefficient is used for it.

ADC_HPF = '1' actives this high pass filter and set it into dynamic mode. In this mode, the DC offset will be canceled dynamically, and it will slightly decrease SNR of ADC.

ADC_HPF = '0' freezes this high pass filter. In this mode, the DC offset is frozen and a constant DC offset exists in digital domain. If there is a constant DC offset in application, ADC_HPF can be cleared to freeze DC offset.

Also, this high pass filter can be disabled with two methods as following.

1. Clear ADC_HPF to '0' before the state machine startup. It will freeze DC offset to zero.
2. Set ADC_RAMCLR to '1' when ADC_HPF has been cleared to '0'. It will clear all data in RAM, including DC offset.

- Register 0X16 – ***ADC, DEFAULT 0000 0100***

Bit Name	Bit	Description
ADC_ RAMCLR	3	adc ram clear when lrck/adc_mclk active

- Register 0X1B – ***ADC, DEFAULT 0000 1100***

Bit Name	Bit	Description
ADC_HPFS1	4:0	ADCHPF stage1 coeff

- Register 0X1C – ***ADC, DEFAULT 0100 1100***

Bit Name	Bit	Description
ADC_HPF	5	ADC offset freeze 0 – freeze offset 1 – dynamic HPF
ADC_HPFS2	4:0	ADCHPF stage2 coeff

10.3.2 VOLUME CONTROL AND ALC

ES8311 ADC has a digital volume register and ALC (automatic level control) registers. ADC_VOLUME controlled by register 0x17 is used for digital volume.

If ALC is enabled, the ADC_VOLUME register is the max gain of ALC, and the recording volume depends on ALC.

If ALC is disabled, the recording volume is controlled by ADC_VOLUME register. The digital volume has a range from -95.5dB to +32dB with a resolution in 0.5dB/step.

- Register 0X17 – ***ADC, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADC_VOLUME	7:0	ADC volume 0x00 – -95.5dB (default) 0x01 – -90.5dB … 0.5dB/step 0xBE – -0.5dB 0xBF – 0dB 0xC0 – +0.5dB … 0xFF – +32dB

- Register 0X18 – ***ADC, DEFAULT 0000 0000***

Bit Name	Bit	Description
ALC_EN	7	ADC auto level control enable 0 – ALC disable(default) 1 – ALC enable
ADC_AUTOMUTE_EN	6	ADC automute enable 0 – automute disable(default) 1 – automute enable
ALC_WINSIZE	3:0	winsize for alc cnt_timer[ALC_WINSIZE] 0 – 0.25dB/2LRCK 1 – 0.25dB/4LRCK ... 15 – 0.25dB/65536LRCK

- Register 0X19 – ***ADC, DEFAULT 0000 0000***

Bit Name	Bit	Description
ALC_MAXLEVEL	7:4	ALC target max level 0 – -30.1dB 1 – -24.1dB 2 – -20.6dB 3 – -18.1dB 4 – -16.1dB 5 – -14.5dB 6 – -13.2dB 7 – -12.0dB 8 – -11.0dB 9 – -10.1dB 10 – -9.3 dB 11 – -8.5 dB 12 – -7.8 dB 13 – -7.2 dB 14 – -6.6 dB 15 – -6.0 dB
ALC_MINLEVEL	3:0	ALC target min level 0 – -30.1dB 1 – -24.1dB 2 – -20.6dB

		3 – -18.1dB 4 – -16.1dB 5 – -14.5dB 6 – -13.2dB 7 – -12.0dB 8 – -11.0dB 9 – -10.1dB 10 – -9.3 dB 11 – -8.5 dB 12 – -7.8 dB 13 – -7.2 dB 14 – -6.6 dB 15 – -6.0 dB

➢ Register 0X1A – ***ADC, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADC_AUTOMUTE_WS	7:4	ADC automute winsize Detect samples= (2^11)*(winsize+1) 0 – 2048 samples - 42ms 1 – 4096 samples - 84ms ... 15 – 32768 samples - 688ms
ADC_AUTOMUTE_NG	3:0	ADC automute noise gate 0 – -96dB 1 – -90dB 2 – -84dB 3 – -78dB 4 – -72dB 5 – -66dB 6 – -60dB 7 – -54dB 8 – -51dB 9 – -48dB 10 – -45dB 11 – -42dB 12 – -39dB 13 – -36dB 14 – -33dB 15 – -30dB

10.3.3 EQUALIZER

ES8311 ADC has an equalizer which is a 2nd filter. This equalizer can be programmed as low pass filter or high pass filter. A band-pass filter can be realized if this equalizer has been combined with the high pass filter descripted in section 10.3.1.

If this equalizer is used for ADC recording, the clock ratio between internal ADC MCLK and LRCK must be equal or greater than 256.

This equalizer can be bypassed if ADC_EQBYPASS is set to '1'. In this mode, the clock ratio between internal ADC MCLK and LRCK must be equal or greater than 240.

Register 0x1E to Register 0x30 are all the coefficient of equalizer. Everest can provide a tool to calculate the coefficient of equalizer. You can get this tool from Everest Semiconductor co., Ltd.

➢ Register 0X1C – ***ADC, DEFAULT 0100 1100***

Bit Name	Bit	Description
ADC_EQBYPASS	6	ADCEQ bypass 0 – normal

		1 – bypass (default)

- Register 0X1D – ***ADC, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B0[29:24]	5:0	30-bit B0 coefficient for ADCEQ

- Register 0X1E – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B0[23:16]	7:0	30-bit B0 coefficient for ADCEQ

- Register 0X1F – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B0[15:8]	7:0	30-bit B0 coefficient for ADCEQ

- Register 0X20 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B0[7:0]	7:0	30-bit B0 coefficient for ADCEQ

- Register 0X21 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_A1[29:24]	7:0	30-bit A1 coefficient for ADCEQ

- Register 0X22 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_A1[23:16]	7:0	30-bit A1 coefficient for ADCEQ

- Register 0X23 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_A1[15:8]	7:0	30-bit A1 coefficient for ADCEQ

- Register 0X24 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_A1[7:0]	7:0	30-bit A1 coefficient for ADCEQ

- Register 0X25 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_A2[29:24]	7:0	30-bit A2 coefficient for ADCEQ

- Register 0X26 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_A2[23:16]	7:0	30-bit A2 coefficient for ADCEQ

- Register 0X27 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_A2[15:8]	7:0	30-bit B0 coefficient for ADCEQ

- Register 0X28 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_A2[7:0]	7:0	30-bit A2 coefficient for ADCEQ

- Register 0X29 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B1[29:24]	7:0	30-bit B1 coefficient for ADCEQ

- Register 0X2A – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B1[23:16]	7:0	30-bit B1 coefficient for ADCEQ

- Register 0X2B – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B1[15:8]	7:0	30-bit B1 coefficient for ADCEQ

- Register 0X2C – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B1[7:0]	7:0	30-bit B1 coefficient for ADCEQ

- Register 0X2D – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B2[29:24]	7:0	30-bit B2 coefficient for ADCEQ

- Register 0X2E – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B2[23:16]	7:0	30-bit B2 coefficient for ADCEQ

- Register 0X2F – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B2[15:8]	7:0	30-bit B2 coefficient for ADCEQ

- Register 0X30 – ***ADCEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCEQ_B2[7:0]	7:0	30-bit B2 coefficient for ADCEQ

10.4 DIGITAL FEEDBACK

The data from DSP block can be outputted serially on ASDOUT pin. ES8311 has a flexible digital feedback feature which combines the data from DSP block and data from DSDIN pin, output this combined data serially on ASDOUT. This is an interesting feature and it will be helpful in the application which need to do echo cancellation.

ADCDAT_SEL controlled by Reg0x44.Bit[6:4] is used for this digital feedback feature.

- Register 0X44 – ***GPIO, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADCDAT_SEL	6:4	ADCDAT output select 0 – ADC + ADC (default) 1 – ADC + 0 2 – 0 + ADC 3 – 0 + 0 4 – DACL + ADC 5 – ADC + DACR 6 – DACL + DACR 7 – NA

In the application which need digital feedback, ADCDAT_SEL can be set to 4 or 5. Below diagram shows the I2S/PCM data alignment in both default mode and digital feedback mode.

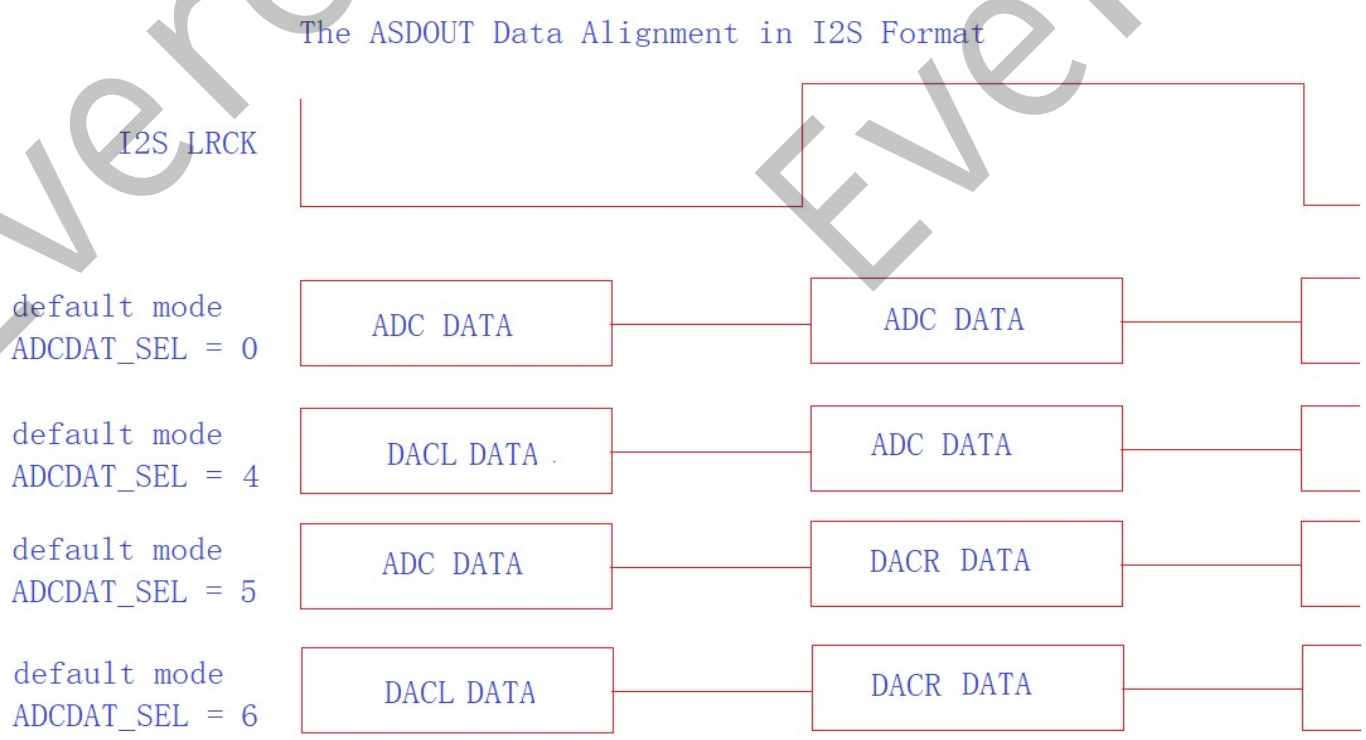

Figure 22. Digital Feedback timing

10.5 DIGITAL MICROPHONE

ES8311 has a digital microphone interface to connect one PDM digital microphone. MIC1P of ES8311 is a multiplexing pin for analog input and DMIC data input. ES8311 can't provide clock for digital microphone so that digital microphone shares clock signal with BCLK/SCLK of I2S.

DMIC_ON = '1' enable digital microphone interface, and DMIC_ON = '0' disable digital microphone interface.

The data of digital microphone will be latched at high level of clock while DMIC_SENSE is cleared to '0'. Otherwise, the data of digital microphone will be latched at low level of clock.

- Register 0X14 – ***SYSTEM, DEFAULT 0001 0000***

Bit Name	Bit	Description
DMIC_ON	6	DMIC SDA slection 0 – no DMIC 1 – select DMIC and DMIC_SDA from MIC1P

- Register 0X15 – ***ADC, DEFAULT 0000 0000***

Bit Name	Bit	Description
DMIC_SENSE	0	DMIC data latch sense 0 – at clock positive edge 1 – at clock negative edge

Below is the application circuit of digital microphone.

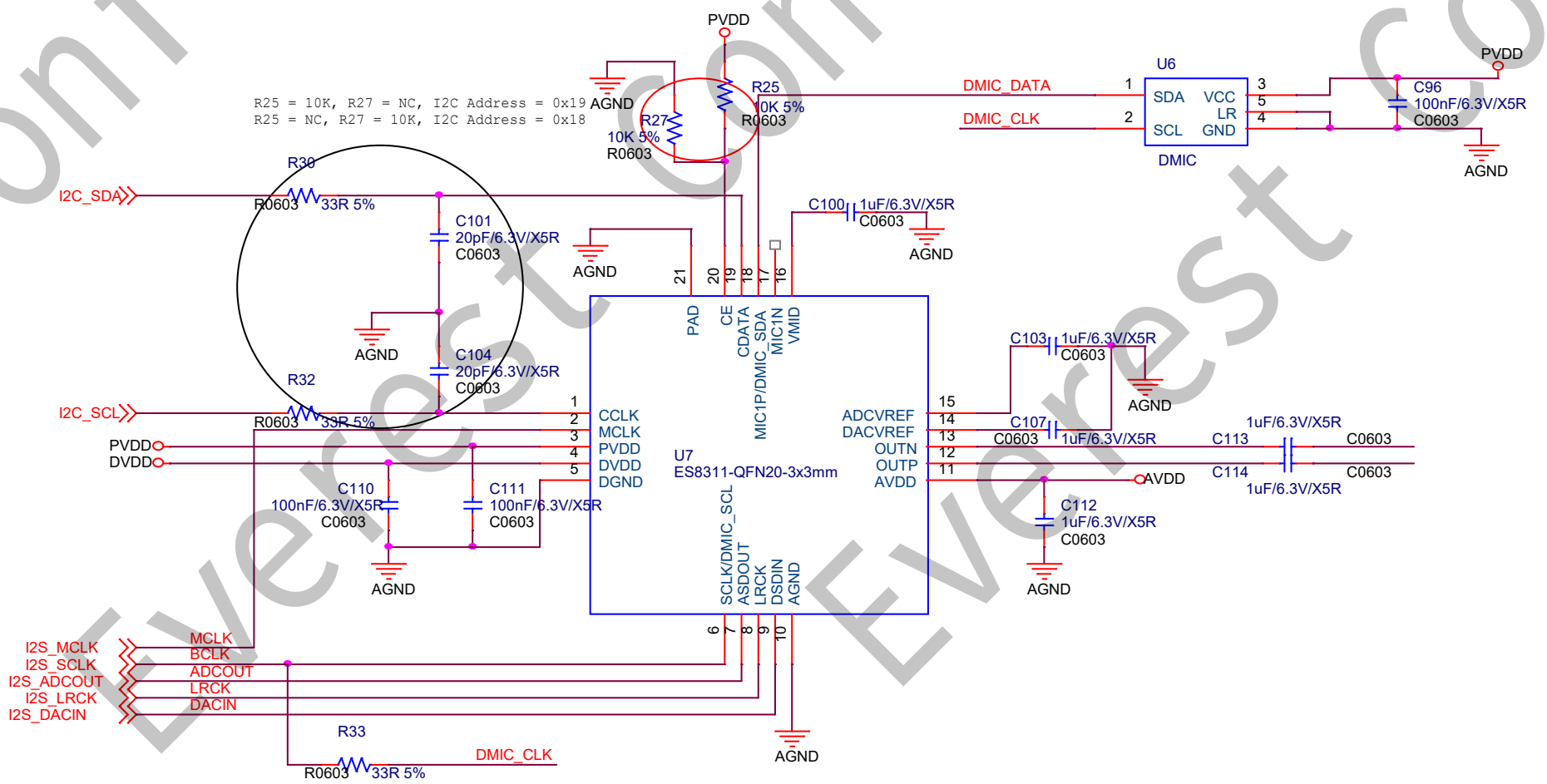

Figure 23. Application Circuit For PDM DMIC

10.6 ADC SPEED MODE, ADC OVER SAMPLE RATE AND ADC SCALE

The ADC in ES8311 can work in single speed or double speed mode. ADC_FSMODE = '0' selects single speed mode and ADC_FSMODE = '1' selects double speed mode.

ADC_OSR is the definition of ADC over sample rate. OSR must be equal or greater than 15 in single speed mode, and must be equal or greater than 16 in double speed mode. So please don't set ADC_OSR to the value equal or lower than 14. Below is the

equation of ADC_OSR. The default of ADC OSR is 32.

1. Single speed, OSR = (internal adc mclk) ÷ LRCK ÷ 8
2. Double speed, OSR = (internal adc mclk) ÷ LRCK ÷ 4

➢ Register 0x03 – ***CLOCK MANAGER, DEFAULT 0001 0000***

Bit Name	Bit	Description
ADC_FSMODE	6	adc fs mode 0 – single speed(default) 1 – double speed
ADC_OSR	5:0	ADC delta sigma over sample rate 0~14 – not use 15 – 60*fs(ss) / (ds not support) 16 – 64*fs(ss) / 32*fs(ds) (default) ... 31 – 124*fs(ss) / 62*fs(ds) 32 – 128*fs(ss) / 64*fs(ds) ... 63 – 252*fs(ss) / 126*fs(ds)

ADC OSR will affect amplitude of the digital signal out from ADC. The smaller ADC OSR, the lower signal amplitude. ADC_SCALE can compensate the amplitude for the ADC digital signal if the ADC OSR is lower than default. If ADC_SCALE isn't used for compensation while small number for OSR, the SNR of ADC will be lower than default because of the small amplitude.

➢ Register 0X16 – ***ADC, DEFAULT 0000 0100***

Bit Name	Bit	Description
ADC_ SCALE	2:0	ADC gain scale up 0 - 0dB 1 - 6dB 2 - 12dB 3 - 18dB 4 - 24dB (default) 5 - 30dB 6 - 36dB 7 - 42dB

10.7 FADE IN AND FADE OUT

ES8311 ADC has a fade in and fade out feature. ADC_RAMPRATE can enable or disable fade in and fade out feature, and select the ramp rate.

➢ Register 0X15 – ***ADC, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADC_RAMPRATE	7:4	ADC VC ramp rate 0 - disable softramp 1 - 0.25dB/4LRCK 2 - 0.25dB/8LRCK 3 - 0.25dB/16LRCK 4 - 0.25dB/32LRCK 5 - 0.25dB/64LRCK 6 - 0.25dB/128LRCK 7 - 0.25dB/256LRCK 8 - 0.25dB/512LRCK 9 - 0.25dB/1024LRCK 10 - 0.25dB/2048LRCK 11 - 0.25dB/4096LRCK 12 - 0.25dB/8192LRCK 13 - 0.25dB/16384LRCK 14 - 0.25dB/32768LRCK

		15 - 0.25dB/65536LRCK

11 ES8311 DAC AND OUTPUT PATH

The playback path of ES8311 includes serial digital port, DAC and differential output. ES8311 only has a mono DAC and a fully differential analog output. The bit stream on DSDIN pin is received by serial digital port, and be transferred to internal DSP block which provides filter, volume control, dynamic range control and equalizer features. Mono DAC converts digital to analog, then the analog signal exists on the fully differential out pins.

Below is the diagram of playback path of ES8311.

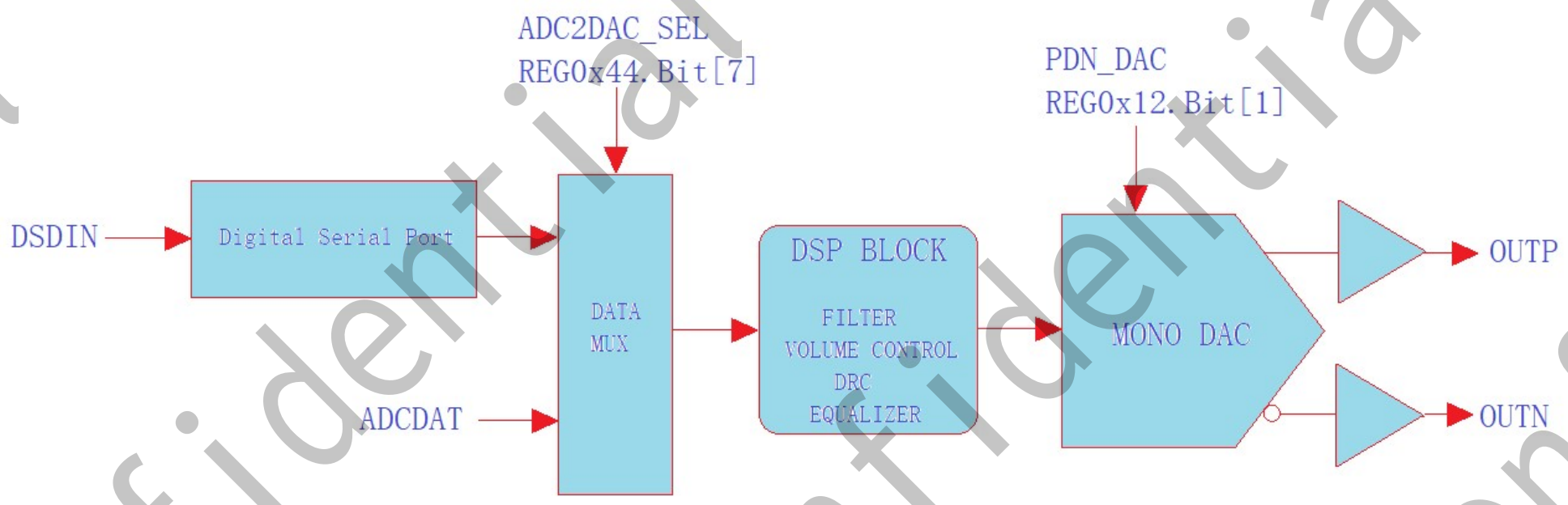

Figure 24. DAC and Output Diagram

11.1 DATA SOURCE OF DAC

ADC2DAC_SEL selects data source for mono DAC. ADC2DAC_SEL = '0' selects the output of digital serial port as source of mono DAC, and ADC2DAC_SEL = '1' selects the digital output of ADC as source of mono DAC.

- Register 0X44 – ***GPIO, DEFAULT 0000 0000***

Bit Name	Bit	Description
ADC2DAC_SEL	7	ADC data to DAC 0 – disable(default) 1 – ADC to DAC

If ADC2DAC_SEL is cleared to '0' and data of digital serial port is select for DAC source, user can select left data or right data of digital serial port for mono DAC. SDP_IN_SEL selects left or right data for DAC.

- Register 0x09 – ***SDP, DEFAULT 0000 0000***

Bit Name	Bit	Description
SDP_IN_SEL	7	SDP in data select 0 – Left channel data to DAC(default) 1 – right channel data to DAC

11.2 FADE IN AND FADE OUT

ES8311 DAC has a fade in and fade out feature. DAC_RAMPRATE can enable or disable fade in and fade out feature, and select the ramp rate.

- Register 0X37 – ***DAC, DEFAULT 0000 1000***

Bit Name	Bit	Description

DAC_RAMPRATE	7:4	DAC VC/DRC ramp rate 0 - disable softramp(default) 1 - 0.25dB/4LRCK 2 - 0.25dB/8LRCK 3 - 0.25dB/16LRCK 4 - 0.25dB/32LRCK 5 - 0.25dB/64LRCK 6 - 0.25dB/128LRCK 7 - 0.25dB/256LRCK 8 - 0.25dB/512LRCK 9 - 0.25dB/1024LRCK 10 - 0.25dB/2048LRCK 11 - 0.25dB/4096LRCK 12 - 0.25dB/8192LRCK 13 - 0.25dB/16384LRCK 14 - 0.25dB/32768LRCK 15 - 0.25dB/65536LRCK

11.3 DAC VOLUME AND DYNAMIC RANGE CONTROL

DAC_VOLUME is digital volume control for DAC with range from -95.5dB to +32dB in 0.5dB/step resolution.

- Register 0X32 – ***DAC, DEFAULT 0000 0000***

Bit Name	Bit	Description
DAC_VOLUME	7:0	DAC volume 0x00 – -95.5dB (default) 0x01 – -90.5dB … 0.5dB/step 0xBE – -0.5dB 0xBF – 0dB 0xC0 – +0.5dB … 0xFF – +32dB

There are several mute control bits for ES8311 DAC. Set these mute bits to '1' will mute DAC.

- Register 0X31 – ***DAC, DEFAULT 0000 0000***

Bit Name	Bit	Description
DAC_DSMMUTE_TO	7	DAC DSM mute target 0 – mute to 8 (default) 1 – mute to 7/9
DAC_DSMMUTE	6	DAC DSM mute control 0 – unmute(default) 1 – mute
DAC_DEMMUTE	5	DAC DEM mute control 0 – unmute(default) 1 – mute

ES8311 has a dynamic range control feature which will update the signal amplitude of DAC automatically. This feature will improve the experience on speaker or headphone even if the music volume is very soft. If dynamic range control (DRC) is enabled, the DAC_VOLUME is inactive and DAC_VOLUME is used for the maximum gain of DRC.

DRC_EN = '1' enables DRC feature and DRC_EN = '0' disables DRC feature. DRC_MAXLEVEL selects the target maximum level, and DRC_MINLEVEL selects the target minimum level. DRC_WINSIZE selects the window size time for volume detection.

When DRC is enabled, it automatically detects the maximum volume of digital signal in window size time controlled by DRC_WINSIZE. If the maximum volume is higher than the target maximum level, it will turn down the volume of digital signal in 0.25dB/step resolution with a ramp rate controlled by DAC_RAMPRATE. If the maximum volume is lower than the target

minimum level, it will turn up the volume of digital signal with the same ramp rate and resolution as volume up. The gain for volume up or down is controlled by DAC_VOLUME.

- Register 0X34 – ***DAC, DEFAULT 0000 0000***

Bit Name	Bit	Description
DRC_EN	7	DAC data range control enable 0 – disable drc(default) 1 – enable DRC
DRC_WINSIZE	3:0	winsize for DRC cnt_timer[DRC_WINSIZE] 0 – 0.25dB/2LRCK(default) 1 – 0.25dB/4LRCK ... 15 – 0.25dB/65536LRCK

- Register 0X35 – ***DAC, DEFAULT 0000 0000***

Bit Name	Bit	Description
DRC_MAXLEVEL	7:4	DRC target max level 15 – -6.0 dB 14 – -6.6 dB 13 – -7.2 dB 12 – -7.8 dB 11 – -8.5 dB 10 – -9.3 dB 9 – -10.1dB 8 – -11.0dB 7 – -12.0dB 6 – -13.2dB 5 – -14.5dB 4 – -16.1dB 3 – -18.1dB 2 – -20.6dB 1 – -24.1dB 0 – -30.1dB(default)
DRC_MINLEVEL	3:0	DRC target min level 15 – -6.0 dB 14 – -6.6 dB 13 – -7.2 dB 12 – -7.8 dB 11 – -8.5 dB 10 – -9.3 dB 9 – -10.1dB 8 – -11.0dB 7 – -12.0dB 6 – -13.2dB 5 – -14.5dB 4 – -16.1dB 3 – -18.1dB 2 – -20.6dB 1 – -24.1dB 0 – -30.1dB(default)

11.4 EQUALIZER

ES8311 DAC has an equalizer which is a 1st filter. This equalizer can be programmed as low pass filter or high pass filter.

This equalizer can be bypassed if DAC_EQBYPASS is set to '1'. Everest can provide a tool to calculate the coefficient of DAC equalizer. You can get this tool from Everest Semiconductor Co., Ltd.

- Register 0X37 – ***DAC, DEFAULT 0000 1000***

Bit Name	Bit	Description
DAC_EQBYPASS	3	DACEQ bypass 0 – enable(default) 1 – bypass

- Register 0X38 – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_B0[29:24]	5:0	30-bit B0 coefficient for DACEQ

- Register 0X39 – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_B0[23:16]	7:0	30-bit B0 coefficient for DACEQ

- Register 0X3a – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_B0[15:8]	7:0	30-bit B0 coefficient for DACEQ

- Register 0X3b – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_B0[7:0]	7:0	30-bit B0 coefficient for DACEQ

- Register 0X3c – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_B1[29:24]	7:0	30-bit B1 coefficient for DACEQ

- Register 0X3d – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_B1[23:16]	7:0	30-bit B1 coefficient for DACEQ

- Register 0X3e – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_B1[15:8]	7:0	30-bit B1 coefficient for DACEQ

- Register 0X3f – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_B1[7:0]	7:0	30-bit B1 coefficient for DACEQ

- Register 0X40 – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_A1[29:24]	7:0	30-bit A1 coefficient for DACEQ

- Register 0X41 – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_A1[23:16]	7:0	30-bit A1 coefficient for DACEQ

- Register 0X42 – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_A1[15:8]	7:0	30-bit A1 coefficient for DACEQ

- Register 0X43 – ***DACEQ, DEFAULT 0000 0000***

Bit Name	Bit	Description
DACEQ_A1[7:0]	7:0	30-bit A1 coefficient for DACEQ