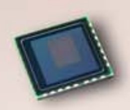
OV7740



datasheet

PRELIMINARY SPECIFICATION

1/5" CMOS VGA (640 x 480) CameraChip™ sensor
with OmniPixel3-HS™ technology

color CMOS VGA (640 x 480) CameraChip™ sensor with OmniPixel3-HS™ technology

datasheet (CSP3)
PRELIMINARY SPECIFICATION

version 1.21
july 2008

To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- PC multimedia

ordering information

- **OV07740-A32A** (color, lead-free)
  32-pin CSP3

features

- support for output formats: RAW RGB and YUV
- support for image sizes: VGA, and QVGA, CIF and any size smaller
- support for black sun cancellation
- support for internal and external frame synchronization
- standard SCCB serial interface
- digital video port (DVP) parallel output interface
- embedded one-time programmable (OTP) memory
- on-chip phase lock loop (PLL)
- embedded 1.5V regulator for core

key specifications

- **active array size:** 656 x 488
- **power supply:**
  core: 1.5VDC +/- 5% (internal regulator)
  analog: 3.3V +/- 5%
  I/O: 1.7 ~ 3.47V
- **power requirements:**
  active: TBD
  standby: TBD
- **temperature range:**
  operating: -30°C to 70°C (see table 8-1)
  stable image: 0°C to 50°C (see table 8-1)
- **output formats (8-bit):** 8-/10-bit Raw RGB data, 8-bit YUV
- **lens size:** 1/5"
- **lens chief ray angle:** TBD
- **input clock frequency:** 6 ~ 27 MHz
- **S/N ratio:** TBD
- **dynamic range:** TBD
- **maximum image transfer rate:**
  VGA (640x480): 60 fps for VGA
  QVGA (320x240): 120 fps for QVGA
- **sensitivity:** TBD
- **shutter:** TBD
- **scan mode:** progressive
- **maximum exposure interval:** 502 x t_{ROW}
- **gamma correction:** programmable
- **pixel size:** 4.2 µm x 4.2 µm
- **well capacity:** TBD
- **dark current:** TBD
- **fixed pattern noise (FPN):** TBD
- **image area:** 2755.2 µm x 2049.6 µm
- **package dimensions:** 4185 µm x 4345 µm

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pin numbers for the OV7740 image sensor. The package information is shown in **section 9**.

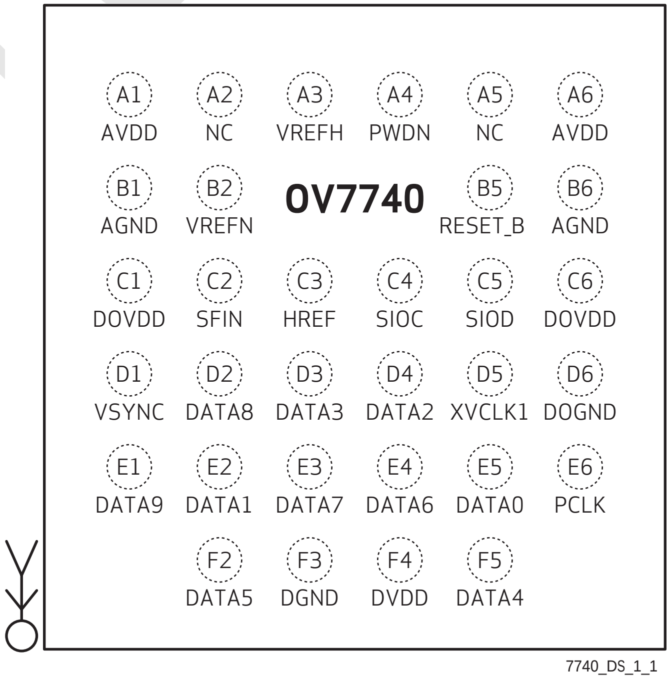
table 1-1 signal descriptions (sheet 1 of 2)

pin number	signal name	pin type	description	default I/O status
A1	AVDD	power	analog power	
A2	NC	–	no connect	
A3	VREFH	reference	reference voltage	
A4	PWDN	input	power down input with pull-down resistor (active high)	
A5	NC	–	no connect	
A6	AVDD	power	analog power	
B1	AGND	ground	analog ground	
B2	VREFN	reference	reference voltage	
B3	NC	–	no connect	
B4	NC	–	no connect	
B5	RESET_B	input	reset input with pull-up resistor (active low)	
B6	AGND	ground	analog ground	
C1	DOVDD	power	I/O power	
C2	SFIN	input	frame sync input	
C3	HREF	output	horizontal SYNC output	
C4	SIOC	SCCB	SCCB clock	
C5	SIOD	SCCB data	SCCB data	
C6	DOVDD	power	I/O power	
D1	VSYNC	I/O	vertical SYNC output	
D2	DATA8	I/O	DV port output	
D3	DATA3	I/O	DV port output	
D4	DATA2	I/O	DV port output (LSB in 8-bit mode)	
D5	XVCLK1	input	input clock	
D6	DOGND	ground	digital ground	
E1	DATA9	I/O	DV port output (MSB)	

table 1-1 signal descriptions (sheet 2 of 2)

pin number	signal name	pin type	description	default I/O status
E2	DATA1	I/O	DV port output	
E3	DATA7	I/O	DV port output	
E4	DATA6	I/O	DV port output	
E5	DATA0	I/O	DV port output (LSB in 10-bit mode)	
E6	PCLK	I/O	pixel clock output	
F1	NC	–	no connect	
F2	DATA5	I/O	DV port output	
F3	DGND	I/O	ground	
F4	DVDD	I/O	digital core power (internal regulator)	
F5	DATA4	I/O	DV port output	
F6	NC	–	no connect	

figure 1-1 pin diagram



top view

2 system level description

2.1 overview

The OV7740 (color) CameraChip™ sensor is a high performance VGA CMOS image sensor that provides the full functionality of a single-chip VGA camera using OmniPixel3-HS™ technology in a small footprint package. It provides full-frame, sub-sampled, windowed or scaled 8-bit/10-bit images in various formats via the control of the Serial Camera Control Bus (SCCB) interface.

The OV7740 has an image array capable of operating at up to 60 frames per second (fps) in VGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions including exposure control, gamma, white balance, color saturation, hue control, defective pixel canceling, noise canceling, etc., are programmable through the SCCB interface. In addition, Omnivision CameraChip sensors use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

For storage purposes, the OV7740 also includes one-time programmable (OTP) memory.

The OV7740 supports a digital video parallel port.

2.2 architecture

The OV7740 sensor core generates stream pixel data at a constant frame rate, indicated by YHREF and YVSYNC. The maximum pixel rate is 60 frames/second, corresponding to a pixel clock rate of 48 MHz. **figure 2-1** shows the functional block diagram of the OV7740 image sensor.

The timing generator outputs signals to access the rows of the image array, precharging and sampling the rows of array in series. In the time between precharging and sampling a row, the charge in the pixels decreases with the time exposed to the incident light, as known as exposure time.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through a analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs a 10-bit data for each pixel in the array.

figure 2-1 OV7740 block diagram

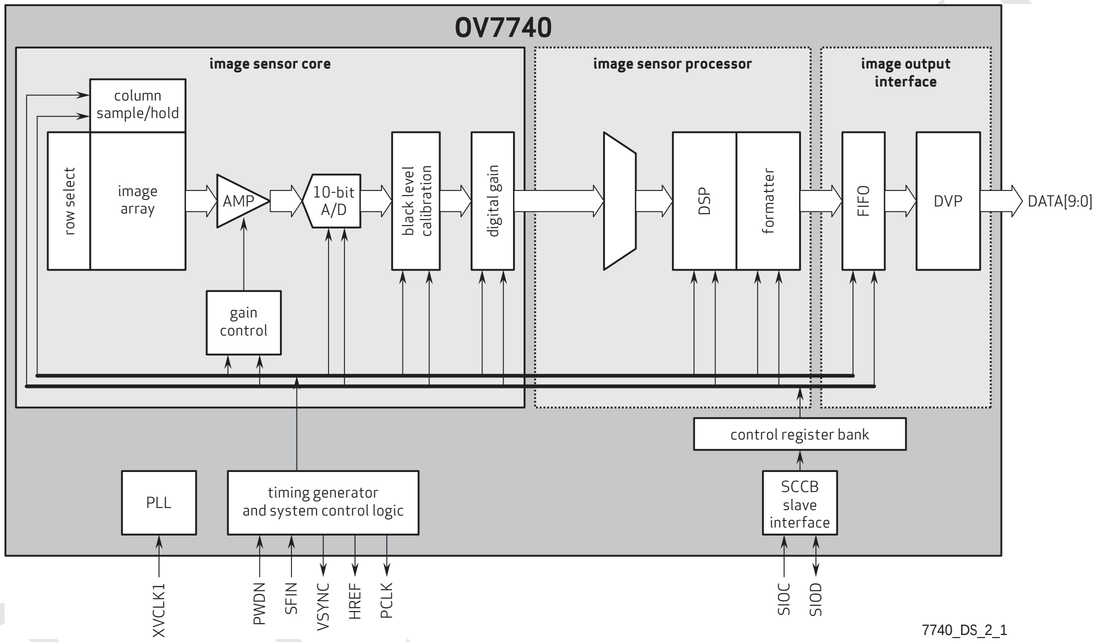
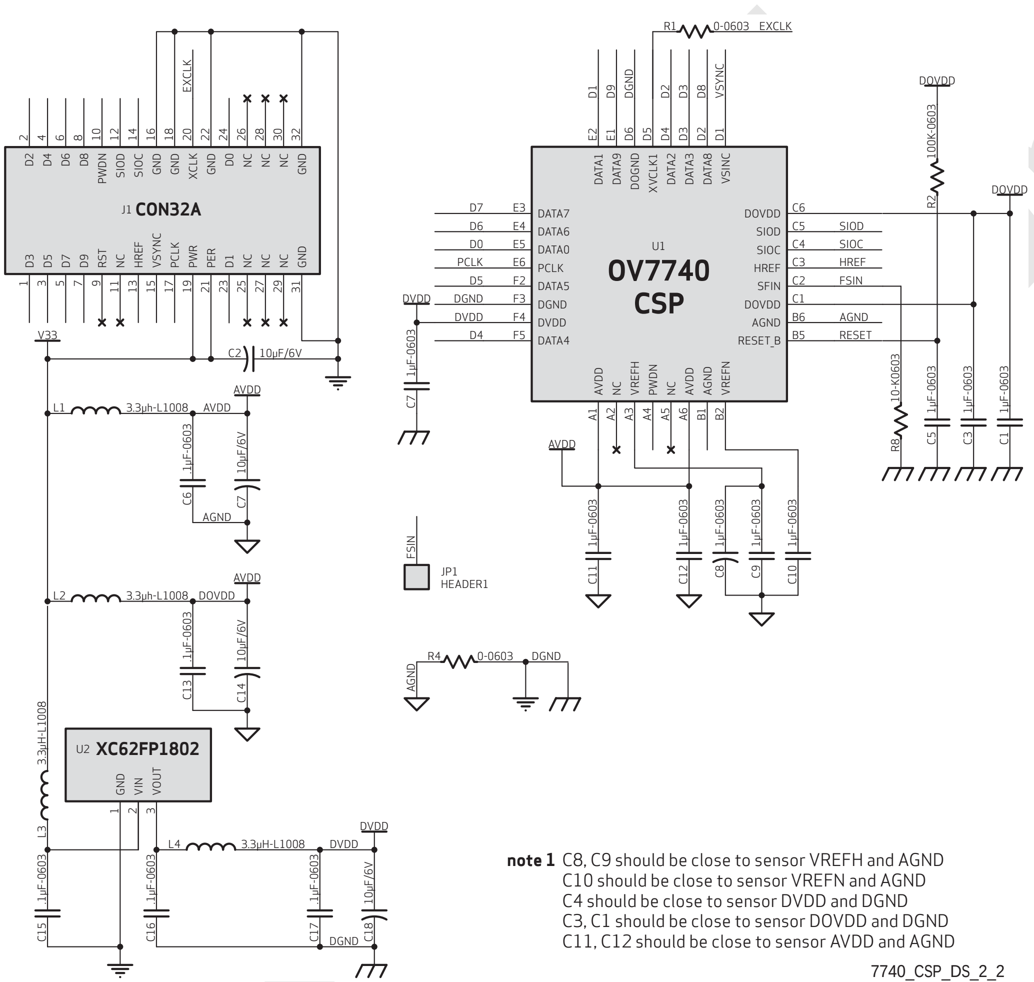


figure 2-2 reference design schematic



note 1 C8, C9 should be close to sensor VREFH and AGND
C10 should be close to sensor VREFN and AGND
C4 should be close to sensor DVDD and DGND
C3, C1 should be close to sensor DOVDD and DGND
C11, C12 should be close to sensor AVDD and AGND

7740_CSP_DS_2_2

2.3 I/O control

The OV7740 I/O pad direction and driving capability can be easily adjusted. **table 2-1** lists the driving capability and direction control registers of the I/O pins.

table 2-1 driving capability and direction control for I/O pads

function	register	description
output drive capability control	0x0E[1:0]	R_PAD[1:0]: output driving capability 00: 1x 01: 2x 10: 3x 11: 4x
DATA[9:0] IO control	0x54[7:5]	input/output selection of the pad pins DATA[9:0], 0x54[7] select DATA[9:2], 0x54[6:5] select DATA[1:0] 0: input 1: output
VSYNC IO control	0x54[1]	input/output selection of the pad pin VSYNC 0: input 1: output
PCLK IO control	0x54[0]	input/output selection of the pad pin PCLK 0: input 1: output
HREF IO control	0x54[2]	input/output selection of the pad pin HREF 0: input 1: output

2.4 format and frame rate

The OV7740 supports the following output formats: YUV422, RAW RGB and ITU656.

table 2-2 format and frame rate

format	resolution	frame rate	scaling method	pixel clock (YUV/RAW)
VGA	640x480	60 fps	full	48/24 MHz
CIF	352x288	60 fps	scaling down from VGA	48/24 MHz
QVGA	320x240	120 fps	sub sampling from VGA	48/24 MHz
QCIF	176x144	120 fps	scaling down from QVGA	48/24 MHz

2.5 SCCB interface

The Serial Camera Control Bus (SCCB) interface controls the CameraChip sensor operation. Refer to the OmniVision Technologies Serial Camera Control Bus (SCCB) Specification for detailed usage of the serial control port.

2.6 power up sequence

Powering up the OV7740 sensor does not require a special power supply sequence. The sensor includes an on-chip initial power-up reset feature. It will reset the whole chip during power up.

2.7 standby and sleep

Two suspend modes are available for the OV7740:

- hardware standby
- SCCB software sleep

To initiate hardware standby mode, the PWDN pin must be tied to high. When this occurs, the OV7740 internal device clock is halted and all internal counters are reset and registers are maintained.

Executing a software power-down through the SCCB interface suspends internal circuit activity but does not halt the device clock. All register content is maintained in standby mode.

3 block level description

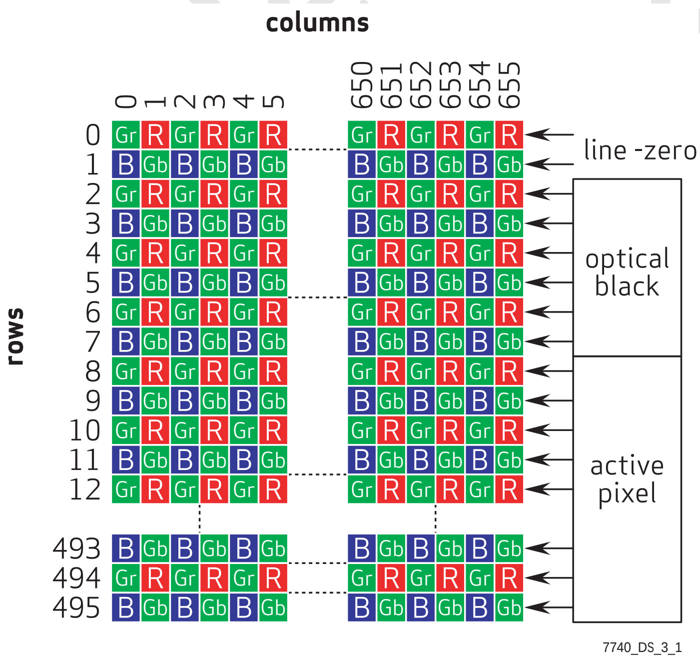
3.1 pixel array structure

The OV7740 sensor has an image array of 656 columns by 496 rows (325,376 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 325,376 pixels, 320,128 (656x488) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration read-out system with line-by-line transfer and an electronic shutter with a synchronous pixel read-out scheme.

figure 3-1 sensor array region color filter layout



4 image sensor core digital functions

4.1 mirror and flip

The OV7740 provides Mirror and Flip read-out modes, which respectively reverse the sensor data read-out order horizontally and vertically (see **figure 4-1**). In mirror mode, since the Bayer order changes from BGBG... to GBGB..., the read-out sequence will be adjusted automatically when the mirror function is on. In flip mode, the VREF starting line needs to be adjusted, then the ISP block will auto-detect whether the pixel is in red line or blue line and make necessary adjustments.

figure 4-1 mirror and flip samples

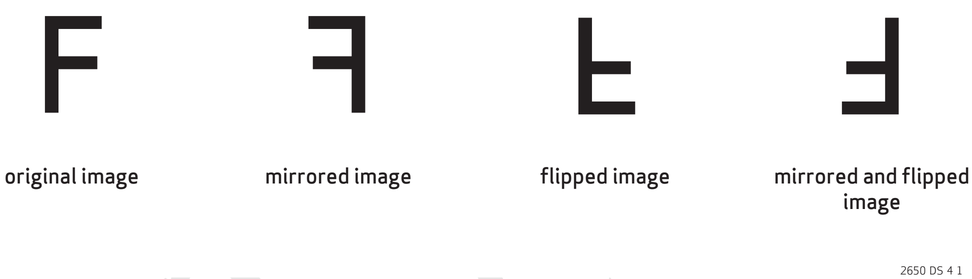


table 4-1 mirror and flip function control

function	register	description
mirror	0C [6]	mirror ON/OFF select 0: mirror OFF 1: mirror ON
flip	0C [7]	flip ON/OFF select 0: flip OFF 1: flip ON

4.2 test pattern

For testing purposes, the OV7740 offers one type pf test pattern: color bar. There are 4 modes of the color bar (see **figure 4-2**). The modes of the color bar can be set with the register 0x84[5:4](base address: 0x38[3:0] = 4'h8). In each mode the color bar can be moved from top to bottom if the bar moving function is enabled by setting signal(0x84[4]: base address: 0x38[3:0] = 4'h7) is 1. The moving step can be configured by setting the register 0x84[3:0](base address: 0x38[3:0] = 4'h8) (see **table 4-2**).

figure 4-2 test pattern

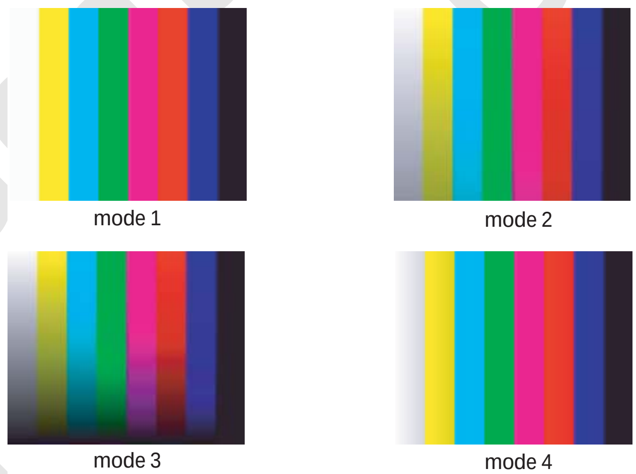


table 4-2 test pattern selection control

address	registe name	default value	R/W	description
0x84 0x38[3:0] = 4'h7	PRE CTRL00	0x00	RW	Bit[4]: bar_moving_en 0: color bar is a still image 1: color bar is a moving image Bit[1]: bar_en 0: output data are normal data 1: output data are color bar data
0x84 0x38[3:0] = 4'h8	PRE CTRL01	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: bar_style Output color bar style Bit[3:0]: bar_step Output color bar step

4.3 AEC/AGC algorithms

4.3.1 overview

The Auto Exposure Control (AEC) and Auto Gain Control (AGC) allows the CameraChip sensor to adjust the image brightness to a desired range by setting the proper exposure time and gain applied to the image. Besides automatic control, exposure time and gain can be set manually from external control. The related registers are listed in **table 4-3**.

table 4-3 AEC/AGC algorithms

function	register	description
AEC enable	0x13[0]	0: manual 1: auto
AEC (exposure time)	0x10 0x0F	0x10 = AEC[7:0] 0x0F = AEC[15:8]
LAEC (less than 1 row exposure time)	0x30 0x1F	0x30 = LAEC[15:8] 0x1F = LAEC[7:0]
AGC (gain)	0x15[1:0] 0x00	AGC[9:8] AGC[7:0]
AGC enable	0x13[2]	0: manual 1: auto

There are two different algorithms to tell whether the current frame is too bright or too dark and determine if the exposure time/gain should increase or decrease for the next frame. One algorithm Histogram, is based on the statistics of the percentage of high/low luminance pixels. The other is based on the weighted-average of a frame.

4.3.2 average-based algorithm

The average-based AEC controls image luminance using registers **WPT** (0x24) and **BPT** (0x25). In average-based mode, the value of register **WPT** (0x24) indicates the high threshold value and the value of register **BPT** (0x25) indicates the low threshold value. When the target image luminance average value **YAVG** (0x2F) is within the range specified by registers **WPT** (0x24) and **BPT** (0x25), the AEC keeps the image exposure. When register **YAVG** (0x2F) is greater than the value in register **WPT** (0x24), the AEC will decrease the image exposure. When register **YAVG** (0x2F) is less than the value in register **BPT** (0x25), the AEC will increase the image exposure. Accordingly, the value in register **WPT** (0x24) should be greater than the value in register **BPT** (0x25). The gap between the values of registers **WPT** (0x24) and **BPT** (0x25) controls the image stability.

The AEC function supports both normal and fast speed selections in order to bring the image exposure into the range set by the values in registers **WPT** (0x24) and **BPT** (0x25). AEC set to normal mode will allow for single-step increment or decrement in the image exposure to maintain the specified range. A value of "0" in register FASTEN[7] (0x13) will result in normal speed operation and a "1" will result in fast speed operation.

Register **VPT** (0x26) controls the fast AEC range. If the target image **YAVG** (0x2F) is greater than **VPT**[7:4] × 16, AEC will decrease by 2. If register **YAVG** (0x2F) is less than **VPT**[3:0] × 16, AEC will increase by 2.

As shown in **figure 4-3**, the AEC/AGC convergence uses two regions, the inner stable operating region and the outer control zone, which defines the convergence step size change as follows:

4.3.2.1 outside control zone
step size: 2 × (AEC[15:0])

t_{STEP}: t_{ROW} × (2 × AEC[15:0])

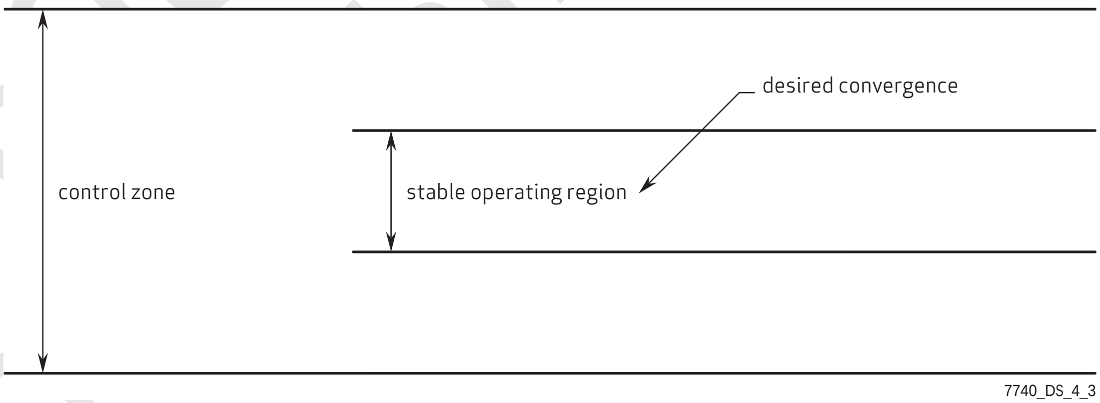
4.3.2.2 inside control zone
step size: 2 × (AEC[15:0]) ÷ 16)

t_{STEP}: t_{ROW} × (2 × AEC[15:0] ÷ 16)

Once the current value is inside the stable operating region, the AEC/AGC value has converged.

The Step Limit register acts to create a "middle ground" by limiting the maximum step size to 32 rows (delay time = t_{ROW} × 32).

figure 4-3 desired convergence



control zone upper limit: {**VPT**[7:4] (0x26[7:4]), 4'b0000}

control zone lower limit: {**VPT**[3:0] (0x26[3:0]), 4'b0000}

stable operating region upper limit: WPT[7:0] (0x24)

stable operating region lower limit: BPT[7:0] (0x25)

For the average-based AEC/AGC algorithm, the measured window is horizontally and vertically adjustable and divided into sixteen (4x4) zones (see **figure 4-4**). Each zone (or block) is 1/16th of the image and has a 4-bit weight in calculating the average luminance (YAVG). The 4-bit weight could be n/16 where n is from 0 to 15. The final YAVG is the weighted average of the sixteen zones. For more details on adjusting horizontal and vertical windows and weight for each window, refer to **section 4.3.2.3,** average luminance (YAVG).

4.3.2.3 average luminance (YAVG)

Auto exposure time calculation is based on a frame brightness average value. By properly setting AHS,AVS, AHW, and AVH as shown in **figure 4-4**, a 4x4 grid average window is defined. The average value is the weighted average of the 16 sections. **table 4-4** lists the corresponding registers.

There are two window modes: auto window mode and manual window mode. In auto window mode, the AHS, AVS, AHW and AVH are defined by sizes of output image. In the manual window mode, the window parameters are registers. **table 4-4** lists the corresponding registers. In order to use these register parameters, the yavg_win_man must be set to 1. Auto mode only supports non-scaling and non-subsampling image.

figure 4-4 average-based window definition

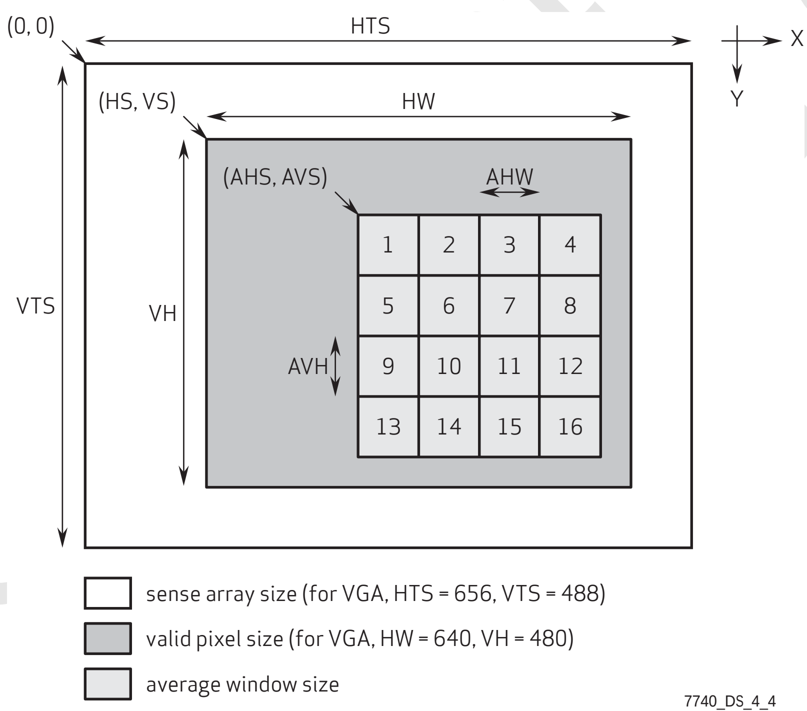


table 4-4 YAVG window registers (sheet 1 of 2)

function	register	description
AHS (horizontal starting pixel)	{0xE9[1:0] and 0x38[3:0]=4'h4, 0xE9 and 0x38[3:0]=4'h2}	0xE9[1:0] and 0x38[3:0]=4'h4: yavg_winofh[9:8] 0xE9 and 0x38[3:0]=4'h2: yavg_winofh[7:0] The horizontal offset of yavg window

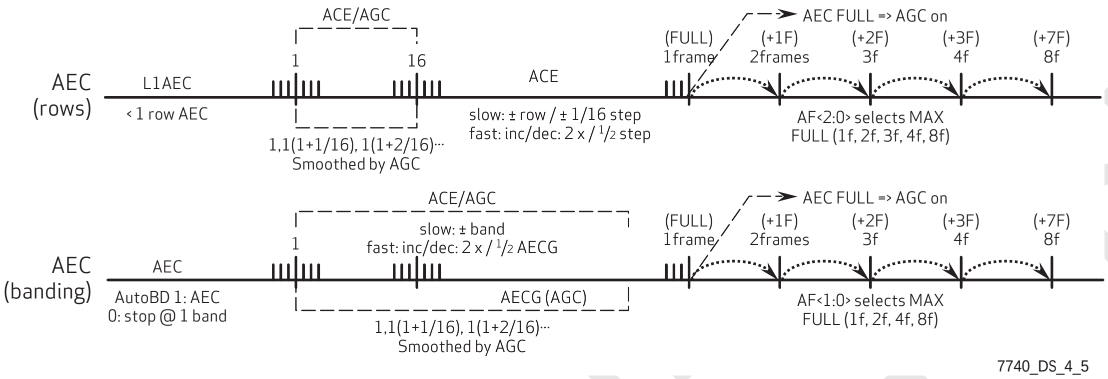
table 4-4 YAVG window registers (sheet 2 of 2)

function	register	description
AVS (vertical starting pixel)	{0xE9[4] and 0x38[3:0]=4'h4, 0xE9 &0x38[3:0]=4'h3}	0xE9[4] and 0x38[3:0]=4'h4: yavg_winofv[8] 0xE9 and 0x38[3:0]=4'h3: yavg_winofv[7:0] The vertical offset of yavg window
AHW (average section width)	0xE9 sub-address 0x38[3:0]=4'h5	horizontal size of cropping window. It will be multiplied by 8 to be real size.
AVH (average section height)	0xE9 sub-address 0x38[3:0]=4'h6	vertical size of cropping window. It will be multiplied by 4 to be real size.
average section weighting	0x56~0x59	0x56[1:0]: section 1 weight 0x56[3:2]: section 2 weight 0x56[5:4]: section 3 weight 0x56[7:6]: section 4 weight 0x57[1:0]: section 5 weight 0x57[3:2]: section 6 weight 0x57[5:4]: section 7 weight 0x57[7:6]: section 8 weight 0x58[1:0]: section 9 weight 0x58[3:2]: section 10 weight 0x58[5:4]: section 11 weight 0x58[7:6]: section 12 weight 0x59[1:0]: section 13 weight 0x59[3:2]: section 14 weight 0x59[5:4]: section 15 weight 0x59[7:6]: section 16 weight

4.4 AEC/AGC steps

figure 4-5 shows how the AEC and AGC work together to obtain adequate exposure/gain based on the current environment's illumination. The upper one illustrates the non-banding operation which time unit is based on Tline. The lower one shows exposure in banding. The x-axis represents the length of exposure in time scale. In normal light circumstances, the length of exposure will fall into a range from 1 Tline to 1 Tframe. In extremely bright or dark circumstances, exposure time less than 1 Tline/Tband or greater than 1 Tframe may be required accordingly. In order to achieve the best signal-to-noise ratio (SNR), extending the exposure time is always preferred, rather than raising the analog gain, when the current illumination is getting brighter. Vice versa, under dark conditions, the action to decrease the gain is always taken prior to shortening the exposure time.

figure 4-5 darker illumination situation brighter illumination situation



4.4.1 auto exposure control (AEC)

The function of the AEC is to calculate integration time of the next frame and send the information to the timing control block. Based on the statistics of previous frames, the AEC is able to determine whether the integration time should increase, decrease, fast increase, fast decrease, or remain the same.

In extremely bright situations, the LAEC activates, allowing integration time to be less than one row. In extremely dark situations, the VAEC activates, allowing integration time to be larger than one frame.

To avoid image flickering under a periodic light source, the integration time step can be adjusted as an integer multiple of the period of the light source. This new AEC step system is called banding, suggesting that the steps are not continuous but fall within bands.

4.4.1.1 LAEC

If the integration time is only one row but the image is too bright, AEC will enter LAEC mode. Within LAEC, the integration time can be further decreased to a minimum of 1/16 row or so. LAEC ON/OFF can be set in 0x13[3].

4.4.1.2 banding mode ON with AEC

When banding mode is ON, AEC step, which is also called 'band', increments by an integer multiple of the period of light intensity. This design is meant to reject image flickering when light source is not steady but periodical.

For a given operating frequency, band step can be expressed in terms of row timing.

Band Step = 'period of light intensity' × 'frame rate' × 'rows per frame'.

The band steps for 50Hz and 60Hz light sources can be set in registers 0x50~0x52.

When auto banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto banding is disabled, the minimum integration time is one minimal band. Auto banding can be set in register 0x13[4].

4.4.1.3 banding mode OFF with AEC

When Banding is OFF, integration time increases/decreases by 1/16 of the previous step in slow mode or becomes twice/half of the previous step in fast mode.

4.4.1.4 VAEC

In extremely dark situations, the integration time must be longer than one frame.

The OV7740 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x15[6:4]. VAEC can be disabled by setting register 0x15[7] to 0.

table 4-5 AEC and banding filter register

function	register	description
LAEC ON/OFF	**0x13**[3]	LAEC ON/OFF select 0: OFF 1: ON
banding ON/OFF	**0x13**[5]	banding ON/OFF 0: OFF 1: ON
VAEC ON/OFF (add frame)	0x15[7]	VAEC ON/OFF select 0: OFF 1: ON
auto banding	0x13[4]	auto banding select 0: OFF 1: ON
VAEC ceiling (max integration time)	0x15[6:4]	VAEC ceiling 001: 1 frame 010: 2 frames 011: 3 frames 1xx: 7 frames
banding step	0x50~0x52	0x52[7:6]=BD60st[9:8]; 0x51[7:0] = BD60st[7:0] 0x52[5:4]=BD50st[9:8]; 0x50[7:0] = BD50st[7:0]
maximum banding step	0x21	Bit[7:4]: for 50 Hz Bit[3:0]: for 60 Hz

4.4.2 auto gain control (AGC)

Unlike prolonging integration time, increasing gain will amplify both signal and noise or between two gaps of banding exposure time. Thus, AGC usually starts after AEC is full. However, in same cases where adjacent AEC step changes are too large (>1/16), AGC step should be inserted in between; otherwise, the integration time will keep switching from two adjacent steps and the image flickers.

4.4.2.1 integration time between 1~16 rows

When integration time is less than 16 rows, the changes between adjacent AEC steps are larger than 1/16, which may possibly make the image oscillate between two AEC levels; thus, some AGC steps are added in between. For example, from AEC = 2 rows to AEC = 3 rows, there are 7 more AGC steps (1+ x/16, x=1~7) inserted, which ensures every step change is less than 1/16.

4.4.2.2 gain insertion between AEC banding steps

In Banding ON mode, the minimal integration time change is the period of light intensity (10ms for 50Hz, 16.67ms for 60Hz). For the first 16 band steps, since the change between adjacent steps is larger than 1/16, AGC steps are inserted to ensure image stability.

4.4.2.3 gain insertion between VAEC steps

Between VAEC steps (e.g., integration time = 1 frame and 2 frames), AGC steps are inserted to ensure no adjacent step change is larger than 1/16 (6.25%).

4.5 black level calibration (BLC)

The pixel array contains six optically shielded (black) rows. These rows are used to provide the data for offset cancellation algorithms (black level calibration).

Digital image processing starts with black level subtraction. The BLC algorithm estimates the offset of the black level from the data provided by black rows. These offsets of different color channels will be subtracted from values of the color pixels. If the subtraction produces a negative result for a particular pixel, the value of this pixel is set to "0." By default, BLC will be triggered when gain is changing.

table 4-6 BLC control functions

function	register	description
target	0x67[5:0]	target black level value that is used in the algorithm
BLC_B, BLC_R	0x0E[6:5]	00: use all 4 channel offsets 01: use R/Gr channel offset for all channels 10: use B/Gb channel offset for all channels 11: use all 4 channel offsets
BLC always ON	0x64[5]	BLC offsets be adjusted every frame.
MBLC	0x69[3]	trigger BLC manually for 64 frames
Gr offset	0x6E[7:6], 0x6A[7:0]	BLC offset for Gr channel
Gb offset	0x6E[5:4], 0x6B[7:0]	BLC offset for Gb channel
R offset	0x6E[3:2], 0x6C[7:0]	BLC offset for R channel
B offset	0x6E[1:0], 0x6D[7:0]	BLC offset for B channel

4.6 DIG GAIN / EVEN ODD

After black level subtraction, multiplication may apply to all pixel values based on an optional digital gain. By default, the sensor will use analog gain up to its maximum before applying digital gain to the pixels.

table 4-7 digital gain control functions

function	register	description
DGAIN	0x15[1:0]	00: 1x digital gain 01: 2x digital gain 10: 2x digital gain 11: 4x digital gain

4.7 one-time programmable (OTP) memory

The OV7740 has a one-time programmable (OTP) memory to store chip identification and manufacturing information. This OTP memory is organized as 128-bit by 1 one-time programmable electrical fuse with random access interface. The main function is to store chip identification and manufacturing information.

The OTP has three operation modes: program (PGM), READ, and inactive. Normally, it is in inactive mode. By setting 0xEF to 0xAA, it enters program mode, which will sequentially burn data into the OTP macro. By setting 0xFE to 0x55, the OTP enters read mode, which will load the OTP data into registers. **table 4-8** summarizes the corresponding registers.

table 4-8 OTP registers

function	register	description
OTP program data	0xF0~0xFF	data to be programmed/read into/from OTP memory
OTP program/read enable	0xEF	0x55: read OTP memory 0xAA: program OTP memory

5 image sensor processor digital functions

5.1 DSP_TOP

The main purpose of the DSP_Top includes:

- integrate all sub-modules
- create necessary control signals

table 5-1 DSP top registers

address	register name	default value	R/W	description
0x80	DSP CTRL00	1'b1	RW	Bit[0]: ISP enable 0: Disable ISP 1: Enable ISP
0x83	DSP CTRL03	1'b0	RW	Bit[5]: Video switch 0: Video start 1: Video stop
0x84 sub address: 0x38[3:0]=4'h6	ROREG ADDR	0x00	R	Bit[7:0]: Read-only register address According to its value, the ISP SCCB outputs the value of different parameter.

5.2 DSP_PRE

The main purposes of the DSP_PRE module includes:

- adjust HREF, valid, RBlue signals and data
- create color bar image
- determine the sizes of input image by removing redundant data
- create control signals

table 5-2 DSP top registers

address	register name	default value	R/W	description
0x84 sub address: 0x38[3:0]=4'h7	PRE CTRL00	0x00	RW	Bit[7:5]: Reserved Bit[4]: bar_moving_en 0: Color bar is a still image 1: Color bar is a moving image Bit[3]: Reserved Bit[2]: rblue_rvs 0: Output rblue signal is same to the input 1: Output rblue signal will be the reversed signal of the input Bit[1]: bar_en 0: Output data are normal data 1: Output data are color bar data Bit[0]: sht_neg 0: Latch data at rising clock edge 1: Latch data at falling clock edge
0x84 sub address: 0x38[3:0]=4'h8	PRE CTRL01	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: bar_style Output color bar style Bit[3:0]: bar_step Output color bar step

5.3 AGC CTRL

The main purposes of the AGC_CTRL is to create some parameters used in other modules, automatically, according to AGC gain.

table 5-3 AGC CTRL registers

address	register name	default value	R/W	description
0x85	AGC OFFSET	0x00	RW	Bit[7:0]: Offset for dsn_th auto value
0x86	AGC BASE1	0x1E	RW	Bit[7:5]: Reserved Bit[4:0]: base1 for y_edge_mt auto value
0x87	AGC BASE2	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: base2 for y_edge_mt auto value. It plays its role with base1. It must be less than base1.
0x88	AGC CTRL	0x00	RW	Bit[7]: Reserved Bit[6]: gain_sel_en 0: Gain range will be max. value 1: Gain range will be the result of gain_sel Bit[5:4]: gain_sel Decides the range of gain which is used to calculate the DNS threshold. the gain range is the result of 2^(gain_sel+3). Bit[3:2]: dns_th_sel Decides the gain which is used to calculate the DNS threshold. New gain is the result of gain dividing by 2^dns_th_sel. Bit[1:0]: edge_mt_range Decides the value which is used to calculate the edge enhancement.

5.4 lens correction (LENC)

The main purpose of the Lens Correction (LENC) function is to compensate for lens imperfection. According to the radius of each pixel to the lens, the module calculates a gain for the pixel, correcting each pixel with its gain calculated to compensate for the light distribution due to lens curvature.

table 5-4 LENC registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x85	AGC OFFSET	0x00	RW	Bit[7:0]: Offset for dsn_th auto value
0x80	ISP CTRL00	1'b1	RW	Bit[1]: LENC_en 0: Disable LENC 1: Enable LENC
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	1'b1 1'b0	RW	Bit[4]: LENC_bias_on 0: LENC bias is 0 1: LENC bias is the LENC offset Bit[0]: LENC_off_man_en 0: LENC offset is the BLC 1: LENC offset is manual offset
0x84 sub address: 0x38[3:0]=4'h2	LENC OFF MAN	0x00	RW	Bit[7:0]: LENC_off_man Manual offset for LENC
0x89	LENC CTRL	0x30	RW	Bit[7:6]: Reserved Bit[5]: LENC_bias_plus 0: LENC bias will be not added back to LENC corrected data. 1: LENC bias will be added back to LENC corrected data. Bit[4]: rnd_en 0: Disable data round 1: Enable data round Bit[3:2]: v_skip Vertical skipand its skip step is 2^(the number set in v_skip) Bit[1:0]: h_skip Horizontal skip and its skip step is 2^(the number set in h_skip)

table 5-4 LENC registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x8A	LENC RED X0	0x40	RW	Bit[7:0]: red_x0[7:0] red_x0 is horizontal center position in red color channels, it should be fixed as the horizontal position of image which come from the middle of lens, so it is usually set as the horizontal position of middle pixel of each image. Range from 0 to 639. see **LENC RED XY0**[1:0] (**0x8C**)
0x8B	LENC RED Y0	0xF0	RW	Bit[7:0]: red_y0[7:0] red_y0 is vertical center position in red color channels, it should be fixed as the vertical position of image which come from the middle of lens, so it is usually set as the vertical position of middle pixel of each image. Range from 0 to 639. see **LENC RED XY0**[4] (**0x8C**)
0x8C	LENC RED XY0	0x01	RW	Bit[7:5]: Reserved Bit[4]: red_y0[8] see **LENC RED Y0**[7:0] (**0x8A**) Bit[1:0]: red_x0[9:8] see **LENC RED Y0**[7:0] (**0x8B**)
0x8D	LENC RED A1	0x22	RW	Bit[7]: Reserved Bit[6:0]: red_a1 The parameter construct the first group of factors used in LENC correction in red color channels.
0x8E	LENC RED B1	0xC2	RW	Bit[7:0]: red_b1 LENC correction in red color channels.

table 5-4 LENC registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x8F	LENC RED AB2	0x87	RW	Bit[7:4]: red_b2 The parameter construct the second group of factors used in LENC correction in red color channels. Bit[3:0]: red_a2 The parameter construct the first group of factors used in LENC correction in red color channels.
0x90	LENC GRN X0	0x40	RW	Bit[7:0]: grn_x0[7:0] grn_x0 is horizontal center position in green color channels, it should be fixed as the horizontalposition of image which come from the middle of lens, so it is usually set as the horizontal position of middle pixel of each image. Range from 0 to 639. see **LENC GRN XY0**[1:0] (**0x92**)
0x91	LENC GRN Y0	0xF0	RW	Bit[7:0]: grn_y0[7:0] grn_y0 is vertical center position in green color channels, it should be fixed as the vertical position of image which come from the middle of lens, so it is usually set as the vertical position of middle pixel of each image. Range from 0 to 639. see **LENC GRN XY0**[4] (**0x92**)
0x92	LENC GRN XY0	0x01	RW	Bit[7:5]: Reserved Bit[4]: grn_y0[8] see **LENC GRN Y0**[7:0] (**0x91**) Bit[1:0]: grn_x0[9:8] see **LENC GRN X0**[7:0] (**0x90**)
0x93	LENC GRN A1	0x22	RW	Bit[7]: Reserved Bit[6:0]: grn_a1 The parameter construct the first group of factors used in LENC correction in green color channels.
0x94	LENC GRN B1	0xC2	RW	Bit[7:0]: grn_b1 LENC correction in green color channels.

table 5-4 LENC registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x95	LENC GRN AB2	0x87	RW	Bit[7:4]: grn_b2 The parameter construct the second group of factors used in LENC correction in green color channels. Bit[3:0]: grn_a2 The parameter construct the first group of factors used in LENC correction in green color channels.
0x96	LENC BLUE X0	0x40	RW	Bit[7:0]: blu_x0[7:0] blu_x0 is horizontal center position in blue color channels, it should be fixed as the horizontalposition of image which come from the middle of lens, so it is usually set as the horizontal position of middle pixel of each image. Range from 0 to 639. see **LENC BLUE XY0**[1:0] (**0x98**)
0x97	LENC BLUE Y0	0xF0	RW	Bit[7:0]: blu_y0[7:0] blu_y0 is vertical center position in blue color channels, it should be fixed as the vertical position of image which come from the middle of lens, so it is usually set as the vertical position of middle pixel of each image. Range from 0 to 639. see **LENC BLUE XY0**[4] (**0x98**)
0x98	LENC BLUE XY0	0x01	RW	Bit[7:5]: Reserved Bit[4]: blu_y0[8] see **LENC BLUE Y0**[7:0] (**0x97**) Bit[3:2]: Reserved Bit[1:0]: blu_x0[9:8] see **LENC BLUE X0**[1:0] (**0x96**)

table 5-4 LENC registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x99	LENC BLUE A1	0x22	RW	Bit[7]: Reserved Bit[6:0]: blu_a1 The parameter construct the first group of factors used in LENC correction in blue color channels.
0x9A	LENC BLUE B1	0xC2	RW	Bit[7:0]: blu_b1 LENC correction in blue color channels.
0x9B	LENC BLUE AB2	0x87	RW	Bit[7:4]: blu_b2 The parameter construct the second group of factors used in LENC correction in blue color channels. Bit[3:0]: blu_a2 The parameter construct the first group of factors used in LENC correction in blue color channels.

5.5 gamma (GMA)

The main purpose of Gamma (GMA) is to compensate the non-linear of sensor. GMA converts the pixel values according to the Gamma curve to compensate the sensor output in different light strength.

The non-linear gamma curve is approximately constructed with different linear function.

table 5-5 GMA registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x83	ISP CTRL03	1'b1	RW	Bit[0]: s2p_first_rblue 0: First line of s2p is GR line 1: First line of s2p is BG line
0x80	ISP CTRL00	1'b1	RW	Bit[3]: gamma_en 0: Disable gamma 1: Enable gamma
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	1'b1 1'b0	RW	Bit[6]: gma_bias_on 0: Gamma bias is 0 1: Gamma bias is the gamma offset Bit[2]: gma_off_man_en 0: Gamma offset is the BLC 1: Ganma offset is manual offset
0x84 sub address: 0x38[3:0]=4'h4	GMA OFF MAN	0x00	RW	Bit[7:0]: gma_off_man Manual offset for LENC
0x9C	GMA YST01	0x0E	RW	Bit[7:0]: YST1 y-coordinate of pixels in the gamma curve
0x9D	GMA YST02	0x1A	RW	Bit[7:0]: YST2 y-coordinate of pixels in the gamma curve
0x9E	GMA YST03	0x31	RW	Bit[7:0]: YST3 y-coordinate of pixels in the gamma curve
0x9F	GMA YST04	0x5A	RW	Bit[7:0]: YST4 y-coordinate of pixels in the gamma curve
0xA0	GMA YST05	0x69	RW	Bit[7:0]: YST5 y-coordinate of pixels in the gamma curve

table 5-5 GMA registers (sheet 2 of 2)

address	register name	default value	R/W	description
0xA1	GMA YST06	0x75	RW	Bit[7:0]: YST6 y-coordinate of pixels in the gamma curve
0xA2	GMA YST07	0x7E	RW	Bit[7:0]: YST7 y-coordinate of pixels in the gamma curve
0xA3	GMA YST08	0x88	RW	Bit[7:0]: YST8 y-coordinate of pixels in the gamma curve
0xA4	GMA YST09	0x8F	RW	Bit[7:0]: YST9 y-coordinate of pixels in the gamma curve
0xA5	GMA YST10	0x96	RW	Bit[7:0]: YST10 y-coordinate of pixels in the gamma curve
0xA6	GMA YST11	0xA3	RW	Bit[7:0]: YST11 y-coordinate of pixels in the gamma curve
0xA7	GMA YST12	0xAF	RW	Bit[7:0]: YST12 y-coordinate of pixels in the gamma curve
0xA8	GMA YST13	0xC4	RW	Bit[7:0]: YST13 y-coordinate of pixels in the gamma curve
0xA9	GMA YST14	0xD7	RW	Bit[7:0]: YST14 y-coordinate of pixels in the gamma curve
0xAA	GMA YST15	0xE8	RW	Bit[7:0]: YST15 y-coordinate of pixels in the gamma curve
0xAB	GMA YSLP	0x20	RW	Bit[7:0]: YSLP15 Slope's slope of pixels in the gamma curve when its x-coordinate is 1.0

5.6 auto white balance (AWB)

The main purpose of Auto White Balance (AWB) is to make auto white balance correction.

table 5-6 AWB registers

address	register name	default value	R/W	description
0x80	ISP CTRL00	1'b1 1'b1	RW	Bit[4]: awb_c_en 0: Disable AWB 1: Enable AWB Bit[2]: awb_gain_en 0: Disable AWB gain 1: Enable AWB gain
0x83~0x84	RSVD	–	–	Reserved
0x84 sub address: 0x38[3:0]=4'h3	AWB OFF MAN	0x00	RW	Bit[7:0]: awb_off_man Manual offset for AWB
0xAC~0xC2	RSVD	–	–	Reserved

5.7 white black pixel cancellation (WBC)

The main purpose of white/black pixel cancellation (WBC) is removing white/black pixels effect.

table 5-7 WBC registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x80	ISP CTRL00	1'b1 1'b1	RW	Bit[6]: Black_en 0: Disable black pixel correction 1: Enable black pixel correction Bit[5]: white_en 0: Disable white pixel correction 1: Enable white pixel correction
0x84 sub address: 0x38[3:0]=4'h0	BIST CTRL	1'b0	RW	Bit[1]: pwrdn_wbc When it is set, WBC SRAM will be reset
0xC3	WBC CTRL00	0x1E	RW	Bit[7]: Reserved Bit[6]: Reserved Bit[5]: mirror_man Manual mirror setting: 0: No mirror mode 1: Mirror mode Bit[4]: sc_en Enable same channel detection Bit[3]: dc_en Enable different channel detection Bit[1]: detail_en Enable detail detection method Bit[0]: man_en Manual mode
0xC4	WBC CTRL01	0x03	RW	Bit[7]: Reserved Bit[6:4]: gain[10:8] Manual AGC gain setting for WBC, see **WBC GAIN MAN**[7:0] (**0xC5**) Bit[3]: gain_man_en 0: Use the real AGC gain in WBC 1: Use manual AGC gain in WBC Bit[2:0]: shift Right shift for gain value

table 5-7 WBC registers (sheet 2 of 2)

address	register name	default value	R/W	description
0xC5	WBC GAIN MAN	0x10	RW	Bit[7:0]: gain[7:0] Manual AGC gain setting for WBC, see **WBC CTRL01**[6:4] (**0xC4**)
0xC6	WBC WHITE THRESHOLD	0x08	RW	Bit[7]: Reserved Bit[6:0]: wthre Threshold value for detecting white pixel
0xC7	WBC BLACK THRESHOLD	0x10	RW	Bit[7:0]: bthre Threshold value for detecting black pixel
0xC8	WBC RECOV THRESHOLD	0x0C	RW	Bit[7:0]: thre Threshold value used in recovery
0xC9	WBC S THRESHOLD	0x08	RW	Bit[7]: Reserved Bit[6:0]: sthre
0xCA	WBC CTRL02	0x6F	RW	Bit[7:5]: gainbd_pwr Set gainbd_times as 2^gainbd_pwr Bit[4:2]: refgain_pwr Set refgain_times as 2^refgain_pwr Bit[1:0]: bd_sel Boundary select options

5.8 color interpolation (CIP)

The main purposes of the CIP module includes:

- de-noise RAW data
- interpolate RAW data to RGB data
- edge enhancement

There are two methods to set some parameters: auto and manual mode. This module can output RGB data and de-noised RAW data. Setting the register **0xCC** Bit[6:5] to 0 will enable auto mode.

table 5-8 CIP registers

address	register name	default value	R/W	description
0x81	ISP CTRL01	1'b1	RW	Bit[0]: cip_en 0: Disable CIP 1: Enable CIP
0x84 sub address: 0x38[3:0]=4'h0	BIST CTRL	1'b0	RW	Bit[2]: pwrdn_cip When it is set, CIP SRAM will be reset
0xCB	CIP DNS THRESH MAN	0x08	RW	Bit[7:0]: dns_th_man Manual setting for de-noise
0xCC	CIP CTRL	0x04	RW	Bit[7]: Reserved Bit[6]: edge_mt_man_en Manual mode for edge enhancement setting Bit[5]: dns_th_man_en Manual mode for de-noise setting Bit[4:0]: y_edge_mt_man Manual setting for edge enhancement
0xCD	CIP EDGE THRESHOLD	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: y_edge_th Edge enhancement threshold

5.9 color matrix (CMX)

The main purpose of color matrix (CMX) is converting the image from RGB domain to YUV domain. For different color temperature, the parameters in the transmitting function will be changed.

table 5-9 CMX registers

address	register name	default value	R/W	description
0x81	ISP CTRL01	1'b1	RW	Bit[1]: cmx_en 0: Disable CMX 1: Enable CMX
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	1'b1 1'b0	RW	Bit[7]: cmx_bias_on 0: CMX bias is 0 1: CMX bias is the CMX offset Bit[3]: cmx_off_man_en 0: CMX offset is the BLC 1: CMX offset is manual offset
0x84 sub address: 0x38[3:0]=4'h5	CMX OFF MAN	0x00	RW	Bit[7:0]: cmx_off_man Manual offset for LENC
0xCE	CMX M1	0x41	RW	Bit[7:0]: cmx_m1 Absolute value setting for color matrix to calculate V
0xCF	CMX M2	0x3C	RW	Bit[7:0]: cmx_m2 Absolute value setting for color matrix to calculate V
0xD0	CMX M3	0x06	RW	Bit[7:0]: cmx_m3 Absolute value setting for color matrix to calculate V
0xD1	CMX M4	0x17	RW	Bit[7:0]: cmx_m4 Absolute value setting for color matrix to calculate U
0xD2	CMX M5	0x3A	RW	Bit[7:0]: cmx_m5 Absolute value setting for color matrix to calculate U
0xD3	CMX M6	0x52	RW	Bit[7:0]: cmx_m6 Absolute value setting for color matrix to calculate U
0xD4	CMX CTRL	0x5E	RW	Bit[6]: cmx_db Bit[5:0]: cmx_sign Sign for **CMX M1** (**0xCE**) to **CMX M6** (**0xD3**)

5.10 WINC

The main purposes of the WINC module is to make the image sizes to be real sizes by remove offsets.

table 5-10 WINC registers

address	register name	default value	R/W	description
0x82	ISP CTRL02	1'b1	RW	Bit[1]: winc_en 0: Disable window cropping 1: Enable window cropping
0x83	ISP CTRL03	1'b0	RW	Bit[2]: raw_aft_cip 0: Output raw data are from WBC 1: Output raw data are the CIP output raw data

5.11 SCALE_H

The main purposes of the SCALE_H module is to realize horizontal zoom-out function. If do horizontal sub-sample and output YUV422, the SCALE_H will be set to 1 automatically.

table 5-11 SCALE_H registers

address	register name	default value	R/W	description
0x82	ISP CTRL02	1'b0	RW	Bit[2]: scale_h_en_reg 0: Disable horizontal scale 1: Enable horizontal scale
0xD7	SCALEH XSC MAN	0x00	RW	Bit[7:0]: xsc_man[7:0] Manual value of horizontal scale coefficient, see 0xD8[2:0] also
0xD8	SCALEH CTRL	0x04	RW	Bit[7]: h_drop 0: Average mode for DCW 1: Drop mode for DCW Bit[6]: scale_man 0: Auto mode 1: Manual mode Bit[5:4]: h_div_man Manual div value Bit[3]: h_round Bit[2:0]: xsc_man[10:8] see **SCALEH XSC MAN**[7:0] (**0xD7**)

5.12 YUV444TO422

The main purposes of the YUV444TO422 module is to transform YUV444 format to YUV422 format.

table 5-12 YUV444TO422 registers

address	register name	default value	R/W	description
0x81	ISP CTRL01	1'b1	RW	Bit[3]: yuv422_en 0: Disable yuv444to422 1: Enable yuv444to422
0xD9	YUV422 CTRL	0x00	RW	Bit[7:2]: Reserved Bit[1]: v_first 0: Output line will be yuyv... 1: Output line will be yvyu... (It will affect definition of u/v in SDE. If it is set, all registers in SDE about u/v must be swapped.) Bit[0]: cnv_opt 0: Average mode 1: Drop mode

5.13 special digital effects (SDE)

The main purpose of Special Digital Effects (SDE) is making special digital effect such as hue/saturation etc.

Use SDE_Ctrl to get some special effect of image. Calculate the new U and V from Hue Cos, Hue Sin, and sign of the parameters, or fix the U and V values; Saturate the U and V according to the Sat_u and Sat_v; calculate the Y from Y offset, Y gain, and Y bright, or set the Y value; invert the Y U V values to get a negative image; fixed U and V to 128 (8bit data) resulting in gray image.

table 5-13 SDE registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x81	ISP CTRL01	1'b1	RW	Bit[5]: sde_en 0: Disable SDE 1: Enable SDE
0xDA	SDE CTRL	0x00	RW	Bit[7]: fixy_en When it is set, the output Y will be a fixed value. Bit[6]: neg_en 0: Disable negative color effect 1: Enable negative color effect Bit[5]: gray_en 0: Disable gray effect 1: Enable gray effect Bit[4]: fixv_en When it is set, the output V will be the value set in register **SDE VREG**[7:0] (**0xE0**) Bit[3]: fixu_en When it is set, the output U will be the value set in register **SDE UREG**[7:0] (**0xDF**) Bit[2]: cont_en 0: Disable contrast/offset /brightness 1: Enable contrast/offset/ brightness Bit[1]: sat_en 0: Disable saturation effect 1 Enable saturation effect Bit[0]: hue_en 0: Disable hue effect. 1: Enable hue effect
0xDB	SDE HUE COS	0x80	RW	Bit[7:0]: hue_cos cos value for hue effect

table 5-13 SDE registers (sheet 2 of 2)

address	register name	default value	R/W	description
0xDC	SDE HUE SIN	0x00	RW	Bit[7:0]: hue_sin sin value for hue effect
0xDD	SDE USAT	0x40	RW	Bit[7:0]: sat_u Enhancement for u value in saturation effect
0xDE	SDE VSAT	0x40	RW	Bit[7:0]: sat_v Enhancement for v value in saturation effect
0xDF	SDE UREG	0x80	RW	Bit[7:0]: u_reg U value for fixed U effect
0xE0	SDE VREG	0x80	RW	Bit[7:0]: v_reg V value for fixed V effect
0xE1	SDE YOFFSET	0x00	RW	Bit[7:0]: y_offset Y value for fixed Y effect or the offset value for contrast effect
0xE2	SDE YGAIN	0x20	RW	Bit[7:0]: y_gain Gain in contract effect
0xE3	SDE YBRIGHT	0x00	RW	Bit[7:0]: y_bright Brightness in brightness effect
0xE4	SDE SGNSET	0x06	RW	Bit[7:6]: Reserved Bit[5:0]: sgnset

5.14 SCALE_V

The main purposes of the SCALE_V module is to do vertical scale.

table 5-14 SCALE_V registers

address	register name	default value	R/W	description
0x82	ISP CTRL02	1'b0	RW	Bit[3]: scale_v_en 0: Disable vertical scale 1: Enable vertical scale
0x84 sub address: 0x38[3:0]=4'h0	BIST CTRL	1'b0	RW	Bit[3]: pwrdn_scale_v When it is set, scale_v SRAM will be reset
0xE5	SCALEV CTRL	0x0C	RW	Bit[7]: Manual_mode Bit[6:4]: drop_offset Offset for DCW drop mode Bit[3]: drop_mode Manual DCW drop mode setting Bit[2]: zoom_2ram_mode Manual ram mode setting Bit[1:0]: v_div Maunal div value for DCW

5.15 VAP

The main purposes of the VAP module is to do horizontal sub-sample when output RAW data.

table 5-15 VAP registers

address	register name	default value	R/W	description
0xE6	VAP CTRL	0x10	RW	Bit[7:5]: Reserved Bit[4]: vap_mean 0: No mean for sum 1: Mean for sum Bit[3:2]: Reserved Bit[1]: g_drop 0: Summary mode 1: Drop mode Bit[0]: br_drop 0: Summary mode 1: Drop mode

5.16 16-zone luminance average (YAVG)

The main purposes of the YAVG module includes:

- calculate Y average based on selected Y
- calculate bright pixel count and black pixel count
- support Y data

table 5-16 YAVG registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x82	ISP CTRL02	1'b1	RW	Bit[5]: yavg_en 0: Disable y average 1: Enable y average
0x83	ISP CTRL03	1'b0 1'b1	RW	Bit[4]: yavg_yuv_mode 0: yavg inputs are raw data 1: yavg inputs are y of yuv422 Bit[3]: yavg_aft_wbc 0: Inputs of yavg comes from awb_gain 1: Inputs of yavg comes from WBC
0xE9 sub address: 0x38[3:0]=4'h0	YAVG BLACK THRESHOLD	0x00	RW	Bit[7:0]: blk_thresh Threshold for blackness
0xE9 sub address: 0x38[3:0]=4'h1	YAVG BRIGHT THRESHOLD	0x00	RW	Bit[7:0]: brt_thresh Threshold for brightness
0xE9 sub address: 0x38[3:0]=4'h2	YAVG HOFF	0x00	RW	Bit[7:0]: yavg_winofh[7:0] Horizontal offset for window cropping in YAVG.
0xE9 sub address: 0x38[3:0]=4'h3	YAVG VOFF	0x00	RW	Bit[7:0]: yavg_winofv[7:0] Vertical offset for window cropping in YAVG.

table 5-16 YAVG registers (sheet 2 of 2)

address	register name	default value	R/W	description
0xE9 sub address: 0x38[3:0]=4'h4	YAVG CTRL	0x00	RW	Bit[7:6]: Reserved Bit[5]: yavg_win_man 0: Window will be the default window 1: Window will be the window set by the registers Bit[4]: yavg_winofv[8] See yavg_voff_l (0xE9, 0x38[3:0] = 4'h3) Bit[3:2]: Reserved Bit[1:0]: yavg_winofh[9:8] See yavg_hoff_l (0xE9, 0x38[3:0] = 4'h2)
0xE9 sub address: 0x38[3:0]=4'h5	YAVG HSIZE	0x00	RW	Bit[7]: Reserved Bit[6:0]: yavg_winh Horizontal size of cropping window. It will be multiplied by 8 to be real size.
0xE9 sub address: 0x38[3:0]=4'h6	YAVG VSIZE	0x00	RW	Bit[7]: Reserved Bit[6:0]: yavg_winv Vertical size of cropping window. It will be multiplied by 4 to be real size.

6 image sensor output interface digital functions

6.1 digital video port (DVP)

6.1.1 overview

The Digital Video Port (DVP) provides 10-bit parallel data output in all formats supported and extended features including HREF, CCIR656 format, HSYNC mode and test pattern output.

6.1.2 HREF mode

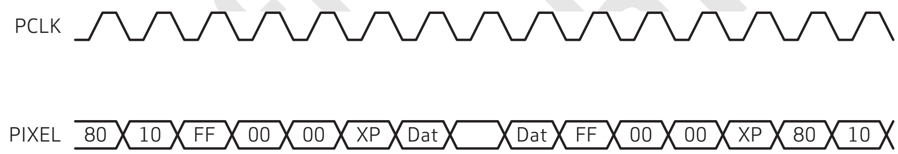
HREF mode is the default mode of the DVP. Each DVP_VSYNC indicates the starting of a new frame.

6.1.3 CCIR656 mode

The OV7740 supports standard CCIR656 mode. The sync code can be changed manually. “F” of the sync code can be switched. To set CCIR656 mode settings:

- write 0x12[5] to 1 (sets CCIR656_EN = 1)
- 0x52[3] indicates “F” of the sync code.

figure 6-1 CCIR656 timing

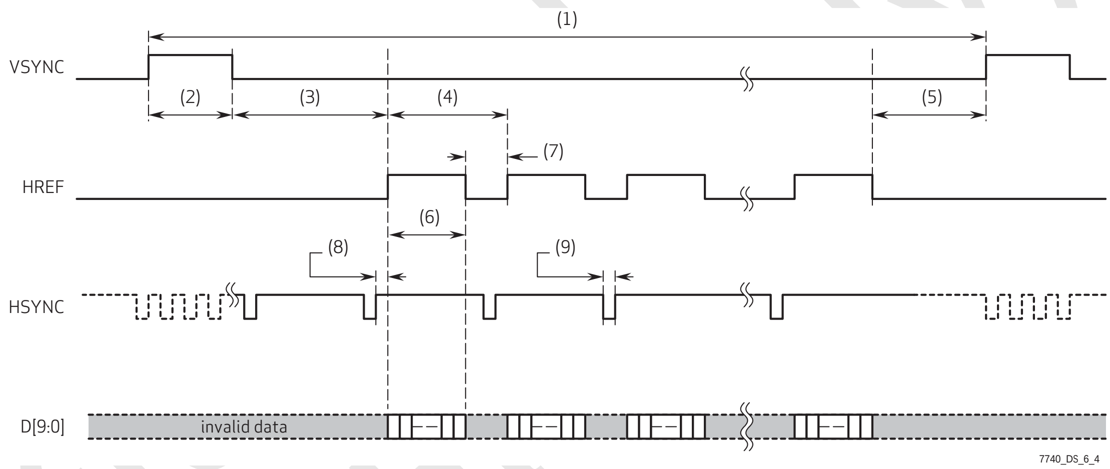


note 1	XP: {1, F, V, H, P[3:0]}	1	F	V	H	P3	P2	P1	P0	1	F	V	H	P3	P2	P1	P0
	F: 0 for field 1; 1 for field 2	1	0	0	0	0	0	0	0	1	1	0	0	0	1	1	1
	V: 0 for all else; 1 for field blanking	1	0	0	1	1	1	0	1	1	1	0	1	1	0	1	0
	H: 0 for SAV; 1 for EAV	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	0
	P[3:0]: protect bits	1	0	1	1	0	1	1	0	1	1	1	1	0	0	0	1

7740_DS_6_3

6.1.4 DVP timing

figure 6-2 DVP timing diagram



> **note** The timing values shown in **table 6-1** may vary depending upon register settings.

table 6-1 DVP timing specifications

mode	timing
VGA 640x480	(1) 399168 = 504 lines (2) 3168 (4 lines) (3) 9674 (4) 792 (5) 6318 (6) 640 (7) 152 (8) 106 (9) 48
QVGA 320x240	(1) 199584 = 252 lines (2) 1584 (2 lines) (3) 6882 (4) 792 (5) 1508 (6) 320 (7) 472 (8) 200 (9) 48

table 6-2 DVP control registers

address	register name	default value	R/W	description
0x12	REG12	0x11	RW	Bit[5]: CCIR656 enable
0x28	REG28	0x00	RW	Bit[7]: Output data bit reverse option. Bit[6]: HREF pin output swap 0: HREF 1: HSYNC Bit[5]: HSYNC polarity 0: Positive 1: Negative Bit[4]: HREF polarity 0: Output positive HREF 1: Output negative HREF for data valid Bit[3]: No VSYNC output option. 0: Still output VSYNC when frame drop 1: No VSYNC output when frame drop Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative
0x0C	REG0C	0x02	RW	Bit[4]: YUV output, Y <-> UV swap 0: YUYVYUYV 1: UYVYUYVY Bit[3]: Output data high 8-bit MSB and LSB swap 0: Output [DATA9,DATA8…DATA3, DATA2,DATA1,DATA0] 1: Output [DATA2,DATA3…DATA8, DATA9,DATA1,DATA0]
0x65	REG65	0x00	RW	Bit[3]: Output data bit swap option 0: Output DATA[9:0] 1: Output DATA[0:9]

7 register tables

The following tables provide descriptions of the device control registers contained in the OV7740. For all register Enable/Disable bits, Enable = 1 and Disable = 0. The device slave addresses are 0x42 for write and 0x43 for read.

table 7-1 system control registers (sheet 1 of 25)

address	register name	default value	R/W	description
0x00	GAIN	0x00	RW	AGC Gain Control LSBs (MSBs in REG15[1:0] (**0x15**)) Bit[7:0]: Analog gain
0x01	BGAIN	0x40	RW	B Channel Gain
0x02	RGAIN	0x40	RW	R Channel Gain
0x03	GGAIN	0x40	RW	G Channel Gain
0x04	RSVD	–	–	Reserved
0x05	BAVG	0x00	RW	B Channel Average
0x06	GAVG	0x00	RW	G Channel Average
0x07	RAVG	0x00	RW	R Channel Average
0x08~ 0x09	RSVD	–	–	Reserved
0x0A	PIDH	0x77	R	Product ID Number MSB (Read only)
0x0B	PIDL	0x40	R	Product ID Number LSB (Read only)
0x0C	REG0C	0x02	RW	Bit[7]: Vertical flip Bit[6]: Mirror Bit[5]: Reserved Bit[4]: YUV output, Y ↔ UV swap 0: YUYVYUYV 1: UYVYUYVY Bit[3]: High 8-bit MSB and LSB swap 0: Output [Y9,Y8…Y3,Y2,Y1,Y0] 1: Output [Y2,Y3…Y8,Y9,Y1,Y0] Bit[2:1]: Max exposure = frame length – limit*2 Bit[0]: Array color bar
0x0D	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 2 of 25)

address	register name	default value	R/W	description
0x0E	REG0E	0xE0		Bit[7]: BLC line selection 0: Electrical BLC. 1: Optical BLC. Bit[6:5]: BLC line selection 00 Select both blue line and red line as BLC line. 01: Only select red line as BLC line. 10: Only select blue line as BLC line. 11: Select both blue line and red line as BLC line. Bit[4]: Reserved Bit[3]: Sleep mode Bit[2:0]: Reserved
0x0F	HAEC	0x00	RW	Automatic Exposure Control Bit[15:8] (LSBs in AEC[7:0] (**0x10**))
0x10	AEC	0xF0	RW	Automatic Exposure Control Bit [7:0] (MSBs in HAEC[7:0] (**0x0F**))
0x11	CLK	0x00	RW	Bit[7:6]: Reserved Bit[5:0]: Clock divider CLK = XVCLK1/(decimal value of CLK[5:0] + 1)
0x12	REG12	0x11	RW	Bit[7]: Soft Reset 0: Reserved 1: Initiate system reset. All registers are set to factory default value after which the chip resumes normal operation. Bit[6]: Vertical skip mode Bit[5]: CC656 mode Bit[4:2]: Reserved Bit[0]: Output raw data RGB mode

table 7-1 system control registers (sheet 3 of 25)

address	register name	default value	R/W	description
0x13	REG13	0x87	RW	Bit[7]: AEC speed selection 0: Normal 1: Faster AEC correction Bit[6]: Enable frame drop function Bit[5]: Banding filter ON/OFF selection Bit[4]: Enable AEC below banding value Bit[3]: Tp level exposure ON/OFF selection Bit[2]: AGC auto/manual control selection Bit[1]: Auto white balance control selection Bit[0]: Exposure auto/manual control selection
0x14	REG14	0x30	RW	Bit[7]: Reserved Bit[6:4]: AGC gain ceiling 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x Bit[3:0]: Reserved
0x15	REG15	0x00	RW	Bit[7]: Enable inserting frames in night mode Bit[6:4]: Ceiling of inserting frames Bit[3:2]: Reserved Bit[1:0]: AGC MSBs (digital gain) (LSBs in GAIN[7:0] (**0x00**))
0x16	REG16	0x00	RW	Bit[7:6]: Reserved Bit[5]: Sensor vertical output size 1 LSBs Bit[4:3]: Sensor horizontal output size 2 LSB Bit[2]: Sensor vertical output start point 1 LSB Bit[1]: Sensor horizontal output start point 2 LSBs
0x17	AHSTART	0x2A	RW	Sensor Horizontal Output Start Point 8 MSBs (LSBs in REG16[1:0] (**0x16**))
0x18	AHSIZE	0xA0	RW	Sensor Horizontal Output size 8 MSBs (LSBs in REG16[4:3] (**0x16**))
0x19	AVSTART	0x05	RW	Sensor Vertical Output Start Point 8 MSBs (LSBs in REG16[2] (**0x16**))

table 7-1 system control registers (sheet 4 of 25)

address	register name	default value	R/W	description
0x1A	AVSIZE	0xF0	RW	Sensor Vertical Output size MSBs (LSB in REG16[5] (**0x16**))
0x1B	PSHFT	0x80	RW	Pixel Shift
0x1C	MIDH	0x7F	R	Manufacturer ID Byte - High
0x1D	MIDL	0xA2	R	Manufacturer ID Byte - Low
0x1E	REG1E	0x11	RW	Bit[7:1]: Reserved Bit[0]: AEC step control 0: AEC max increasing step less than vertical black 1: AEC max increasing step has no limit
0x1F	REG1F	0x00		LSBs of tp level exposure control when exposure is less than one line. (MSBs in REG30 (**0x30**))
0x20~ 0x23	RSVD	–	–	Reserved
0x24	WPT	0x78	RW	Luminance Signal High Range for AEC/AGC Operation
0x25	BPT	0x68	RW	Luminance Signal Low Range for AEC/AGC Operation
0x26	VPT	0xD4	RW	Effective only AEC/AGC fast mode
0x27	REG27	0x00	RW	Bit[7]: Black sun cancellation enable Bit[6:0]: Reserved

table 7-1 system control registers (sheet 5 of 25)

address	register name	default value	R/W	description
0x28	REG28	0x00	RW	Bit[7]: Output data bit reverse option Bit[6]: HREF pin output swap 0: HREF 1: HSYNC Bit[5]: HSYNC polarity 0: Positive 1: Negative Bit[4]: HREF polarity 0: Output positive HREF 1: Output negative HREF for data valid Bit[3]: No VSYNC output option 0: Still output VSYNC when frame drop 1: No VSYNC output when frame drop Bit[2]: Reserved Bit[1]: VSYNC polarity 0: Positive 1: Negative Bit[0]: Reserved
0x29	REG29	0x18	RW	Horizontal tp Counter End Point LSBs
0x2A	REG2A	0x03	RW	Horizontal tp Counter End Point MSBs
0x2B	REG2B	0xF8	RW	Row Counter End Point LSBs
0x2C	REG2C	0x01	RW	Row Counter End Point MSBs
0x2D	REG2D	0x00	RW	Automatically Inserted Dummy Lines in Night Mode LSBs
0x2E	REG2E	0x00	RW	Automatically Inserted Dummy Lines in Night Mode MSBs
0x2F	YAVG	0x00	RW	Luminance Average Value
0x30	REG30	0x00	RW	MSBs of tp Level Exposure Control when exposure is less than one line. (LSBs in REG1F **0x1F**)
0x31	HOUTSIZE	0xA0	RW	DSP H output size 8MSB H output size = {HOUTSIZE[7:0] (**0x31**), REG34[2:1] (**0x34**)}
0x32	VOUTSIZE	0xF0	RW	DSP V output size 8MSB V output size = {VOUTSIZE[7:0] (**0x32**), REG34[0] (**0x34**)}
0x33	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 6 of 25)

address	register name	default value	R/W	description
0x34	REG34	0x00	RW	Bit[7:3]: Reserved Bit[2]: DSP H output size 2 LSBs Bit[0]: DSP V output size 1 LSB
0x35~ 0x37	RSVD	–	–	Reserved
0x38	REG38	0x10	RW	BIT[7:4]: Reserved Bit[3:0]: Monitor[3:0] I2C registers sub-address control bits
0x39~0x4F	RSVD	–	–	Reserved
0x50	REG50	0x2E	RW	LSBs of Banding Starting Step for 50 Hz light source (MSBs in REG52[5:4] (**0x52**))
0x51	REG51	0xFC	RW	LSBs of Banding Starting Step for 60 Hz light source (MSBs in REG52[7:6] (**0x52**))
0x52	REG52	0x10	RW	Bit[7:6]: MSBs of banding starting step for 60 Hz light source (LSBs in REG51 (**0x51**)) Bit[5:4]: MSBs of banding starting step for 50 Hz light source (LSBs in REG50 (**0x50**)) Bit[3:0]: Reserved
0x53~ 0x55	RSVD	–	–	Reserved
0x56	REG56	0xFF	RW	16-zone Y Average Select (for long exposure in HDR) In each zone: 00: Not selected 01: Weight x1 10: Weight x2 11: Weight x4 Bit[7:6]: Zone 4 Bit[5:4]: Zone 3 Bit[3:2]: Zone 2 Bit[1:0]: Zone 1
0x57		0xFF	RW	In each zone: 00: Not selected 01: Weight x1 10: Weight x2 11: Weight x4 Bit[7:6]: Zone 8 Bit[5:4]: Zone 7 Bit[3:2]: Zone 6 Bit[1:0]: Zone 5

table 7-1 system control registers (sheet 7 of 25)

address	register name	default value	R/W	description
0x58		0xFF	RW	In each zone: 00: Not selected 01: Weight x1 10: Weight x2 11: Weight x4 Bit[7:6]: Zone 12 Bit[5:4]: Zone 11 Bit[3:2]: Zone 10 Bit[1:0]: Zone 9
0x59		0xFF	RW	In each zone: 00: Not selected 01: Weight x1 10: Weight x2 11: Weight x4 Bit[7:6]: Zone 16 Bit[5:4]: Zone 15 Bit[3:2]: Zone 14 Bit[1:0]: Zone 13
0x5A~ 0x62	RSVD	–	–	Reserved
0x63		0x00	RW	Luminance Average Value of one zone. This zone was selected by Monitor[3:0] in REG37[3:0] (**0x38**)
0x64	RSVD	–	–	Reserved
0x65		0x00	RW	Bit[7:4]: Reserved Bit[3]: Output data bit swap option 0: Output DATA[9:0] 1: Output DATA[0:9] Bit[2]: Reserved Bit[1]: GPIO register for pin HREF Bit[0]: GPIO register for pin VSYNC
0x66		0x00	RW	AWB Bias
0x67		0x80	RW	Bit[7:6]: Reserved Bit[5:0]: BLC target
0x68	RSVD	–	–	Reserved
0x69		0x00	RW	Bit[7:4]: Reserved Bit[3]: MBLC When setting this bit to 1, auto BLC will be initiated for 64 frames Bit[2:0]: Reserved
0x6A		0x00	RW	LSBs of BLC Offsets for Gr Channel

table 7-1 system control registers (sheet 8 of 25)

address	register name	default value	R/W	description
0x6B		0x00	RW	LSBs of BLC Offsets for Gb Channel
0x6C		0x00	RW	LSBs of BLC Offsets for R Channel
0x6D		0x00	RW	LSBs of BLC Offsets for B Channel
0x6E		0x00	RW	Bit[7:6]: MSBs of BLC offsets for Gr channel Bit[5:4]: MSBs of BLC offsets for Gb channel Bit[3:2]: MSBs of BLC offsets for R channel Bit[1:0]: MSBs of BLC offsets for B channel
0x6F~ 0x7F	RSVD	–	–	Reserved
0x80	ISP CTRL00	0x7F	RW	Bit[7]: Reserved Bit[6]: black_en 0: Disable black pixel correction 1: Enable black pixel correction Bit[5]: white_en 0: Disable white pixel correction 1: Enable white pixel correction Bit[4]: awb_c_en 0: Disable AWB 1: Enable AWB Bit[3]: gamma_en 0: Disable gamma 1: Enable gamma Bit[2]: awb_gain_en 0: Disable AWB gain 1: Enable AWB gain Bit[1]: lenc_en 0: Disable LENC 1: Enable LENC Bit[0]: isp_en 0: Disable ISP 1: Enable ISP

table 7-1 system control registers (sheet 9 of 25)

address	register name	default value	R/W	description
0x81	ISP CTRL01	0x3F	RW	Bit[7:6]: Reserved Bit[5]: sde_en 0: Disable SDE 1: Enable SDE Bit[4]: uv_adj_en 0: Disable UV adjust 1: Enable UV adjust Bit[3]: yuv422_en 0: Disable yuv444to422 1: Enable yuv444to422 Bit[2]: uv_avg_en 0: Disable uv average 1: Enable uv average Bit[1]: cmx_en 0: Disable CMX 1: Enable CMX Bit[0]: cip_en 0: Disable CIP 1: Enable CIP
0x82	ISP CTRL02	0x32	RW	Bit[7:6]: Reserved Bit[5]: yavg_en 0: Disable y average 1: Enable y average Bit[4] : fifo_en 0: Disable FIFO 1: Enable FIFO Bit[3] : scale_v_en 0: Disable vertical scale 1: Enable vertical scale Bit[2] : scale_h_en_reg 0: Disable horizontal scale 1: Enable horizontal scale Bit[1] : winc_en 0: Disable window cropping 1: Enable window cropping Bit[0]: smthscale_en 0: Disable smooth scale 1: Enable smooth scale

table 7-1 system control registers (sheet 10 of 25)

address	register name	default value	R/W	description
0x83	ISP CTRL03	0x09	RW	Bit[7:6]: Reserved Bit[5]: video_off 0: Normal outputs 1: No outputs Bit[4]: yavg_yuv_mode 0: yavg inputs are raw data 1: yavg inputs are y of yuv422 Bit[3]: yavg_aft_wbc 0: Inputs of yavg come from awb_gain 1: Inputs of yavg come from WBC Bit[2]: raw_aft_cip 0: the output raw data are from wbc 1: the output raw data are the cip output raw data Bit[1]: awb2_aft_gma 0: Second inputs of AWB statistic are the inputs of GMA 1: Second inputs of AWB statistic are the outputs of GMA Bit[0]: s2p_fst_rblue 0: First line of s2p is GR line 1: First line of s2p is BG line

table 7-1 system control registers (sheet 11 of 25)

address	register name	default value	R/W	description
0x84 sub address: 0x38[3:0]=4'h0	BIST CTRL	0x00	RW	Bit[7:6]: Reserved Bit[5]: bist_en When set, SRAM bist will be done Bit[4]: pwrdn_fifo When set, FIFO SRAM will be reset Bit[3]: pwrdn_scale_v When set, scale_v SRAM will be reset Bit[2]: pwrdn_cip When set, CIP SRAM will be reset Bit[1]: pwrdn_wbc When set, WBC SRAM will be reset Bit[0]: pwrdn_awb When set, AWB SRAM will be reset

table 7-1 system control registers (sheet 12 of 25)

address	register name	default value	R/W	description
0x84 sub address: 0x38[3:0]=4'h1	BIAS CTRL	0xf0	RW	Bit[7]: cmx_bias_on 0: CMX bias is 0 1: CMX bias is the CMX offset Bit[6]: gma_bias_on 0: Gamma bias is 0 1: Gamma bias is the gamma offset Bit[5]: awb_bias_on 0: AWB bias is 0 1: AWB bias is the AWB offset Bit[4]: lenc_bias_on 0: LENC bias is 0 1: LENC bias is the LENC offset Bit[3]: cmx_off_man_en 0: CMX offset is the BLC 1: CMX offset is manual offset Bit[2]: gma_off_man_en 0: Gamma offset is the BLC 1: Gamma offset is manual offset Bit[1]: awb_off_man_en 0: AWB offset is the BLC 1: AWB offset is manual offset Bit[0]: lenc_off_man_en 0: LENC offset is the BLC 1: LENC offset is manual offset
0x84 sub address: 0x38[3:0]=4'h2	LENC OFF MAN	0x00	RW	lenc_off_man Manual offset for LENC
0x84 sub address: 0x38[3:0]=4'h3	AWB OFF MAN	0x00	RW	awb_off_man Manual offset for AWB
0x84 sub address: 0x38[3:0]=4'h4	GMA OFF MAN	0x00	RW	gma_off_man Manual offset for GMA
0x84 sub address: 0x38[3:0]=4'h5	CMX OFF MAN	0x00	RW	cmx_off_man Manual offset for CMX

table 7-1 system control registers (sheet 13 of 25)

address	register name	default value	R/W	description
0x84 sub address: 0x38[3:0]=4'h6	ROREG ADDR	0x00	R	isp_roreg_address Read-only registers' address
0x84 sub address: 0x38[3:0]=4'h7	PRE CTRL00	0x00	RW	Bit[7:5]: Reserved Bit[4]: bar_move When it is set, the color bar is moving color bar. Bit[3]: Reserved Bit[2]: rblue_inv When it is set, the RBlue signal will be inversed Bit[1]: bar_en 0: DSP PRE output normal data 1: DSP PRE output color bar Bit[0]: sht_neg 0: Latch data at rising clock edge 1: Latch data at falling clock edge
0x84 sub address: 0x38[3:0]=4'h8	PRE CTRL01	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: bar_style Style of the output color bar Bit[3:0]: bar_step Step of the output color bar
0x85	AGC OFFSET	0x00	RW	Bit[7:0]: Offset for dsn_th auto value
0x86	AGC BASE1	0x1E	RW	Bit[7:5]: Reserved Bit[4:0]: base1 Base1 for y_edge_mt auto value.
0x87	AGC BASE2	0x02	RW	Bit[7:5]: Reserved Bit[4:0]: base2 Base2 for y_edge_mt auto value. It plays its role with base1. It must be less than base1.

table 7-1 system control registers (sheet 14 of 25)

address	register name	default value	R/W	description
0x88	AGC CTRL	0x00	RW	Bit[7]: Reserved Bit[6]: gain_sel_en 0: Gain range will be max. value 1: Gain range will be the result of gain_sel Bit[5:4]: gain_sel To decide the range of gain which is used to calculate the DNS threshold. the gain range is the result of 2^(gain_sel+3) Bit[3:2]: dns_th_sel Decide the gain which is used to calculate the DNS threshold. New gain is the result of gain dividing by 2^dns_th_sel Bit[1:0]: edge_mt_range To decide the value which is used to calculate the edge enhancement
0x89	LENC CTRL	0x30	RW	Bit[7:6]: Reserved Bit[5]: lenc_bias_plus 0: LENC bias will be not added back to lenc-corrected data 1: LENC bias will be added back to lenc_corrected data BIt[4]: rnd_en 0: Disable data round 1: Enable data round Bit[3:2]: v_skip Vertical skip and its skip step is 2^(the number set in v_skip) Bit[1:0]: h_skip Horizontal skipand its skip step is 2^(the number set in h_skip)

table 7-1 system control registers (sheet 15 of 25)

address	register name	default value	R/W	description
0x8A	LENC RED X0	0x40	RW	Bit[7:0]: red_x0[7:0] red_x0 is horizontal center position in red color channels, it should be fixed as the horizontal position of image which come from the middle of lens, so it is usually set as the horizontal position of middle pixel of each image. Range from 0 to 639. see **LENC RED XY0**[1:0] (**0x8C**)
0x8B	LENC RED Y0	0xF0	RW	Bit[7:0]: red_y0[7:0] red_y0 is vertical center position in red color channels, it should be fixed as the vertical position of image which come from the middle of lens, so it is usually set as the vertical position of middle pixel of each image. Range from 0 to 639. see **LENC RED XY0**[4] (**0x8C**)
0x8C	LENC RED XY0	0x01	RW	Bit[7:5]: Reserved Bit[4]: red_y0[8] see **LENC RED Y0**[7:0] (**0x8A**) Bit[1:0]: red_x0[9:8] see **LENC RED Y0**[7:0] (**0x8B**)
0x8D	LENC RED A1	0x22	RW	Bit[7]: Reserved Bit[6:0]: red_a1 The parameter construct the first group of factors used in LENC correction in red color channels.
0x8E	LENC RED B1	0xC2	RW	Bit[7:0]: red_b1 LENC correction in red color channels.

table 7-1 system control registers (sheet 16 of 25)

address	register name	default value	R/W	description
0x8F	LENC RED AB2	0x87	RW	Bit[3:0]: red_a2 The parameter construct the first group of factors used in LENC correction in red color channels. Bit[7:4]: red_b2 The parameter construct the second group of factors used in LENC correction in red color channels.
0x90	LENC GRN X0	0x40	RW	Bit[7:0]: grn_x0[7:0] grn_x0 is horizontal center position in green color channels, it should be fixed as the horizontalposition of image which come from the middle of lens, so it is usually set as the horizontal position of middle pixel of each image. Range from 0 to 639. see **LENC GRN XY0**[1:0] (**0x92**)
0x91	LENC GRN Y0	0xF0	RW	Bit[7:0]: grn_y0[7:0] grn_y0 is vertical center position in green color channels, it should be fixed as the vertical position of image which come from the middle of lens, so it is usually set as the vertical position of middle pixel of each image. Range from 0 to 639. see **LENC GRN XY0**[4] (**0x92**)
0x92	LENC GRN XY0	0x01	RW	Bit[7:5]: Reserved Bit[4]: grn_y0[8] see **LENC GRN Y0**[7:0] (**0x91**) Bit[1:0]: grn_x0[9:8] see **LENC GRN X0**[7:0] (**0x90**)
0x93	LENC GRN A1	0x22	RW	Bit[7]: Reserved Bit[6:0]: grn_a1 The parameter construct the first group of factors used in LENC correction in green color channels.

table 7-1 system control registers (sheet 17 of 25)

address	register name	default value	R/W	description
0x94	LENC GRN B1	0xC2	RW	Bit[7:0]: grn_b1 LENC correction in green color channels.
0x95	LENC GRN AB2	0x87	RW	Bit[7:4]: grn_b2 The parameter construct the second group of factors used in LENC correction in green color channels. Bit[3:0]: grn_a2 The parameter construct the first group of factors used in LENC correction in green color channels.
0x96	LENC BLUE X0	0x40	RW	Bit[7:0]: blu_x0[7:0] blu_x0 is horizontal center position in blue color channels, it should be fixed as the horizontalposition of image which come from the middle of lens, so it is usually set as the horizontal position of middle pixel of each image. Range from 0 to 639. see **LENC BLUE XY0**[1:0] (**0x98**)
0x97	LENC BLUE Y0	0xF0	RW	Bit[7:0]: blu_y0[7:0] blu_y0 is vertical center position in blue color channels, it should be fixed as the vertical position of image which come from the middle of lens, so it is usually set as the vertical position of middle pixel of each image. Range from 0 to 639. see **LENC BLUE XY0**[4] (**0x98**)
0x98	LENC BLUE XY0	0x01	RW	Bit[7:5]: Reserved Bit[4]: blu_y0[8] see **LENC BLUE Y0**[7:0] (**0x97**) Bit[3:2]: Reserved Bit[1:0]: blu_x0[9:8] see **LENC BLUE X0**[1:0] (**0x96**)

table 7-1 system control registers (sheet 18 of 25)

address	register name	default value	R/W	description
0x99	LENC BLUE A1	0x22	RW	Bit[7]: Reserved Bit[6:0]: blu_a1 The parameter construct the first group of factors used in LENC correction in blue color channels.
0x9A	LENC BLUE B1	0xC2	RW	Bit[7:0]: blu_b1 LENC correction in blue color channels.
0x9B	LENC BLUE AB2	0x87	RW	Bit[7:4]: blu_b2 The parameter construct the second group of factors used in LENC correction in blue color channels. Bit[3:0]: blu_a2 The parameter construct the first group of factors used in LENC correction in blue color channels.
0x9C	GMA YST01	0x0E	RW	YST1 y-coordinate of pixels in the gamma curve
0x9D	GMA YST02	0x1A	RW	YST2 y-coordinate of pixels in the gamma curve
0x9E	GMA YST03	0x31	RW	YST3 y-coordinate of pixels in the gamma curve
0x9F	GMA YST04	0x5A	RW	YST4 y-coordinate of pixels in the gamma curve
0xA0	GMA YST05	0x69	RW	YST5 y-coordinate of pixels in the gamma curve
0xA1	GMA YST06	0x75	RW	YST6 y-coordinate of pixels in the gamma curve
0xA2	GMA YST07	0x7E	RW	YST7 y-coordinate of pixels in the gamma curve
0xA3	GMA YST08	0x88	RW	YST8 y-coordinate of pixels in the gamma curve
0xA4	GMA YST09	0x8F	RW	YST9 y-coordinate of pixels in the gamma curve
0xA5	GMA YST10	0x96	RW	YST10 y-coordinate of pixels in the gamma curve
0xA6	GMA YST11	0xA3	RW	YST11 y-coordinate of pixels in the gamma curve

table 7-1 system control registers (sheet 19 of 25)

address	register name	default value	R/W	description
0xA7	GMA YST12	0xAF	RW	YST12 y-coordinate of pixels in the gamma curve
0xA8	GMA YST13	0xC4	RW	YST13 y-coordinate of pixels in the gamma curve
0xA9	GMA YST14	0xD7	RW	YST14 y-coordinate of pixels in the gamma curve
0xAA	GMA YST15	0xE8	RW	YST15 y-coordinate of pixels in the gamma curve
0xAB	GMA YSLP	0x20	RW	YSLP15 Slope's slope of pixels in the gamma curve when its x-coordinate is 1.0
0xAC~ 0xC2	RSVD	–	–	Reserved
0xC3	WBC CTRL00	0x1E	RW	Bit[7:6]: Reserved Bit[5:0]: Mirror mode
0xC4	WBC CTRL01	0x03	RW	Bit[7]: Reserved Bit[6:4]: gain[10:8] Manual AGC gain setting for WBC, see **WBC GAIN MAN**[7:0] (**0xC5**) Bit[3]: gain_man_en 0: Use the real AGC gain in WBC 1: Use manual AGC gain in WBC Bit[2:0]: shift Right shift for gain value
0xC5	WBC GAIN MAN	0x10	RW	Bit[7:0]: gain[7:0] Manual AGC gain setting for WBC, see **WBC CTRL01**[6:4] (**0xC4**)
0xC6	WBC WHITE THRESHOLD	0x08	RW	Bit[7]: Reserved Bit[6:0]: wthre Threshold value for detecting white pixel
0xC7	WBC BLACK THRESHOLD	0x10	RW	Bit[7:0]: bthre Threshold value for detecting black pixel
0xC8	WBC RECOV THRESHOLD	0x0C	RW	Bit[7:0]: thre Threshold value used in recovery

table 7-1 system control registers (sheet 20 of 25)

address	register name	default value	R/W	description
0xC9	WBC S THRESHOLD	0x08	RW	Bit[7]: Reserved Bit[6:0]: sthre
0xCA	WBC_CTRL02	0x6F	RW	Bit[7:5]: gainbd_pwr Set gainbd_times as 2^gainbd_pwr Bit[4:2]: refgain_pwr Set refgain_times as 2^refgain_pwr Bit[1:0]: bd_sel Boundary select options
0xCB	CIP DNS THRESH MAN	0x08	RW	Bit[7:0]: dns_th_man Manual setting for de-noise
0xCC	CIP CTRL	0x04	RW	Bit[7]: Reserved Bit[6]: edge_mt_man_en Manual mode for edge enhancement setting Bit[5]: dns_th_man_en Manual mode for de-noise setting Bit[4:0]: y_edge_mt_man Manual setting for edge enhancement
0xCD	CIP EDGE THRESHOLD	0x06	RW	Bit[7:4]: Reserved Bit[3:0]: y_edge_th Edge enhancement threshold
0xCE	CMX M1	0x41	RW	cmx_m1 Absolute value setting for color matrix to calculate V
0xCF	CMX M2	0x3C	RW	cmx_m2 Absolute value setting for color matrix to calculate V
0xD0	CMX M3	0x06	RW	cmx_m3 Absolute value setting for color matrix to calculate V
0xD1	CMX M4	0x17	RW	cmx_m4 Absolute value setting for color matrix to calculate U
0xD2	CMX M5	0x3A	RW	cmx_m5 Absolute value setting for color matrix to calculate U
0xD3	CMX M6	0x52	RW	cmx_m6 Absolute value setting for color matrix to calculate U

table 7-1 system control registers (sheet 21 of 25)

address	register name	default value	R/W	description
0xD4	CMX CTRL	0x5E	RW	Bit[6]: cmx_db Bit[5:0]: cmx_sign Sign for **CMX M1** (**0xCE**) to **CMX M6** (**0xD3**)
0xD5	SCALE SMTH CTRL	0x10	RW	Bit[7:6]: Reserved Bit[5]: scale_size_restart When it is set, restart the smooth scale procedure if size setting is changed Bit[4]: scale_zoom_mode 0: Zoom in mode 1: Zoom out mode Bit[2:0]: scale_step_num To decide how many steps to do smooth scale. The larger the value is set, the slower the smooth scale moves
0xD6	RSVD	–	–	Reserved
0xD7	SCALEH XSC MAN	0x00	RW	Bit[7:0]: xsc_man[7:0] Manual value of horizontal scale coefficient, see 0xD8[2:0] also
0xD8	SCALEH CTRL	0x04	RW	Bit[7]: h_drop 0: Average mode for DCW 1: Drop mode for DCW Bit[6]: scale_man 0: Auto mode 1: Manual mode Bit[5:4]: h_div_man Manual div value Bit[3]: h_round Bit[2:0]: xsc_man[10:8] see **SCALEH XSC MAN**[7:0] (**0xD7**)
0xD9	YUV422 CTRL	0x00	RW	Bit[7:2]: Reserved Bit[1]: v_first 0: Output line will be yuyv... 1: Output line will be yvyu... (It will affect definition of u/v in sde. If it is set, all registers in sde about u/v must be swapped.) Bit[0]: cnv_opt 0: Average mode 1: Drop mode

table 7-1 system control registers (sheet 22 of 25)

address	register name	default value	R/W	description
0xDA	SDE CTRL	0x00	RW	Bit[7]: fixy_en When it is set, the output Y will be a fixed value. Bit[6]: neg_en 0: Disable negative color effect 1: Enable negative color effect Bit[5]: gray_en 0: Disable gray effect 1: Enable gray effect Bit[4]: fixv_en When it is set, the output V will be the value set in register sde_vreg(0xE0) Bit[3]: fixu_en When it is set, the output U will be the value set in register sde_ureg(0xDF) Bit[2]: cont_en 0: Disable contrast/ offset/brightness 1: Enable contrast/ offset/brightness Bit[1]: sat_en 0: Disable saturation effect 1: Enable saturation effect Bit[0]: hue_en 0: Disable hue effect 1: Enable hue effect
0xDB	SDE HUE COS	0x80	RW	Bit[7:0]: hue_cos Cosine value for hue effect
0xDC	SDE HUE SIN	0x00	RW	Bit[7:0]: hue_sin Sine value for hue effect
0xDD	SDE USAT	0x40	RW	Bit[7:0]: sat_u Enhancement for U value in saturation effect
0xDE	SDE VSAT	0x40	RW	Bit[7:0]: sat_v Enhancement for V value in saturation effect
0xDF	SDE UREG	0x80	RW	Bit[7:0]: u_reg U value for fixed U effect
0xE0	SDE VREG	0x80	RW	Bit[7:0]: v_reg V value for fixed V effect

table 7-1 system control registers (sheet 23 of 25)

address	register name	default value	R/W	description
0xE1	SDE YOFFSET	0x00	RW	Bit[7:0]: y_offset Y value for fixed Y effect or the offset value for contrast effect
0xE2	SDE YGAIN	0x20	RW	Bit[7:0]: y_gain Gain in contract effect
0xE3	SDE YBRIGHT	0x00	RW	Bit[7:0]: y_bright Brightness in brightness effect
0xE4	SDE SGNSET	0x06	RW	Bit[7:6]: Reserved Bit[5:0]: sgnset
0xE5	SCALEV CTRL	0x0C	RW	Bit[7]: Manual_mode Bit[6:4]: drop_offset Offset for DCW drop mode Bit[3]: drop_mode Manual DCW drop mode setting Bit[2]: zoom_2ram_mode Manual ram mode setting Bit[1:0]: v_div Maunal div value for DCW
0xE6	VAP CTRL	0x10	RW	Bit[7:5]: Reserved Bit[4]: vap_mean 0: No mean for sum 1: Mean for sum Bit[3:2]: Reserved Bit[1]: g_drop 0: Summary mode 1: Drop mode Bit[0]: br_drop 0: Summary mode 1: Drop mode
0xE7	FIFO CTRL	0x00	RW	BIt[7:6]: Reserved Bit[5:4]: fifo_speed Speed for FIFO data output Bit[3]: fifo_valid_mode 0: HREF mode 1: Valid mode Bit[2]: fifo_man Manual mode for FIFO setting Bit[1:0]: fifo_opt Offset adjustment for FIFO delay
0xE8	FIFO DELAY	0x00	RW	Bit[7:0]: fifo_delay Manual setting for FIFO delay
0xE9	YAVG BLK THRE	0x00	RW	Bit[7:0]: blk_thresh Threshold for blackness

table 7-1 system control registers (sheet 24 of 25)

address	register name	default value	R/W	description
0xE9 sub address: 0x38[3:0]=4'h0	YAVG BRT THRE	0x00	RW	Bit[7:0]: brt_thresh Threshold for brightness
0xE9 sub address: 0x38[3:0]=4'h1	YAVG HOFF L	0x00	RW	yavg_winofh Bit[7:0]: Horizontal offset for window cropping in YAVG.
0xE9 sub address: 0x38[3:0]=4'h2	YAVG VOFF L	0x00	RW	yavg_winofv Bit[7:0]: Vertical offset for window cropping in YAVG
0xE9 sub address: 0x38[3:0]=4'h3	YAVG CTRL	0x00	RW	BIt[7:6]: Reserved Bit[5]: yavg_win_man 0: Window will be the default window 1: Window will be the window set by the registers Bit[4]: yavg_winofv[8] See **YAVG VOFF L** (0xE9, 0x38[3:0] = 4'h2) Bit[3:2]: Reserved Bit[1:0]: yavg_winofh[9:8] See **YAVG HOFF L** (0xE9, 0x38[3:0] = 4'h1)
0xE9 sub address: 0x38[3:0]=4'h4	YAVG HSIZE	0x00	RW	Bit[7]: Reserved Bit[6:0]: yavg_winh Horizontal size of cropping window. It will be multiplied by 8 to be real size.
0xE9 sub address: 0x38[3:0]=4'h5	YAVG VSIZE	0x00	RW	Bit[7]: Reserved Bit[6:0]: yavg_winv Vertical size of cropping window. It will be multiplied by 4 to be real size.
0xEA~ 0xEB	RSVD	–	–	Reserved

table 7-1 system control registers (sheet 25 of 25)

address	register name	default value	R/W	description
0xEC	REGEC	0x00	RW	Bit[7]: BD50auto 0: Select banding filter for 50 Hz manually (**REGEC**[6] (**0xEC**)) 1: Select banding filter for 50 Hz by 50/60 auto detection Bit[6]: MBAND50 0: Select banding filter step for 60 Hz 1: Select banding filter step for 50 Hz
0xED	RSVD	–	–	Reserved
0xEE	REGEE			Register for Group Latch Function
0xEF	OTP CTRL			OTP Control Register
0xF0~ 0xFF	OTP			16 bytes for OTP

8 electrical specifications

table 8-1 absolute maximum ratings

parameter		absolute maximum rating[a]
operating temperature range[b]		-30°C to +70°C
stable image temperature range[c]		-40°C to +125°C
supply voltage (with respect to ground)	$V_{DD\text{-}A}$	4.5V
	$V_{DD\text{-}IO}$	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to $V_{DD\text{-}IO}$ + 1V
I/O current on any input or output pin		± 200 mA
peak solder temperature (10 second dwell time)		245°C

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

b. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

c. image quality remains stable throughout this temperature range table 8-2 DC characteristics (-30°C < T_A < 70°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	3.14	3.3	3.47	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	3.47	V
I_{DD-A}	active (operating) current	TBD	25	TBD	mA
I_{DD-IO}		TBD	25	TBD	mA
$I_{DDS-SCCB}$	standby current	TBD	22	TBD	mA
$I_{DDS-PWDN}$		TBD	22	TBD	µA
digital inputs (typical conditions: AVDD = 2.8V, DOVDD = 1.8V)					
V_{IL}	input voltage LOW		0.8	TBD	V
V_{IH}	input voltage HIGH	TBD	1.0		V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62	1.43		V
V_{OL}	output voltage LOW		0.12	0.18	V
serial interface inputs					
V_{IL}[a]	SIOC and SIOD	-0.5	0	0.54	V
V_{IH}[a]	SIOC and SIOD	1.26	1.8	2.3	V

a. based on DOVDD = 1.8V.

table 8-3 AC characteristics (T_A = 25°C, V_{DD-A} = 3.3V, V_{DD-IO} = 1.8V)

symbol	parameter	min	typ	max	unit
ADC parameters					
B	analog bandwidth		12		MHz
DLE	DC differential linearity error		< 0.5		LSB
ILE	DC integral linearity error		< 0.5		LSB
	setting time for software reset			<1	ms
	setting time for resolution mode change			<1	ms
	setting time for register setting			<300	ms

table 8-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK1)	6	24	27	MHz
t_r, t_f	clock input rise/fall time			5 (10[a])	ns

a. if using the internal PLL

9 mechanical specifications

9.1 physical specifications

figure 9-1 package specifications

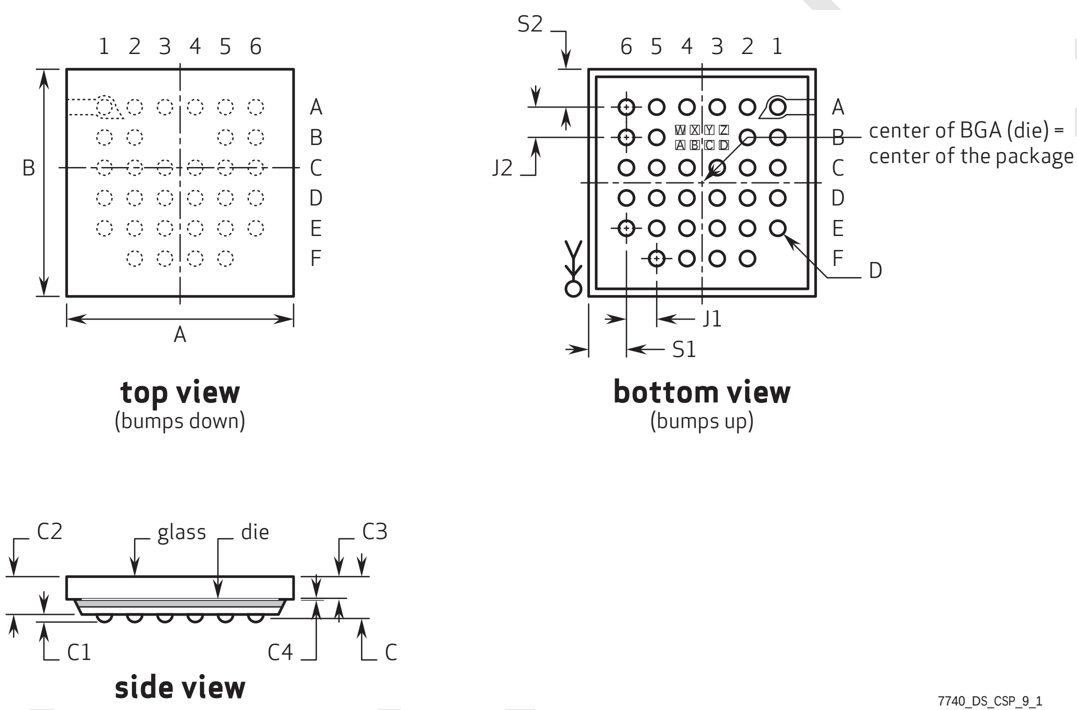


table 9-1 package dimensions (sheet 1 of 2)

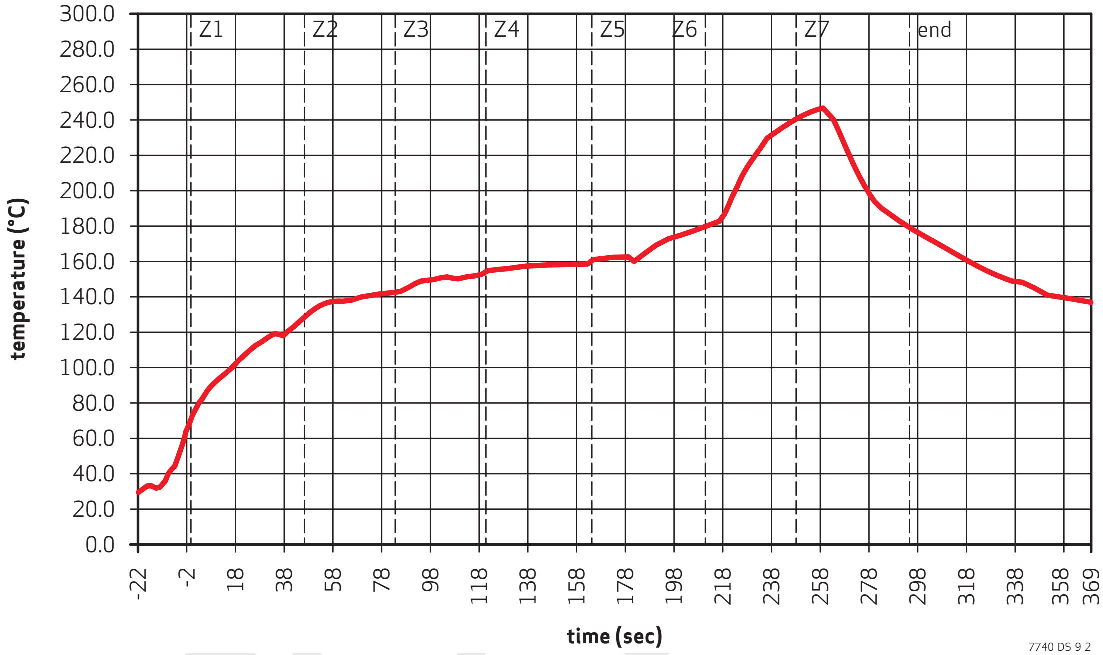
parameter	symbol	min	typ	max	unit
package body dimension x	A	4160	4185	4210	µm
package body dimension y	B	4320	4345	4370	µm
package height	C	720	780	840	µm
ball height	C1	130	160	190	µm
package body thickness	C2	575	620	665	µm
cover glass thickness	C3	390	400	410	µm
airgap between cover glass and sensor	C4	37	41	45	µm
ball diameter	D	270	300	330	µm

table 9-1 package dimensions (sheet 2 of 2)

parameter	symbol	min	typ	max	unit
total pin count	N		32		
pin count x-axis	N1		6		
pin count y-axis	N2		6		
pins pitch x-axis	J1		610		µm
pins pitch y-axis	J2		630		µm
edge-to-pin center distance analog x	S1	538	568	598	µm
edge-to-pin center distance analog y	S2	568	598	628	µm

9.2 IR reflow specifications

figure 9-2 IR reflow ramp rate requirements



note
The OV7740 uses a lead free package.

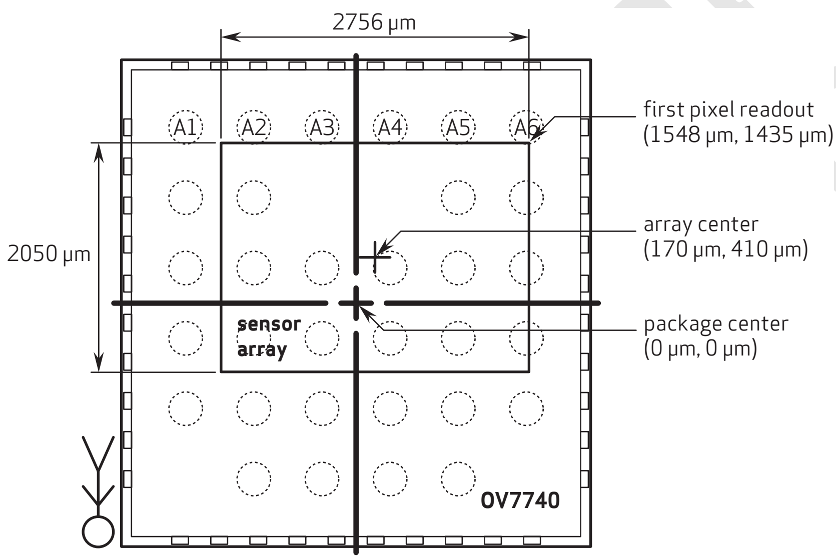
table 9-2 reflow conditions

condition	exposure
average ramp-up rate (30°C to 217°C)	less than 3°C per second
> 100°C	between 330 - 600 seconds
> 150°C	at least 210 seconds
> 217°C	at least 30 seconds (30 ~ 120 seconds)
peak temperature	245°C
cool-down rate (peak to 50°C)	less than 6°C per second
time from 30°C to 245°C	no greater than 390 seconds

10 optical specifications

10.1 sensor array center

figure 10-1 sensor array center



top view

note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.

7740_DS_CSP_10_1

10.2 lens chief ray angle (CRA)

figure 10-2 chief ray angle (CRA)

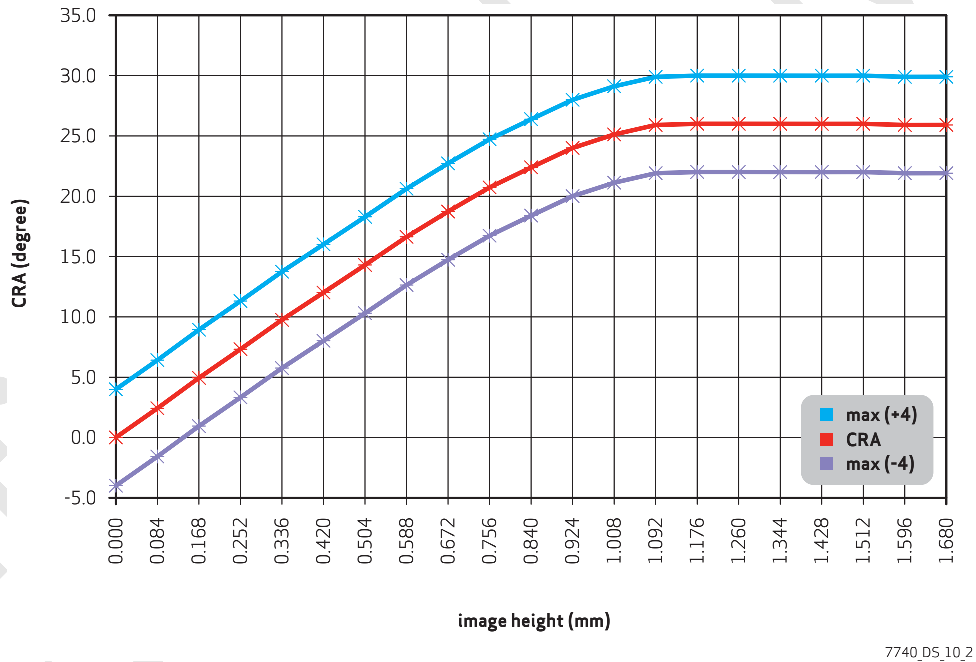


table 10-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0	0.000	0.0
0.05	0.084	2.4
0.1	0.168	4.9
0.15	0.252	7.3
0.2	0.336	9.7
0.25	0.420	12.0
0.3	0.504	14.3
0.35	0.588	16.6
0.4	0.672	18.7
0.45	0.756	20.7

table 10-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.5	0.840	22.4
0.55	0.924	24.0
0.6	1.008	25.1
0.65	1.092	25.9
0.7	1.176	26.0
0.75	1.260	26.0
0.8	1.344	26.0
0.85	1.428	26.0
0.9	1.512	26.0
0.95	1.596	25.9
1	1.680	25.9

revision history

version 1.0 **04.18.2008**

- initial release

version 1.1 **05.09.2008**

- in chapter 4, section 4-2 test pattern updated the description from “For testing purposes, the OV7740 offers one type of test pattern, color bar.” changed to “For testing purposes, the OV7740 offers one type pf test pattern: color bar. There are 4 modes of the color bar (see figure 4-2). The modes of the color bar can be set with the register 0x84[5:4](base address: 0x38[3:0] = 4'h8). In each mode the color bar can be moved from top to bottom if the bar moving function is enabled by setting signal(0x84[4]: base address: 0x38[3:0] = 4'h7) is 1. The moving step can be configured by setting the register 0x84[3:0](base address: 0x38[3:0] = 4'h8) (see table 4-2).”
- in chapter 4, section 4-2 replaced the test pattern figure and updated table 4-2
- in chapter 4, added the following sentence to 4.3.2.3 YAVG “Auto mode only supports non-scaling and non-subsampling image.”
- in chapter 4, modified figure 4-4 “valid pixel size (for VGA, HW = 640, VTS = 480)” changed to “valid pixel size (for VGA, HW = 640, VH = 480)”
- in chapter 4, modified table 4-5 title from “AEC/AGC algorithims” changed to “YAVG window registers”
- in chapter 4, updated section 4.4.1.2 banding mode ON with AEC; from “The band steps for 50Hz and 60Hz light sources can be set in registers 0x49~0x4A.When auto banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto banding is disabled, the minimum integration time is one minimal band. Auto banding can be set in register 0x13[5].”
  changed to
  “The band steps for 50Hz and 60Hz light sources can be set in registers 0x50~0x52. When auto banding is ON, if the next integration time is less than the minimum band step, banding will automatically turn OFF. It will turn ON again when the next integration time becomes larger than the minimum band. If auto banding is disabled, the minimum integration time is one minimal band. Auto banding can be set in register 0x13[4].”
- in chapter 4, updated section 4.4.1.4 VAEC from “The OV7740 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x03[7:5]. VAEC can be disabled by setting register 0x0E[3] to 0.”
  changed to:
  “The OV7740 supports long integration time such as 1 frame, 2 frames, 3 frames and 7 frames. This is achieved by slowing down original frame rate and waiting for exposure. VAEC ceiling can be set in register 0x15[6:4]. VAEC can be disabled by setting register 0x15[7] to 0.”
- in chapter 4, updated table 4-6 title from “AGC registers” changed to “AEC and banding filter register”

- in chapter 4, updated table 4-6 from:

function	register	description
LAEC ON/OFF	0x13[3]	LAEC ON/OFF select 0: OFF 1: ON
banding ON/OFF	0x13[5]	banding ON/OFF 0: OFF 1: ON
VAEC ON/OFF (add frame)	0x15[7]	VAEC ON/OFF select 0: OFF 1: ON
auto banding	0x13[4]	auto banding select 0: OFF 1: ON
VAEC ceiling (max integration time)	0x15[6:4]	VAEC ceiling 001: 1 frame 010: 2 frames 011: 3 frames 1xx: 7 frames
max_band	0x20[5:0]	max band step for in terms of row exposure
banding step	0x50~0x52	0x52[7:6]=BD60st[9:8]; 0x51[7:0] = BD60st[7:0] 0x52[5:4]=BD50st[9:8]; 0x50[7:0] = BD50st[7:0]

changed to:

function	register	description
LAEC ON/OFF	0x13[3]	LAEC ON/OFF select 0: OFF 1: ON
banding ON/OFF	0x13[5]	banding ON/OFF 0: OFF 1: ON
VAEC ON/OFF (add frame)	0x15[7]	VAEC ON/OFF select 0: OFF 1: ON
auto banding	0x13[4]	auto banding select 0: OFF 1: ON
VAEC ceiling (max integration time)	0x15[6:4]	VAEC ceiling 001: 1 frame 010: 2 frames 011: 3 frames 1xx: 7 frames

function	register	description
banding step	0x50~0x52	0x52[7:6]=BD60st[9:8]; 0x51[7:0] = BD60st[7:0] 0x52[5:4]=BD50st[9:8]; 0x50[7:0] = BD50st[7:0]
maximum banding step	0x21	Bit[7:4]: for 50 Hz Bit[3:0]: for 60 Hz

- in chapter 4, updated Table 4-8 digital gain control functions description from:

function	register	description
DGAIN	0x15[1:0]	target 00: Reserved 11: data*4 - target*3

changed to:

function	register	description
DGAIN	0x15[1:0]	00: 1x digital gain 01 or 10: 2x digital gain 11: 4x digital gain

- in chapter 5, updated table 5-1 DSP registers address 0x83 description from

address	register name	default value	R/W	description
0x83	DSP CTRL03	1'b0	RW	Bit[5]: Video 0: disable video off 1: enable video off

changed to:

address	register name	default value	R/W	description
0x83	DSP CTRL03	1'b0	RW	Bit[5]: Video switch 0: video start 1: video stop

- in chapter 5, deleted section 5.3 - S2P
- in chapter 5, section 5.7 auto white balance (AWB); removed from the section description “The module judges whether the color temperature is Day,A or CWF. AWB R/G/B Gain are decided by white pixel G/B and G/R value of current color temperature. AWB R/G/B gain also depends previous awb r/g/b gain.”

- in chapter 5, section 5.8 - white black pixel cancellation; removed from the section description “The new WBC algorithm use some modes to select if the vertical line of bad pixels should be removed or enable the module remove the consecutive bad pixels in same or different channel.”
- in chapter 5, section 5.9 - CIP; added to the section description “Setting the register 0xCC Bit[6:5] to 0 will enable auto mode.”
- in chapter 5, section 5.12 - SCALE_H; removed from the section description “ whether its enable-register is 1 or not.”
- in chapter 5, deleted section 5.17 - FIFO
- in chapter 6, updated section 6.1.2 - HREF mode from
  “HREF mode is the default mode of the DVP (see figure 6-1). Each DVP_VSYNC indicates the starting of a new frame. The OV7740 supports three types of DVP_VSYNC signals (vsync_old, vsync_new, and vsync3) as shown in figure 6-2). DVP_VSYNC, DVP_HREF, and DVP_PCLK can be reversed using the register settings.”

  changed to

  “HREF mode is the default mode of the DVP. Each DVP_VSYNC indicates the starting of a new frame.
- in chapter 6, deleted figure 6-1 DVP timing, figure 6-2 VSYNC timing diagram and section 6.1.3 HSYNC mode

version 1.2 **07.18.2008**

- on the cover page, changed the lens size from 1/13" changed to 1/5"
- under the ordering information, changed the order number from OV7740-CSP changed to OV07740-A32A
- under key specifications, added package dimensions: 4185µm x 4345µm
- in chapter 4, Table 4-7 BLC control functions; replaced the register values of R offset, B offset, Gr offset and Gb offset from

R offset	0x6A[3:2], 0x6D[7:0]	BLC offset for R channel
B offset	0x6A[1:0], 0x6E[7:0]	BLC offset for B channel
Gr offset	0x6A[7:6], 0x6B[7:0]	BLC offset for Gr channel
Gb offset	0x6A[5:4], 0x6C[7:0]	BLC offset for Gb channel

c

Gr offset	0x6E[7:6], 0x6A[7:0]	BLC offset for Gr channel
Gb offset	0x6E[5:4], 0x6B[7:0]	BLC offset for Gb channel
R offset	0x6E[3:2], 0x6C[7:0]	BLC offset for R channel
B offset	0x6E[1:0], 0x6D[7:0]	BLC offset for B channel

- under chapter 7, changed from register 0x13 Bit[4]: Simple histogram changed to register 0x13 Bit[4]: Enable AEC below banding value

- under chapter 7, changed from register 0x16 Reserved changed to 0x16 Bit[7:6]: Reserved, Bit[5]: Sensor vertical output size 1LSB, Bit[4:3]: Sensor horizontal output size 2LSB, Bit[2]: Sensor vertical output start point 1LSB, Bit[1]: Sensor horizontal output start point 2LSB
- under chapter 7, changed register (17, 18, 19) from

Sensor Horizontal Output Start Point MSBs (LSBs in REG16 Bit[1:0])
Sensor Horizontal Output size MSBs (LSBs in REG16 Bit[4:3])
Sensor Vertical Output Start Point MSBs (LSBs in REG16 Bit[2])

changed to:

Sensor Horizontal Output Start Point 8 MSBs (LSBs in REG16 Bit[1:0])
Sensor Horizontal Output size 8 MSBs (LSBs in REG16 Bit[4:3])
Sensor Vertical Output Start Point 8 MSBs (LSBs in REG16 Bit[2])

- under chapter 7, updated register (0x31, 0x32) from:

0x31		0xA0	RW	DSP Output Total Column Number in One Frame
0x32		0xF0	RW	DSP Output Total Line Number in One Frame

changed to:

0x31	HOUTSIZE	0xA0	RW	DSP H output size 8MSB H output size = {Houtsize [7:0] (0x31), REG 34 [2:1] (0x34)}
0x32	VOUTSIZE	0xF0	RW	DSP V output size 8MSB H output size = {Houtsize [7:0] (0x32), REG 34 [0] (0x34)}

- under chapter 7, added register 0x34

0x34	REG34	0x00	RW	Bit[7:3]: Reserved Bit[2]: DSP H output size 2 LSB Bit[0]: DSP V output size 2 LSB

- under chapter 7, updated the following from:

0x84 sub address: 0x38[3:0]=4'h2	AWB_OFF_MAN	0x00	RW	awb_off_man Manual offset for AWB
0x84 sub address: 0x38[3:0]=4'h3	GMA_OFF_MAN	0x00	RW	gma_off_man Manual offset for LENC
0x84 sub address: 0x38[3:0]=4'h4	CMX_OFF_MAN	0x00	RW	cmx_off_man Manual offset for LENC
0x84 sub address: 0x38[3:0]=4'h5	ISP_ROREG _ADDR	0x00	R	isp_roreg_address Read-only registers' address
0x84 sub address: 0x38[3:0]=4'h6	PRE_CTRL0	0x00	RW	Bit[7:5]: Reserved Bit[4]: bar_move When it is set, the color bar is moving color bar. Bit[3]: Reserved Bit[2]: rblue_inv When it is set, the RBlue signal will be inversed Bit[1]: bar_en 0: DSP PRE output normal data 1: DSP PRE output color bar Bit[0]: sht_neg 0: Latch data at rising clock edge 1: Latch data at falling clock edge
0x84 sub address: 0x38[3:0]=4'h7	PRE_CTRL1	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: bar_style Style of the output color bar Bit[3:0]: bar_step Step of the output color bar

changed to:

0x84 sub address: 0x38[3:0]=4'h3	AWB OFF MAN	0x00	RW	awb_off_man Manual offset for AWB
0x84 sub address: 0x38[3:0]=4'h4	GMA OFF MAN	0x00	RW	gma_off_man Manual offset for GMA
0x84 sub address: 0x38[3:0]=4'h5	CMX OFF MAN	0x00	RW	cmx_off_man Manual offset for CMX
0x84 sub address: 0x38[3:0]=4'h6	ROREG ADDR	0x00	R	isp_roreg_address Read-only registers' address
0x84 sub address: 0x38[3:0]=4'h7	PRE CTRL0	0x00	RW	Bit[7:5]: Reserved Bit[4]: bar_move When it is set, the color bar is moving color bar. Bit[3]: Reserved Bit[2]: rblue_inv When it is set, the RBlue signal will be inversed Bit[1]: bar_en 0: DSP PRE output normal data 1: DSP PRE output color bar Bit[0]: sht_neg 0: Latch data at rising clock edge 1: Latch data at falling clock edge
0x84 sub address: 0x38[3:0]=4'h8	PRE CTRL1	0x00	RW	Bit[7:6]: Reserved Bit[5:4]: bar_style Style of the output color bar Bit[3:0]: bar_step Step of the output color bar

- in chapter 9, updated package dimension for package height and package body thickness from:

package height	C	825	885	945	µm
package body thickness	C2	680	725	770	µm

changed to:

package height	C	720	780	840	µm
package body thickness	C2	575	620	665	µm

- under chapter 8, updated table 8-1 with a new absolute maximum ratings table
- in chapter 10, updated the dimensions on the sensor array center

version 1.21 **07.29.2008**

- upated figure 9-1 with new diagram addressing the cover glass thickness

the clear advantage™

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