

- CSE232 -

Homework 2

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① Assume for a particular year that a particular size chip using state-of-the-art technology can contain 1 billion transistors. Assuming Moore's Law (doubling each 18 months) holds, how many transistors will the same size chip be able to contain in ten years?

$$\text{Total number of months in 10 years: } \frac{1 \text{ year} \times 12 \text{ month}}{10 \text{ year} \times ?} = 120 \text{ month}$$

$$120 \text{ month} / 18 \text{ month} \approx 6.67$$

$$\text{If it doubling each 18 months} \rightarrow 1 \text{ billion} \cdot 2^{6.67} \approx \underline{\underline{101.82 \text{ billion}}}$$

transistors.

② Evaluate the Boolean equation $F = (a \text{ AND } b) \text{ OR } c \text{ OR } d$ for the given values of variables a, b, c and d :

a) $a=1, b=1, c=1, d=0$

b) $a=0, b=1, c=1, d=0$

c) $a=1, b=1, c=0, d=0$

d) $a=1, b=0, c=1, d=1$

$$\text{a) } (1 \text{ AND } 1) \text{ OR } 1 \text{ OR } 0 = 1 \text{ OR } 1 \text{ OR } 0 = 1 //$$

$$\text{b) } (0 \text{ AND } 1) \text{ OR } 1 \text{ OR } 0 = 0 \text{ OR } 1 \text{ OR } 0 = 1 //$$

$$\text{c) } (1 \text{ AND } 1) \text{ OR } 0 \text{ OR } 0 = 1 \text{ OR } 0 \text{ OR } 0 = 1 //$$

$$\text{d) } (1 \text{ AND } 0) \text{ OR } 1 \text{ OR } 1 = 0 \text{ OR } 1 \text{ OR } 1 = 1 //$$

③ For the function $F = a + a'b + acd + c'$:

- a) List all the variables. \rightarrow represents a value (0 or 1)
 b) List all the literals. \rightarrow Appearance of a variable, in true or complemented form
 c) List all the product terms. \rightarrow Product of literals.

- a) a, b, c and d .
 b) a, a', b, a, c, d and c' .
 c) $a, a'b, acd$ and c' .

④ Convert the function F shown in the truth table in the table to an equation.
 Don't minimize the equation.

When converting the truth table to an equation, we should consider conditions where the output is 1.

$$F = a'b'c + a'bc' + a'bc + ab'c + abc' + abc$$

inputs			output
a	b	c	F
0	0	0	0
0	0	1	1 $a'b'c$
0	1	0	1 $a'bc'$
0	1	1	1 $a'bc$
1	0	0	0
1	0	1	1 $ab'c$
1	1	0	1 abc'
1	1	1	1 abc

⑤ Use algebraic manipulation to minimize the equation obtained in Exercise 4.

$$F = a'b'c + a'bc' + a'bc + ab'c + abc' + abc$$

$$F = a'(b'c + bc' + bc) + a(b'c + bc' + bc) \quad \text{(Distributive)}$$

$$F = (b'c + bc' + bc) \cdot (a' + a) \quad \text{(Distributive)}$$

$$F = (b'c + bc' + bc) \cdot 1 \quad \text{(complement rule)}$$

$$F = (b'c + b(c' + c))$$

$$F = (b'c + b \cdot 1) \quad \text{(complement rule)}$$

$$F = b'c + b \quad \text{(identity rule)}$$

⑥ Determine whether the Boolean Functions $F = (a+b)' * a$ and $G = a + b'$ are equivalent, using: a) algebraic manipulation, and b) truth tables.

a) $F = (a+b)' \cdot a$ (DeMorgan's Law)

$F = (a' b') \cdot a$ (Associative Law)

$F = (a' a) \cdot b'$ (Complement Law)

$F = b' \cdot 0$ (Null elements)

$F = 0$

$G = a + b'$

$G = a + a' b'$

\neq

b)

a	b	F
0	0	0
0	1	0
1	0	0
1	1	0

\neq

a	b	G
0	0	1
0	1	0
1	0	1
1	1	1

F and G are not equivalent

⑦ Using the combinational design process, create a 4-bit prime number detector. The circuit has four inputs, N_3, N_2, N_1 and N_0 that correspond to a 4-bit number (N_3 is the most significant bit) and one output P that is 1 when the input is a prime number and that is 0 otherwise.

Using the combinational design process:

Step 1

(Truth table)

N_3	N_2	N_1	N_0	P
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1 (2)
0	0	1	1	1 (3)
0	1	0	0	0
0	1	0	1	1 (5)
0	1	1	0	0
0	1	1	1	1 (7)
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1 (11)
1	1	0	0	0
1	1	0	1	1 (13)
1	1	1	0	0
1	1	1	1	0

- $2^4 = 16$ rows in truth table.

- Output is 1 when the input is a prime number.

Step 2

2A (Create Equation)

$$P = N_3'N_2'N_1N_0' + N_3'N_2'N_1N_0 + N_3'N_2N_1'N_0 + N_3'N_2N_1N_0 + N_3N_2'N_1'N_0 + N_3N_2N_1'N_0$$

Simplify the equation:

$$P = N_3'N_2'N_1(\overbrace{N_0' + N_0}^1) + N_3'N_2N_0(\overbrace{N_1' + N_1}^1) + N_3N_2'N_1'N_0 + N_3N_2N_1'N_0$$

→ (use distributive)

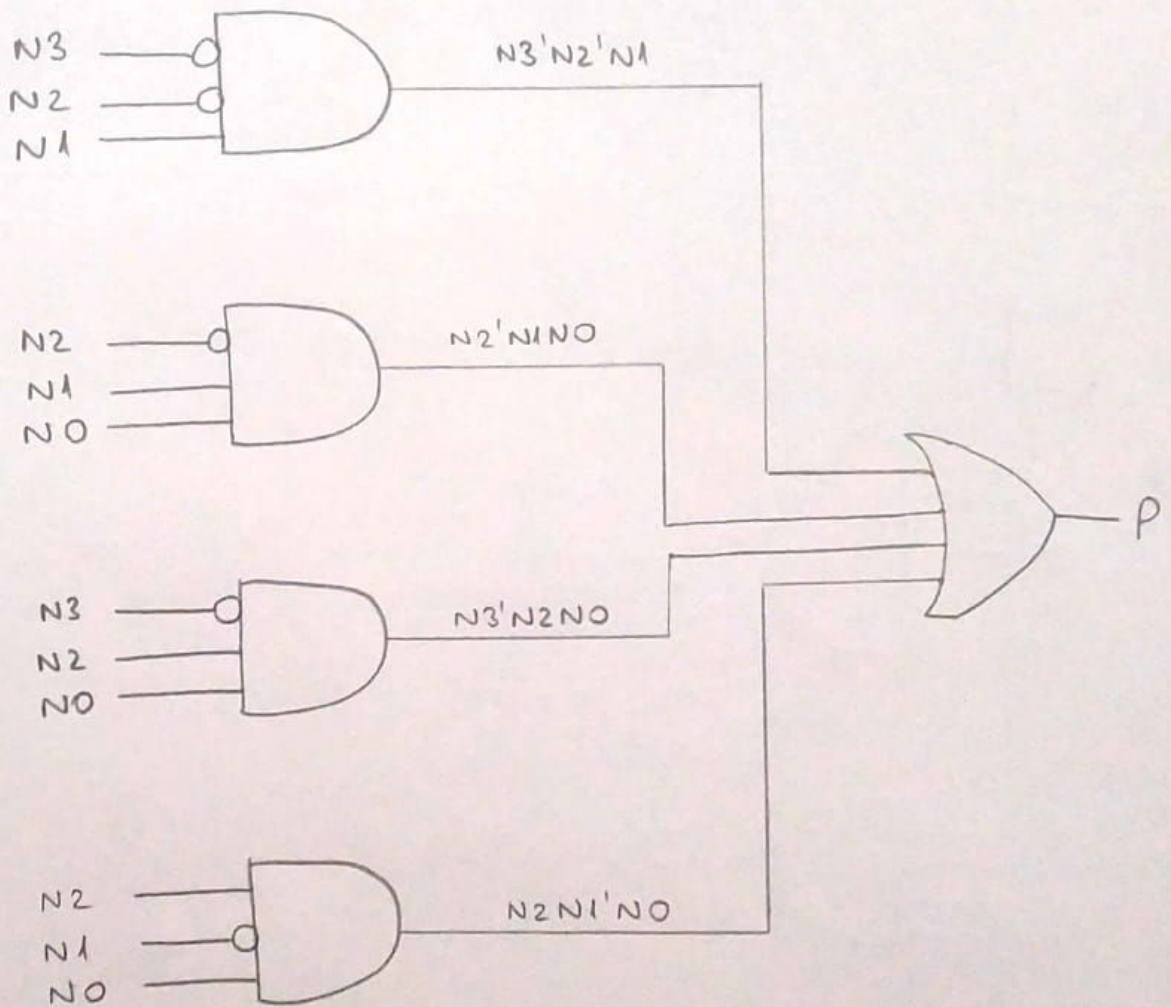
$$= N_2'N_1(N_3' + N_3N_0) + N_2N_0(N_3' + N_3N_1')$$

from $a + a'b = a + b$

$$= N_2'N_1(N_3' + N_0) + N_2N_0(N_3' + N_1')$$

$$P = N_3'N_2'N_1 + N_2'N_1N_0 + N_3'N_2N_0 + N_2N_1'N_0$$

28 (Implement as a gate-based circuit)



8) A network router connects multiple computers together and allows them to send messages to each other. If two or more computers send messages simultaneously, the messages "collide" and the messages must be resent. Using the combinational design process of Table 2.5, create a collision detection circuit for a router that connects 4 computers. The circuit has 4 inputs labeled M0 through M3 that are 1 when the corresponding computer is sending a message and 0 otherwise. The circuit has one output labeled C that is 1 when a collision is detected and 0 otherwise.

Using the combinational design process:

Step 1 (Truth table)

[If two or more input (computer) are 1 then I write output 1]

m3	m2	m1	m0	C
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Step 2 (Create Equation)

2A

Since the ones in the output are less than the zeros.

So I take the zeros while creating the equation and then I take the inverse of the function.

So I got a simpler equation

$$C' = m_3'm_2'm_1'm_0' + m_3'm_2'm_1'm_0 + m_3'm_2'm_1m_0' + m_3'm_2m_1'm_0' + m_3m_2m_1'm_0' + m_3m_2m_1m_0'$$

Simplify the equation:

$$C' = m_3'm_2'm_1' \underbrace{(m_0' + m_0)}_{\substack{1 \\ \text{(complement)}}} + m_3'm_2'm_1m_0' + m_3'm_2m_1'm_0' + m_3m_2'm_1'm_0'$$

$$C = (m_3'm_2'm_1' + m_3'm_2'm_1m_0' + m_3'm_2m_1'm_0' + m_3m_2'm_1'm_0')'$$

2B (Implement as a gate-based circuit)

