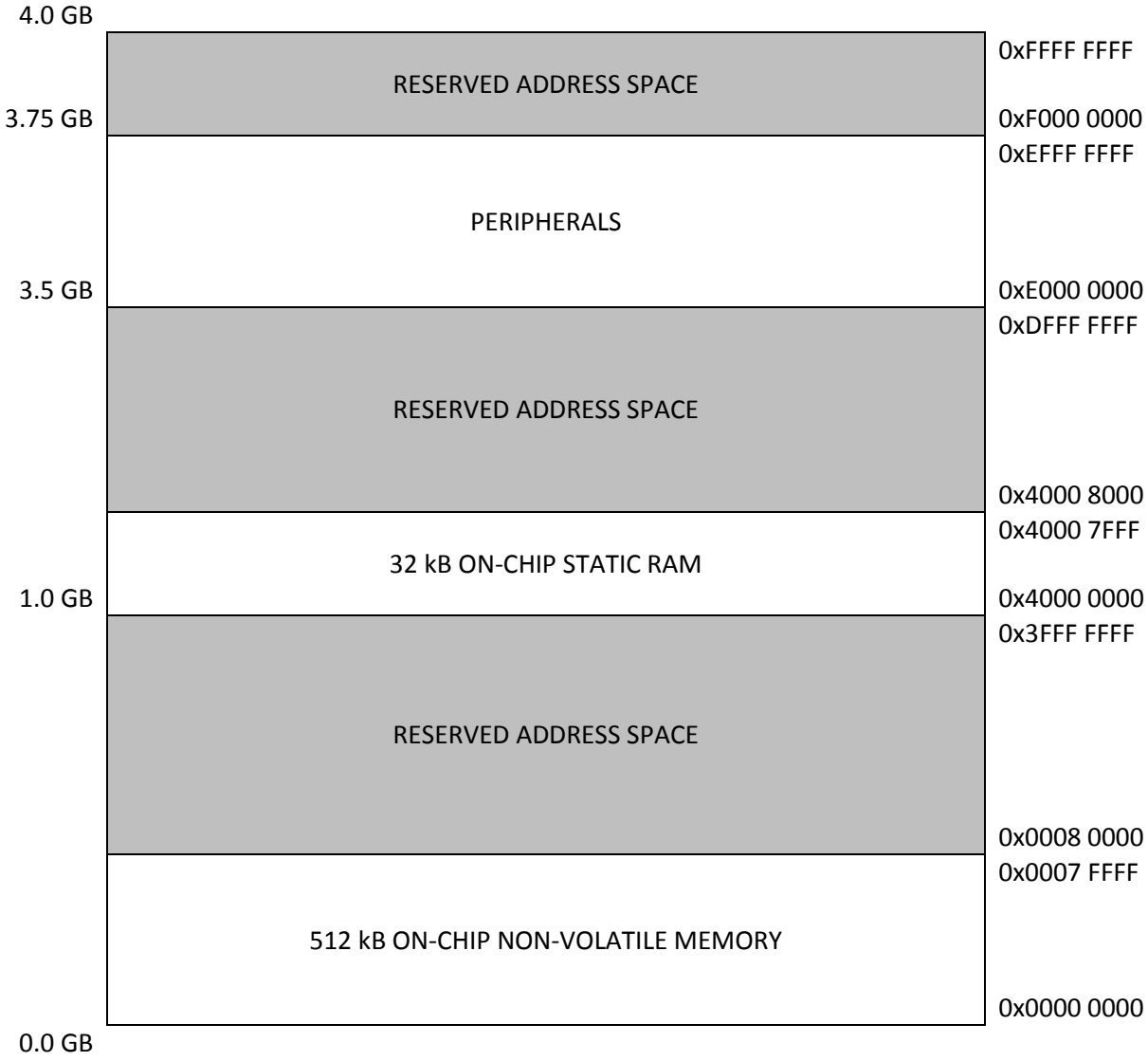
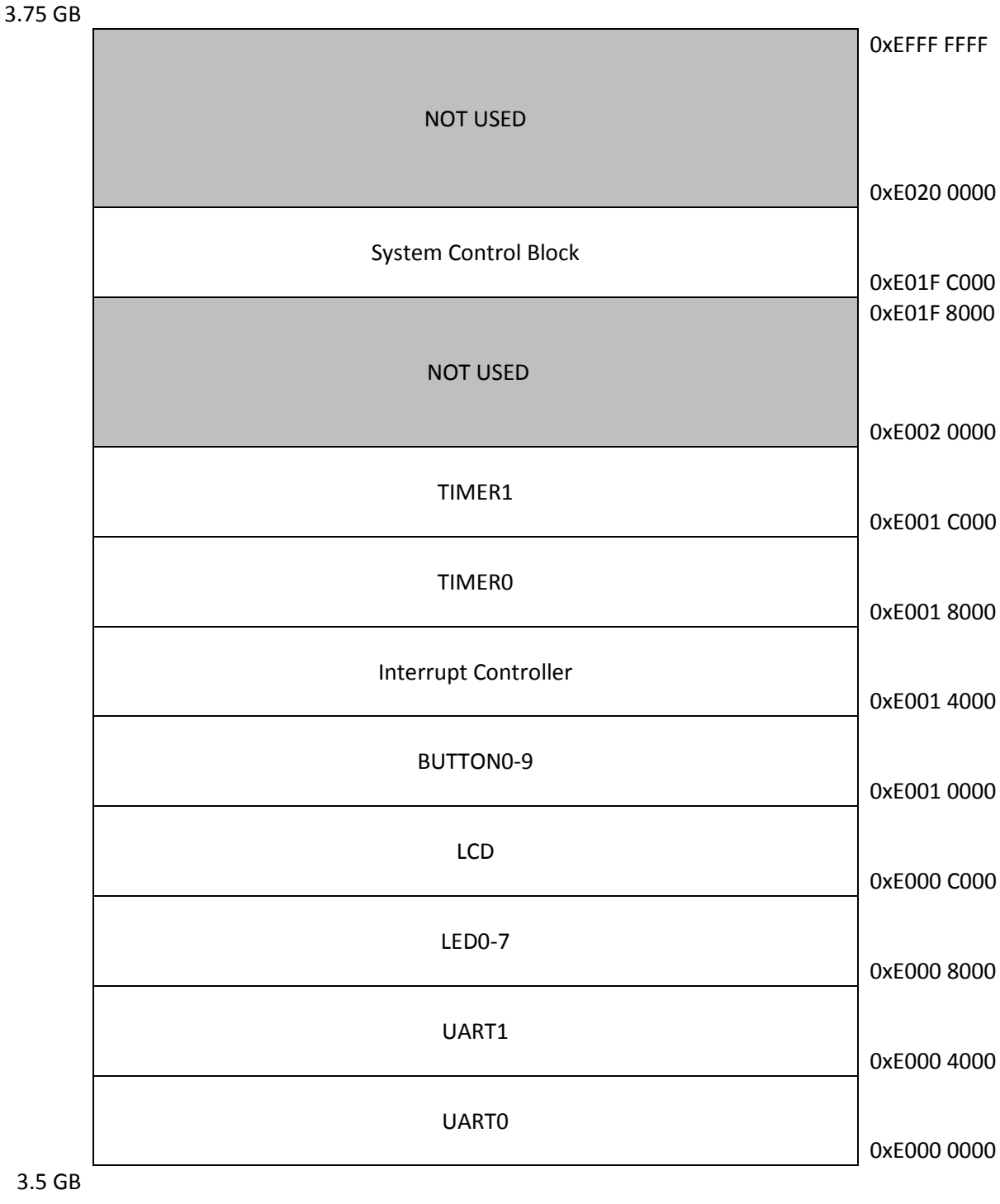
1.1 Memory Map of Development Board



1.2 Detail View of Peripheral Memory Map



1.3 Peripherals

1.3.1 UARTs

The development board contains two 64-byte versions of the *standard* National Semiconductor UARTs. The model is 16750. For an in-depth explanation of the various registers and how to configure them, check out this article.

1.3.2 LED

The development board contains 8 programmable LEDs that can be turned on and off individually. The status of the LEDs can be queried by polling the respective bit of the LED Status Register. To enable LED n set the n-th bit of the LED Status Register. Likewise to disable LED n clear the n-th bit of the LED Status Register.

1.3.3 LCD

The embedded LCD of the development board is modeled after the Hitachi HD44780, although a bit simplified. Check out the *Instruction Description* in the HD44780.pdf file and then look at the provided assembler and C example code. It should be pretty self explainatory then.

1.3.4 Pushbuttons

The development board contains 10 Push Buttons. The status of the Push Buttons can be queried by polling the respective bit of the Button Status Register. If the button is pressed the bit will be set, otherwise it will be cleared. The least significant bit (LSB) corresponds to button 0.

1.3.5 Timers

The development board has two timers used to generate interrupts as time-out timers or interval timers.

Each timer has a 16-bit counter. The cpu clock (CPUCLK, 1/16 CPUCLK and 1/256 CPUCLK) performs counting. Timer interrupts occur when the counter value reaches a certain value specified as the reference value, or when it overflows. The status register flag indicates which of the above has caused the interrupt.

1.3.6 Programmable Interrupt Controller

The PIC is modeled after the PIC used in Samsung's S3C4510B microcontroller (also known as KS32C50100) and provides 21 lines for controlling up to 21 different interrupts.

For a detailed description of the exposed HW registers and how to configure the PIC, take a look at the S3C4510B Datasheet, Chapter 13 (Interrupt Controller).

Overview of interrupt processing

Line	Name	Cause
4	INT_UART0TX	UART0 transmit-interrupt
5	INT_UART0RX	UART0 receive-interrupt
6	INT_UART1TX	UART1 transmit-interrupt
7	INT_UART1RX	UART1 receive-interrupt

1.4 Memory-Mapped Hardware Registers

1.4.1 UART0

U0RBR	*UART0 Receiver Buffer*	0xE000 0000
U0THR	*UART0 Transmitter Holding Buffer*	0xE000 0000
U0DLL	*UART0 Devisor Latch Low Byte*	0xE000 0000
U0DLH	*UART0 Devisor Latch High Byte*	0xE000 0004
U0IER	*UART0 Interrupt Enable Register*	0xE000 0004
U0IIR	*UART0 Interrupt Identification Register*	0xE000 0008
U0FCR	*UART0 FIFO Control Register*	0xE000 0008
U0LCR	*UART0 Line Control Register*	0xE000 000C
U0LSR	*UART0 Line Status Register*	0xE000 0014
U0SCR	*UART0 Scratch Register*	0xE000 001C

1.4.2 UART1

U1RBR	*UART1 Receiver Buffer*	0xE000 4000
U1THR	*UART1 Transmitter Holding Buffer*	0xE000 4000
U1DLL	*UART1 Devisor Latch Low Byte*	0xE000 4000
U1DLH	*UART1 Devisor Latch High Byte*	0xE000 4004
U1IER	*UART1 Interrupt Enable Register*	0xE000 4004
U1IIR	*UART1 Interrupt Identification Register*	0xE000 4008
U1FCR	*UART1 FIFO Control Register*	0xE000 4008
U1LCR	*UART1 Line Control Register*	0xE000 400C
U1LSR	*UART1 Line Status Register*	0xE000 4014
U1SCR	*UART1 Scratch Register*	0xE000 401C

1.4.3 LED0-7

LEDSTATUS	*LED Status Register*	0xE000 8000

1.4.4 LCD

LCDC_IOCTL	*LCD I/O Control Register*	0xE000 C000
LCDC_DATA	*LCD Data Transfer Register*	0xE000 C001

1.4.5 BUTTON0-9

BTNSTATUS	*Button Status Register*	0xE001 0000

1.4.6 Programmable Interrupt Controller

INTMOD	*Interrupt Mode Register*	0xE001 4000
INTPND	*Interrupt Pending Register*	0xE001 4004
INTMSK	*Interrupt Mask Register*	0xE001 4008
INTPRI0	*Interrupt Priority Register 0*	0xE001 400C
INTPRI1	*Interrupt Priority Register 1*	0xE001 4010
INTPRI2	*Interrupt Priority Register 2*	0xE001 4014
INTPRI3	*Interrupt Priority Register 3*	0xE001 4018
INTPRI4	*Interrupt Priority Register 4*	0xE001 401C
INTPRI5	*Interrupt Priority Register 5*	0xE001 4020
INTOFFSET	*Interrupt Offset Register*	0xE001 4024
INTOSET_FIQ	*FIQ Interrupt Offset Register*	0xE001 4028
INTOSET_IRQ	*IRQ Interrupt Offset Register*	0xE001 402C
INTPNDPRI	*Interrupt Pending By Priority Register*	0xE001 4030
INTPNDTST	*Interrupt Pending Test Register*	0xE001 4034

1.4.7 TIMER0

T0_MODE	*Mode Setting and Status Register*	0xE001 8000
T0_COUNT	*Counter Value Register (upper 16 bit fixed to 0)*	0xE001 8004
T0_COMP	*Compare Value Register (upper 16 bit fixed to 0)*	0xE001 8008

T0_MODE: Register for setting modes and reading status

31	07	06	05	04	03	02	01 00
-	OVFF	EQUF	OVFE	CMPE	CUE	ZRET	CLKS
	0	0	0	0	0	0	0

Name	Pos.	Contents
CLKS	1:0	Clock Selection 00 CPUCLK (16.8 MHz) 01 1/16 of the CPUCLK 10 1/128 of the CPUCLK 11 1/256 of the CPUCLK

ZRET	2	Zero Return 0 The counter keeps counting, ignoring the reference value 1 The counter is cleared to 0 when the counter value is equal to the reference value.
CUE	3	Count Up Enable 0 Stops counting. 1 Starts/restarts counting.
CMPE	4	Compare-Interrupt Enable 0 A compare-interrupt is not generated. 1 An interrupt is generated when the counter value is equal to the reference value.
OVFE	5	Overflow-Interrupt Enable 0 An overflow-interrupt is not generated. 1 An interrupt is generated when an overflow occurs.
EQUF	6	Equal Flag The value is set to 1 when a compare-interrupt occurs. Writing 1 clears the equal flag.
OVFF	7	Overflow Flag The value is set to 1 when an overflow-interrupt occurs. Writing 1 clears the overflow flag.

T0_COUNT: Counter register

31	16	15	0
-		COUNT	
0		0	

Name	Pos.	Contents
COUNT	15:0	Counter value The counter value is incremented according to the conditions of the clock specified in the T0_MODE register.

T0_COMP: Comparison register

31	16	15	0
-		COMP	
0		0	

Name	Pos.	Contents
COMP	15:0	Compare value Reference value to be compared with T0_COUNT.

1.4.8 TIMER1

T1_MODE	*Mode Setting and Status Register*	0xE001 C000
T1_COUNT	*Counter Value Register (upper 16 bit fixed to 0)*	0xE001 C004
T1_COMP	*Compare Value Register (upper 16 bit fixed to 0)*	0xE001 C008

T1_MODE: Register for setting modes and reading status

31	07	06	05	04	03	02	01 00
-	OVFF	EQUF	OVFE	CMPE	CUE	ZRET	CLKS
	0	0	0	0	0	0	0

Name	Pos.	Contents
CLKS	1:0	Clock Selection 12 CPUCLK (16.8 MHz) 13 1/16 of the CPUCLK 22 1/128 of the CPUCLK 23 1/256 of the CPUCLK
ZRET	2	Zero Return 2 The counter keeps counting, ignoring the reference value 3 The counter is cleared to 0 when the counter value is equal to the reference value.
CUE	3	Count Up Enable 2 Stops counting. 3 Starts/restarts counting.
CMPE	4	Compare-Interrupt Enable 2 A compare-interrupt is not generated. 3 An interrupt is generated when the counter value is equal to the reference value.
OVFE	5	Overflow-Interrupt Enable 2 An overflow-interrupt is not generated. 3 An interrupt is generated when an overflow occurs.
EQUF	6	Equal Flag The value is set to 1 when a compare-interrupt occurs. Writing 1 clears the equal flag.
OVFF	7	Overflow Flag The value is set to 1 when an overflow-interrupt occurs. Writing 1 clears the overflow flag.

T1_COUNT: Counter register

31	16	15	00
-		COUNT	

0	0

Name	Pos.	Contents
COUNT	15:0	Counter value The counter value is incremented according to the conditions of the clock specified in the T1_MODE register.

T1_COMP: Comparison register

31	16	15	0
-		COMP	
0		0	

Name	Pos.	Contents
COMP	15:0	Compare value Reference value to be compared with T1_COUNT.

1.4.9 System Control Block

The System Control Block includes several system features and control registers for a number of functions that are not related to specific peripheral devices.

PCON *Power Control Register* `0xE01F C000`

Setting the least significant bit (LSB) of the *Power Control Register* will power down the development board and return control to the calling JavaScript code.