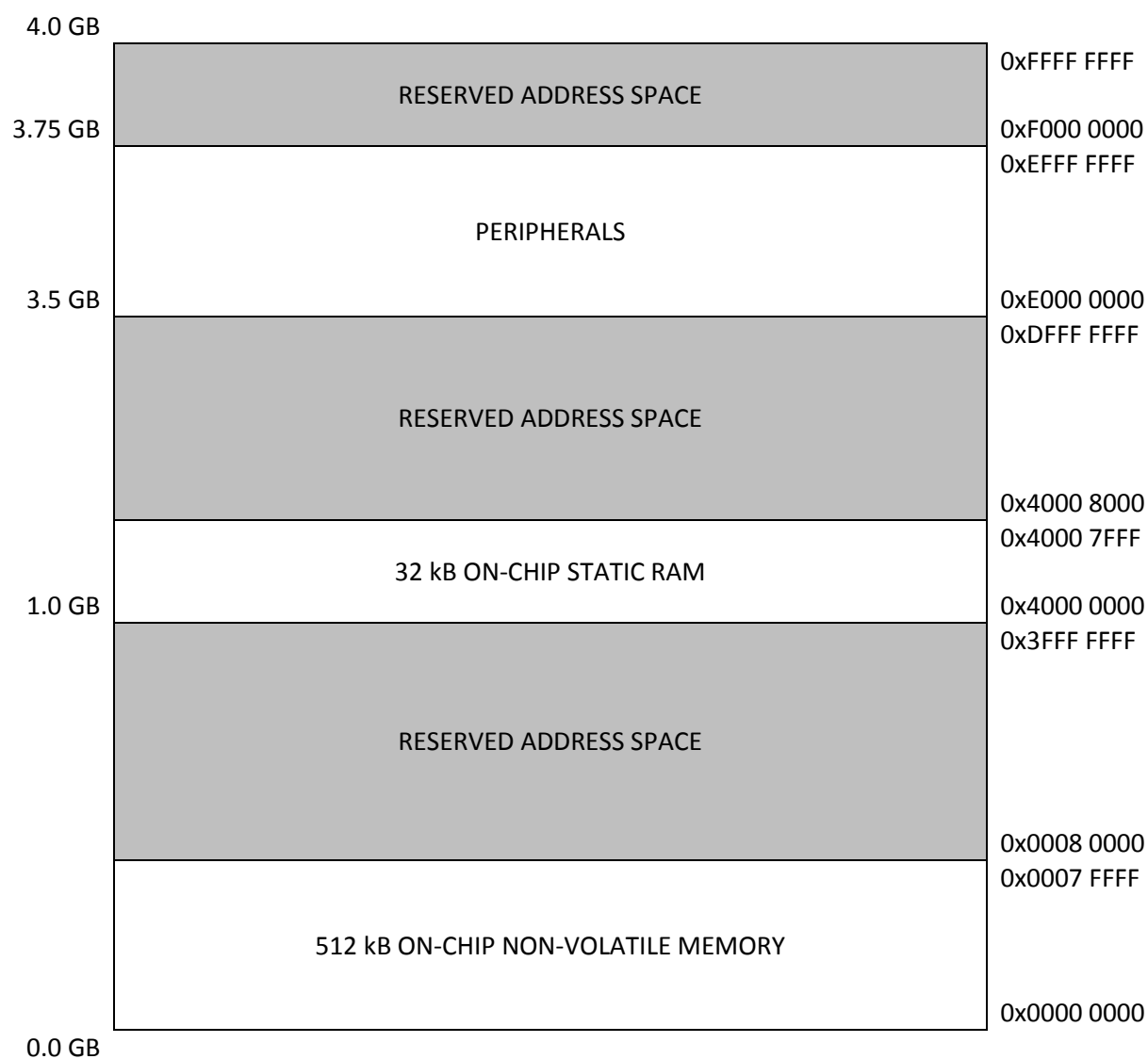


1.1 Memory Map of Development Board



1.2 Detail View of Peripheral Memory Map

3.75 GB		0xEFFF FFFF
	NOT USED	0xE020 0000
	System Control Block	0xE01F C000
	NOT USED	0xE01F 8000
		0xE001 4000
	Interrupt Controller	0xE001 0000
	LCD	0xE000 C000
	LED0-8	0xE000 8000
	UART1	0xE000 4000
3.5 GB	UART0	0xE000 0000

1.3 Memory-Mapped Hardware Registers

1.3.1 UART0

The UARTs are 64-byte versions of the *standard* National Semiconductor UARTs. The model is 16750. For an in-depth explanation of the various registers and how to configure them, check out [this article](#).

U0RBR	<i>UART0 Receiver Buffer</i>	0xE000 0000
U0THR	<i>UART0 Transmitter Holding Buffer</i>	0xE000 0000
U0DLL	<i>UART0 Devisor Latch Low Byte</i>	0xE000 0000
U0DLH	<i>UART0 Devisor Latch High Byte</i>	0xE000 0004
U0IER	<i>UART0 Interrupt Enable Register</i>	0xE000 0004
U0IIR	<i>UART0 Interrupt Identification Register</i>	0xE000 0008
U0FCR	<i>UART0 FIFO Control Register</i>	0xE000 0008
U0LCR	<i>UART0 Line Control Register</i>	0xE000 000C
U0LSR	<i>UART0 Line Status Register</i>	0xE000 0014
U0SCR	<i>UART0 Scratch Register</i>	0xE000 001C

1.3.2 UART1

The UARTs are 64-byte versions of the *standard* National Semiconductor UARTs. The model is 16750. For an in-depth explanation of the various registers and how to configure them, check out [this article](#).

U1RBR	<i>UART1 Receiver Buffer</i>	0xE000 4000
U1THR	<i>UART1 Transmitter Holding Buffer</i>	0xE000 4000
U1DLL	<i>UART1 Devisor Latch Low Byte</i>	0xE000 4000
U1DLH	<i>UART1 Devisor Latch High Byte</i>	0xE000 4004
U1IER	<i>UART1 Interrupt Enable Register</i>	0xE000 4004
U1IIR	<i>UART1 Interrupt Identification Register</i>	0xE000 4008
U1FCR	<i>UART1 FIFO Control Register</i>	0xE000 4008
U1LCR	<i>UART1 Line Control Register</i>	0xE000 400C
U1LSR	<i>UART1 Line Status Register</i>	0xE000 4014
U1SCR	<i>UART1 Scratch Register</i>	0xE000 401C