* 1. Memory Map of Development Board

|  |  |  |
| --- | --- | --- |
| 4.0 GB |  |  |
| 3.75 GB | RESERVED ADDRESS SPACE | 0xFFFF FFFF  0xF000 0000 |
| 3.5 GB | PERIPHERALS | 0xEFFF FFFF  0xE000 0000 |
|  | RESERVED ADDRESS SPACE | 0xDFFF FFFF  0x4000 8000 |
| 1.0 GB | 32 kB ON-CHIP STATIC RAM | 0x4000 7FFF  0x4000 0000 |
|  | RESERVED ADDRESS SPACE | 0x3FFF FFFF  0x0008 0000 |
|  | 512 kB ON-CHIP NON-VOLATILE MEMORY | 0x0007 FFFF  0x0000 0000 |
| 0.0 GB |  |  |

* 1. Detail View of Peripheral Memory Map

|  |  |  |
| --- | --- | --- |
| 3.75 GB |  |  |
|  | NOT USED | 0xEFFF FFFF  0xE020 0000 |
|  | System Control Block | 0xE01F C000 |
|  | NOT USED | 0xE01F 8000  0xE001 4000 |
|  | Interrupt Controller | 0xE001 0000 |
|  | LCD | 0xE000 C000 |
|  | LED0-8 | 0xE000 8000 |
|  | UART1 | 0xE000 4000 |
|  | UART0 | 0xE000 0000 |
| 3.5 GB |  |  |

* 1. Memory-Mapped Hardware Registers
     1. UART0

The UARTs are 64-byte versions of the *standard* National Semiconductor UARTs. The model is 16750. For an in-depth explanation of the various registers and how to configure them, check out [this article](https://en.wikibooks.org/wiki/Serial_Programming/8250_UART_Programming).

|  |  |  |
| --- | --- | --- |
| **U0RBR** | *UART0 Receiver Buffer* | 0xE000 0000 |
| **U0THR** | *UART0 Transmitter Holding Buffer* | 0xE000 0000 |
| **U0DLL** | *UART0 Devisor Latch Low Byte* | 0xE000 0000 |
| **U0DLH** | *UART0 Devisor Latch High Byte* | 0xE000 0004 |
| **U0IER** | *UART0 Interrupt Enable Register* | 0xE000 0004 |
| **U0IIR** | *UART0 Interrupt Identification Register* | 0xE000 0008 |
| **U0FCR** | *UART0 FIFO Control Register* | 0xE000 0008 |
| **U0LCR** | *UART0 Line Control Register* | 0xE000 000C |
| **U0LSR** | *UART0 Line Status Register* | 0xE000 0014 |
| **U0SCR** | *UART0 Scratch Register* | 0xE000 001C |

* + 1. UART1

The UARTs are 64-byte versions of the *standard* National Semiconductor UARTs. The model is 16750. For an in-depth explanation of the various registers and how to configure them, check out [this article](https://en.wikibooks.org/wiki/Serial_Programming/8250_UART_Programming).

|  |  |  |
| --- | --- | --- |
| **U1RBR** | *UART1 Receiver Buffer* | 0xE000 4000 |
| **U1THR** | *UART1 Transmitter Holding Buffer* | 0xE000 4000 |
| **U1DLL** | *UART1 Devisor Latch Low Byte* | 0xE000 4000 |
| **U1DLH** | *UART1 Devisor Latch High Byte* | 0xE000 4004 |
| **U1IER** | *UART1 Interrupt Enable Register* | 0xE000 4004 |
| **U1IIR** | *UART1 Interrupt Identification Register* | 0xE000 4008 |
| **U1FCR** | *UART1 FIFO Control Register* | 0xE000 4008 |
| **U1LCR** | *UART1 Line Control Register* | 0xE000 400C |
| **U1LSR** | *UART1 Line Status Register* | 0xE000 4014 |
| **U1SCR** | *UART1 Scratch Register* | 0xE000 401C |

* + 1. LCD

The LCD is modeled after the Hitachi HD44780, although a bit simplified. Check out the *Instruction Description* in the HD44780.pdf file and then look at the provided assembler and C example code. It should be pretty self explainatory then. The exposed HW registers are:

|  |  |  |
| --- | --- | --- |
| **LCDC\_IOCTL** | *LCD I/O Control Register* | 0xE000 C000 |
| **LCDC\_DATA** | *LCD Data Transfer Register* | 0xE000 C001 |

* + 1. Programmable Interrupt Controller

The PIC is modeled after the PIC used in Samsung's S3C4510B microcontroller (also known as KS32C50100). For a detailed description of the exposed HW registers and how to configure the PIC, take a look at the S3C4510B Datasheet, Chapter 13 (Interrupt Controller).

|  |  |  |
| --- | --- | --- |
| **INTMOD** | *Interrupt Mode Register* | 0xE001 0000 |
| **INTPND** | *Interrupt Pending Register* | 0xE001 0004 |
| **INTMSK** | *Interrupt Mask Register* | 0xE001 0008 |
| **INTPRI0** | *Interrupt Priority Register 0* | 0xE001 000C |
| **INTPRI1** | *Interrupt Priority Register 1* | 0xE001 0010 |
| **INTPRI2** | *Interrupt Priority Register 2* | 0xE001 0014 |
| **INTPRI3** | *Interrupt Priority Register 3* | 0xE001 0018 |
| **INTPRI4** | *Interrupt Priority Register 4* | 0xE001 001C |
| **INTPRI5** | *Interrupt Priority Register 5* | 0xE001 0020 |
| **INTOFFSET** | *Interrupt Offset Register* | 0xE001 0024 |
| **INTOSET\_FIQ** | *FIQ Interrupt Offset Register* | 0xE001 0028 |
| **INTOSET\_IRQ** | *IRQ Interrupt Offset Register* | 0xE001 002C |
| **INTPNDPRI** | *Interrupt Pending By Priority Register* | 0xE001 0030 |
| **INTPNDTST** | *Interrupt Pending Test Register* | 0xE001 0034 |