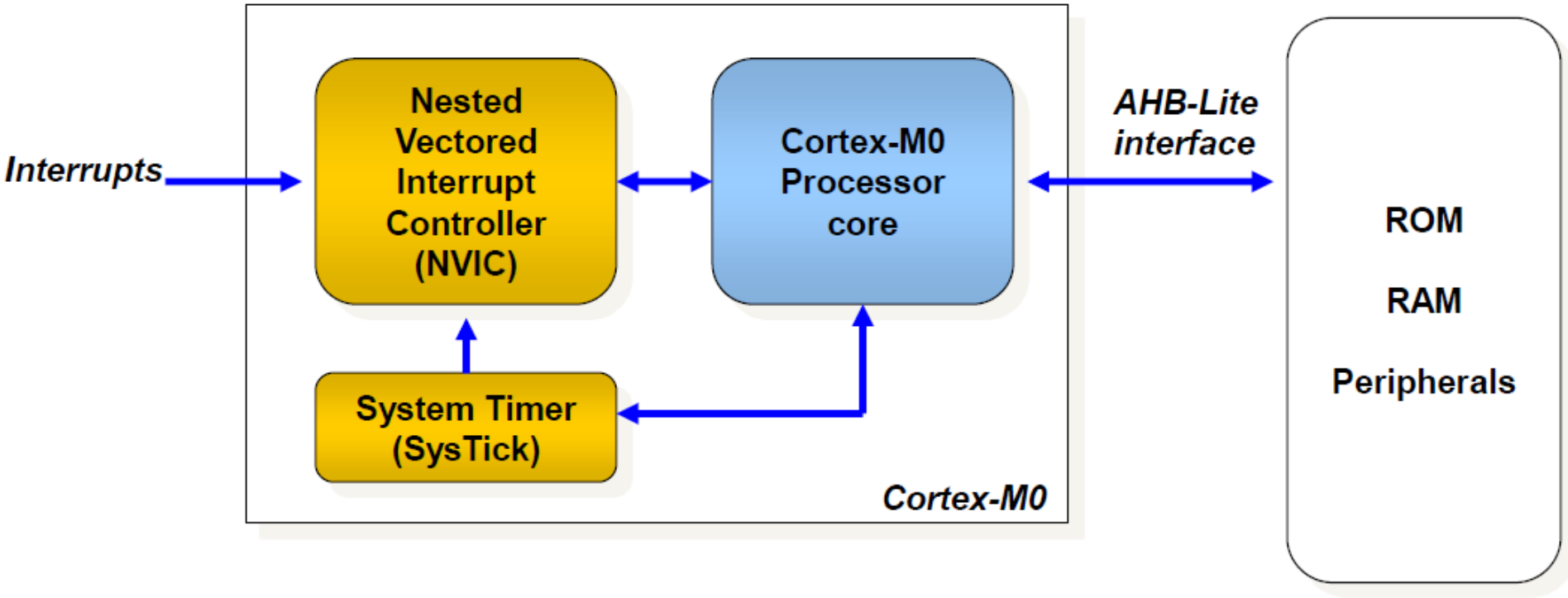
Politechnika Wrocławska

CortexM0 SysTick

Cortex M0

- Cortex-M0 processor includes
  - Cortex-M0 processor core
  - Nested Vectored Interrupt Controller (NVIC)
  - System Timer (SysTick)

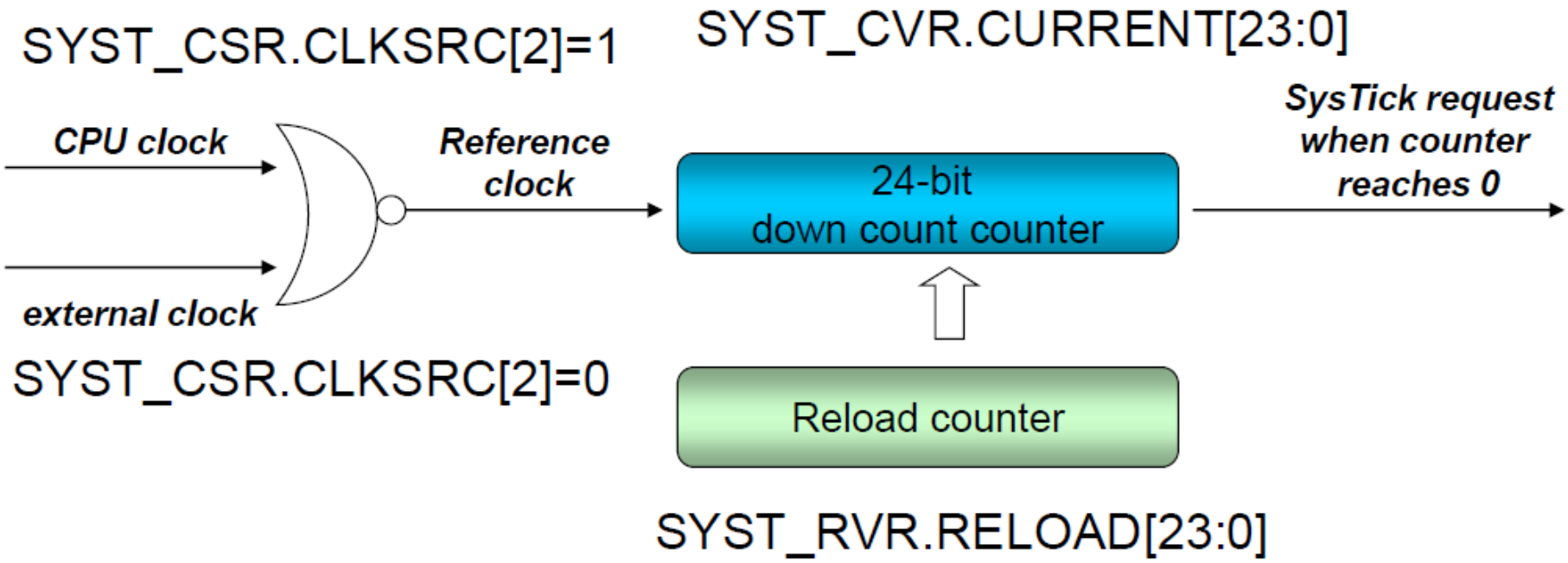


System Timer - SysTick

- SysTick: 24-bit clear-on-write, decrementing, wrap-on-zero counter.
- be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.
- When enabled, count down from SysTick Current Value Register (SYST_CVR) to zero, and reload SysTick Reload Value Register (SYST_RVR), then continue decrement.
- When count down to zero, COUNTFLAG=1. COUNTFLAG=0, on reads.
- SYST_CVR value is UNKNOWN on reset.
- SYST_RVR =0, timer=0. (disable timer even if timer enable)

System Timer - SysTick

- The reference clock can be the core clock or an external clock source.



System timer register

Address	Name	Function	Type	Reset Value
0xE000E010	SYST_CSR	SysTick Control and Status Enables counting and interrupt Selects reference clock source	R/W	0x00000000
0xE000E014	SYST_RVR	SysTick Reload value Copied to current value register when counter reaches 0	R/W	UNKNOWN
0xE000E018	SYST_CVR	SysTick Current value Keeps current counter value	R/W	UNKNOWN
0xE000E01C	SYST_CALIB	SysTick Calibration value Defined by implementation	RO	IMP DEF

SysTick Control and Status (SYST_CSR)

Bits	Name	Function
[16]	COUNTFLAG	=1, if timer counted to 0. =0, read or write to the Current Value register.
[2]	CLKSRC	1 = Core clock used for SysTick. 0 = Clock source is external reference clock
[1]	TICKINT	1 = Counting down to 0 will cause the SysTick exception. 0 = does not cause the SysTick exception. (check COUNTFLAG)
[0]	ENABLE	1 = The counter will operate in a multi-shot manner 0 = The counter is disabled

SysTick timer (STK)

When enabled, the timer:

- counts down from the reload value to zero,
- reloads (wraps to) the value in the STK_RVR on the next clock cycle,
- then decrements on subsequent clock cycles.

Writing a value of zero to the STK_RVR disables the counter on the next wrap.
When the counter transitions to zero, the COUNTFLAG status bit is set to 1.

Reading STK_CSR clears the COUNTFLAG bit to 0.

Writing to the STK_CVR clears the register and the COUNTFLAG status bit to 0. The write does not trigger the SysTick exception logic.
Reading the register returns its value at the time it is accessed.