SESSION 3: **Micron Technology, Inc. Clinic**
FLASH Memory Testing

Officer's Club West
Session Chairman: Gregory S. Bray

12:25 **Gregory S. Bray**
"Introduction to NAND FLASH Project and Overview of GUI and Collaboration Tools"

12:45 **Kyle E. Stewart**
"Technical Overview: USB, Firmware SOPC Builder and the Avalon Bus"

1:05 **Jeff A. Gorton**
"The Design, Function, and Importance of the NAND Controller"

1:25 **Jonathan R. Morgan**
"System Verification Using Simulation Tools and a Digital Probe"

1:45 **Garrett L. Thomas**
"Results and Future Applications of the Project Within the FLASH Industry"

Industrial Liaison: Dean Klein
Dennis Zattiero

Faculty Advisor: Ken Stevens

SESSION 3 12:25 p.m. Officer's Club West

INTRODUCTION TO NAND FLASH PROJECT AND OVERVIEW OF GUI AND COLLABORATION TOOLS

Gregory S. Bray, Kyle E. Stewart, Jeff A. Gorton, Jonathan R. Morgan, Garrett L. Thomas (Ken Stevens), Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112

NAND FLASH memory has become more popular in consumer electronics because of its low cost, high density, low power, shock resistance and non-volatile features. Due to the nature of FLASH technology, the memory has a limited number of use cycles before individual blocks begin to fail. Current NAND FLASH memory is guaranteed to operate for up to 100,000 Program-and-Erase cycles, but failure rates beyond this point are usually unavailable since they will vary significantly between manufacturers and product lines. By developing an open platform for NAND FLASH failure analysis for use by product engineers, we aim to improve the adaptation of NAND FLASH technology in future devices and provide reliable data on failure rates beyond the manufactures cycle limit specifications. The project makes use of an intuitive Graphical User Interface Design (GUI) to provide in-depth analysis of NAND FLASH failure rates and many different online communication and collaboration tools to support a world-wide audience.

SESSION 3 12:45 p.m. Officer's Club West

TECHNICAL OVERVIEW: USB, FIRMWARE, SOPC BUILDER AND THE AVALON BUS

Kyle E. Stewart, Jeff A. Gorton, Jonathan R. Morgan, Garrett L. Thomas, Gregory S. Bray (Ken Stevens), Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112

This presentation deals with the design issues involved with the communication path between the graphical interface running on a desktop machine to the physical NAND FLASH memory. It discusses the use of a user-space Universal Serial Bus (USB) framework to write the driver for the NAND controller without the additional difficulty of working within the Windows kernel framework. It also discusses how existing USB firmware was modified to conform to the USB 2.0 standard. Finally, the presentation includes how previous NAND Controller hardware was modified to fit within the modular architecture of our target FPGA platform as an SOPC Builder component. This allows straightforward communications over the built-in Avalon bus between all the components placed on the FPGA.

SESSION 3 1:05 p.m. Officer's Club West

THE DESIGN, FUNCTION, AND IMPORTANCE OF THE NAND CONTROLLER

Jeff A. Gorton, Jonathan R. Morgan, Garrett L. Thomas, Gregory S. Bray, Kyle E. Stewart (Ken Stevens), Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112

In order for the NAND FLASH to function, it needs perform commands to either retrieve data or write data. There are six of these commands: Erase, Read ID, Read Page, Program Page, Reset, and Read Status. To implement each of these commands, the timing diagrams from the NAND FLASH specifications were studied and evaluated. A state machine was created for each command, first on paper and then written in code. The whole NAND Controller functions as a state machine with three states: Top_Idle, Top_Command, and Top_Done. The first state waits for the command to be given. The second state performs each command, and then the last state restores all default values and returns to the first state. In the second state, Top_Command, each command steps through its state machine. The main function of the NAND Controller is to provide communication between the NAND FLASH chip on the Daughter Board and the Altera DE2 board.

SESSION 3 1:25 p.m. Officer's Club West

SYSTEM VERIFICATION USING SIMULATION TOOLS AND A DIGITAL PROBE

Jonathan R. Morgan, Garrett L. Thomas, Gregory S. Bray, Kyle E. Stewart, Jeff A. Gorton (Ken Stevens), Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112

Changes in NAND FLASH technology have caused current device characterizations to be inaccurate. An automated system was designed to test the robustness of NAND FLASH and create new benchmarks for its performance. The completed development for this system needed to be accomplished within a short amount of time. Simulation using Altera's ModelSim application provided a way to quickly assess major flaws in the design code. Not all problems were found during the simulation and it was necessary to use a more complicated digital probe to scope the various output states. Isolation of specific problems was possible through the use of simulation and hardware testing tools.

SESSION 3 1:45 p.m. Officer's Club West

RESULTS AND FUTURE APPLICATIONS OF THE PROJECT WITHIN THE FLASH INDUSTRY

Garrett L. Thomas, Gregory S. Bray, Kyle E. Stewart, Jeff A. Gorton, Jonathan R. Morgan (Ken Stevens), Department of Electrical and Computer Engineering, University of Utah, Salt Lake City, UT 84112

Due to the extensive time required to discover significant failures over a given SLC NAND FLASH chip, all results at this point are preliminary. This can primarily be attributed to the length of testing required to execute the necessary 100,000+ program and erase cycles (which may require three months or more). Nevertheless, extended testing over the NAND FLASH with its associated results remains the primary objective and pursuit of this project. Going beyond this semester, and more than likely outside this project team, one possible future objective would be the incorporation of different daughter boards for the testing of different manufacturers' NAND FLASH. This would require different drivers and pin maps, but the majority of the application would already be in place. This would prove a valuable asset to manufacturers and integrators. Manufacturers would benefit by knowing at what rate their NAND FLASH begins to fail, thereby allowing the adoption of better ECC (error code correction) algorithms to allow a more refined end. Integrators would be benefited by knowing which manufacturers' NAND FLASH best suits their individual application(s). As an open source project all the code, tutorials, and other relevant information is located on the Google Code webpage so that this project can be adapted to the individual needs of those who are either in the NAND FLASH industry or are looking to use NAND FLASH within one of their applications. All results and findings from this year's testing of Micron NAND will also be shown, so as to give everyone a site for viewing the characteristics of Micron FLASH.