NAND Flash Memory

Serial Peripheral Interface (SPI)

MT29F1G01ZAC

Features

- Single-level cell (SLC) technology
- Organization
  - Page size:
    x1: 2112 bytes (2048 + 64 bytes)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size: 1Gb: 1024 blocks
- Data retention: 10 years
- Endurance: 100,000 PROGRAM/ERASE cycles

Options

- Density: 1Gb (single die)
- Operating temperature:
  - Commercial (0°C to +70°C)
  - Extended (–40°C to +85°C)
- Package (available for SPI only):
  - 63-ball VFBGA, lead-free (10.5mm x 13mm)[1]
  - 63-ball VFBGA, lead-free (9mm x 11mm)[2]

Notes: 1. Package code HC.
2. Package code H4.

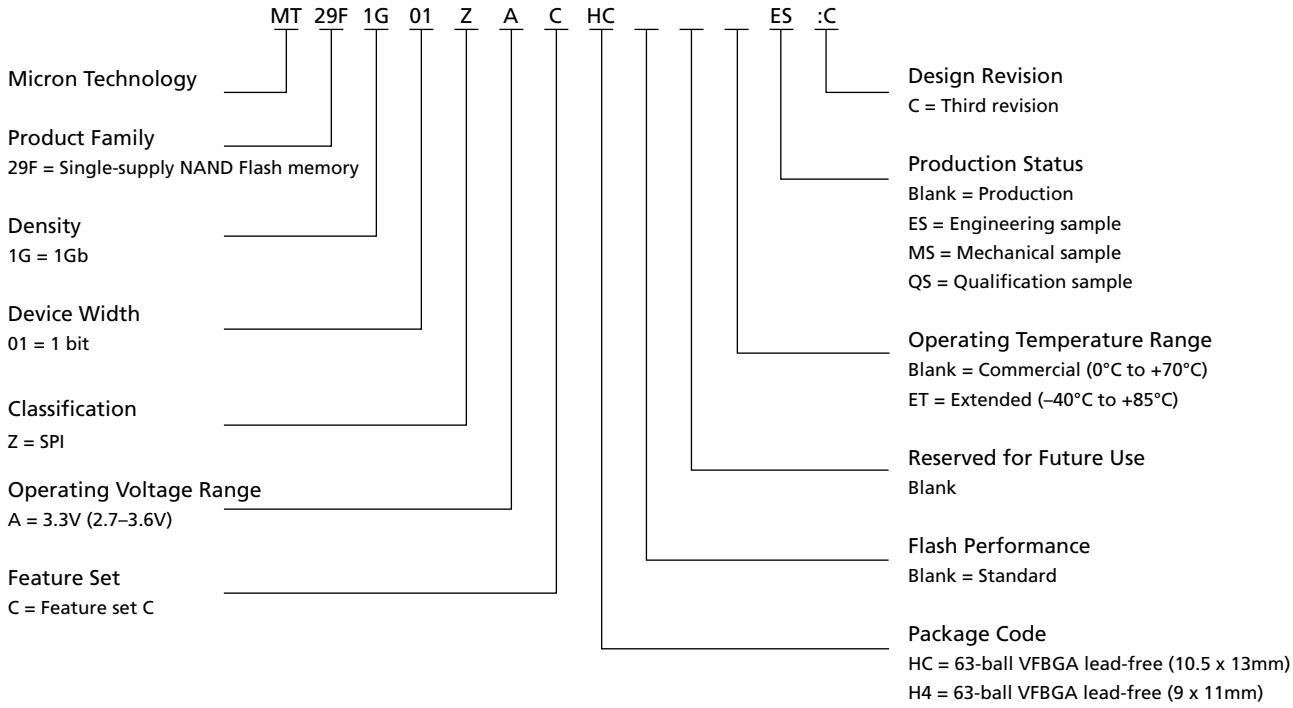
Table 1: SPI NAND Flash Parameters

Parameters	Values
V_{CC} range	2.7–3.6V
Frequency	50 MHz
Transfer rate	20ns
Loading throughput	50 MT/s
^{t}BERS (BLOCK ERASE)	4ms (TYP)
^{t}PROG (PAGE PROGRAM)	400µs (TYP)
^{t}RD (PAGE READ)	100µs (MAX)
Internal ECC correction	1-bit
Width	x1

Part Numbering Information

Micron® NAND Flash devices are available in different configurations and densities (see Figure 1

Figure 1: SPI Part Number Chart



Valid Part Number Combinations

After building the part number from the part numbering chart, verify that the part number is offered and valid by using the Micron Parametric Part Search Web site at www.micron.com/products/parametric. If the device required is not on this list, contact the factory.

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General Description

The serial peripheral interface (SPI) provides NAND Flash with a cost-effective non-volatile memory storage solution in systems where pin count must be kept to a minimum. It is also an alternative to SPI-NOR, offering superior write performance and cost per bit over SPI-NOR.

MT29F1G01xxx serial NAND Flash is a 1Gb SPI SLC NAND Flash memory device based on the standard parallel NAND Flash. The serial electrical interface follows the industry-standard serial peripheral interface. New command protocols and registers are defined for SPI operation. The command set resembles common SPI-NOR command sets, modified to handle NAND-specific functions and added new features. New features include user-selectable internal ECC.

SPI NAND Flash devices have six signal lines plus V_{CC} and ground (GND). The signal lines are SCK (serial clock), SI, SO (for command/response and data input/output), and control signals CS, HOLD#, WP#. (HOLD# and WP# are not available on SPI-ER devices.) This hardware interface creates a low-pin-count device with a standard pinout that remains the same from one density to another, supporting future upgrades to higher densities without board redesign.

The MT29F1G01xxx serial NAND Flash device contains 1024 blocks. Each block is subdivided into 64 programmable pages. Each page consists of 2112 bytes. The pages are further divided into a 2048-byte data storage region with a separate 64-byte spare area. The 64-byte area is typically used for memory and error management functions. See Table 10 on page 30 for available user area when ECC is enabled.

With internal ECC enabled, ECC code is generated internally when a page is written to the memory core. The ECC code is stored in the spare area of each page. When a page is read to the cache register, the ECC code is calculated again and compared with the stored value. Errors are corrected if necessary. The device either outputs corrected data or returns an ECC error status.

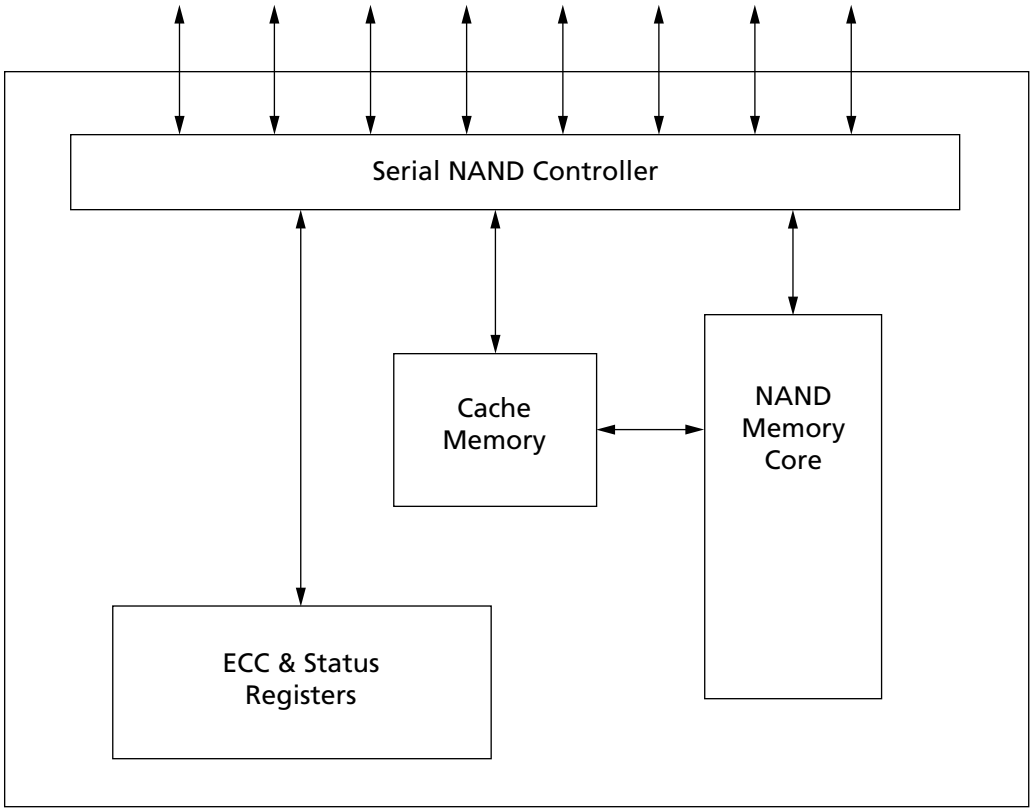
Architecture

These devices use an industry-standard NAND Flash memory core organized by page/block. The standard parallel NAND Flash electrical interface and I/O logic are replaced by an SPI interface. The new command protocol set is a modification of the SPI-NOR command set common in the industry. The modifications are specifically to handle functions related to NAND Flash architecture. The interface supports page and random read/write and copy-back functions. The device also includes an internal ECC feature.

Data is transferred to or from the NAND Flash memory array, page by page, to a data register and a cache register. The cache register is closest to I/O control circuits and acts as a data buffer for the I/O data; the data register is closest to the memory array and acts as a data buffer for the NAND Flash memory array operation.

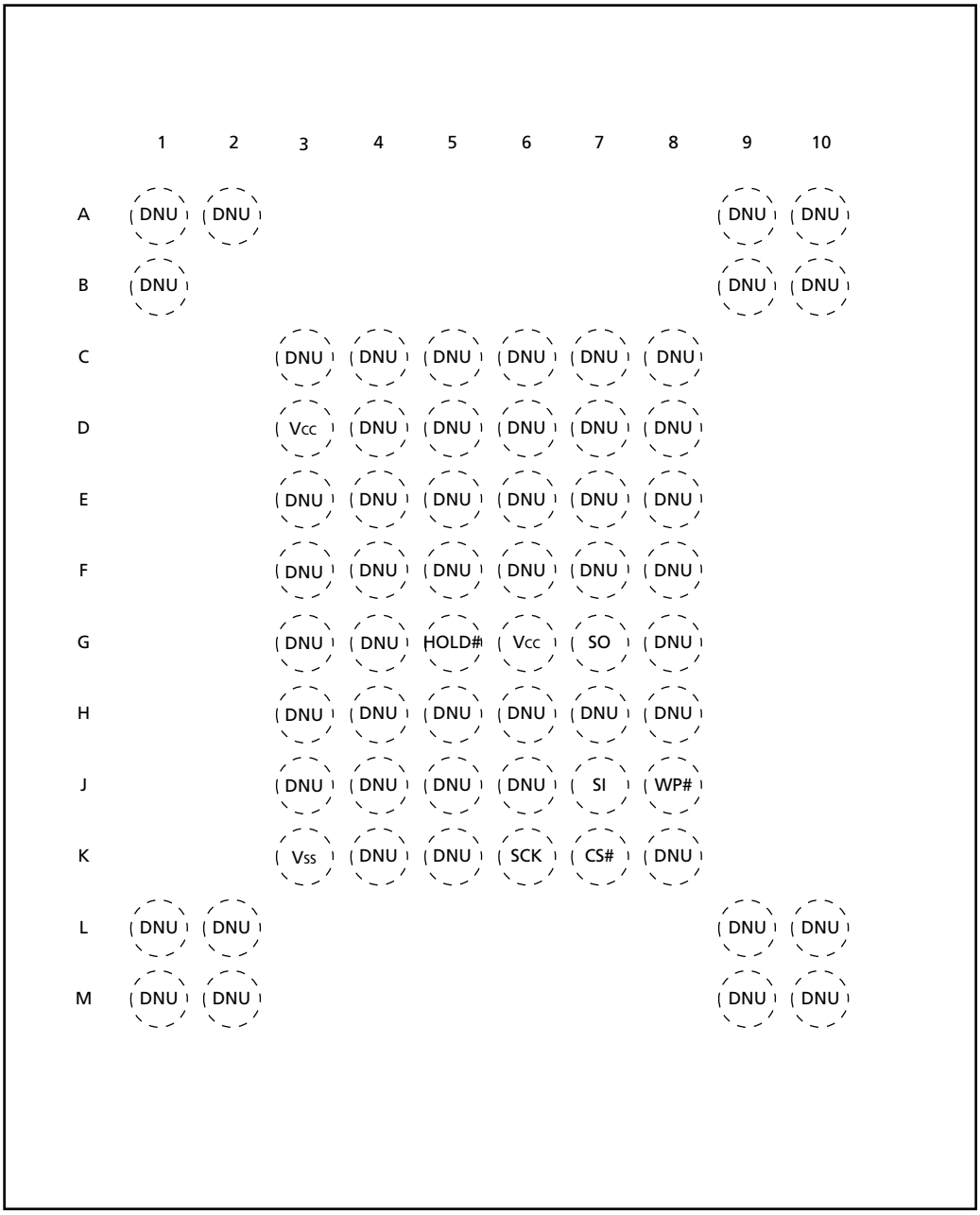
The NAND Flash memory array is programmed and read in page-based operations; it is erased in block-based operations. The cache register functions as the buffer memory to enable random data READ/WRITE operations. These devices also use a new SPI status register that reports the status of device operation.

Figure 2: Functional Block Diagram



Ball Descriptions

Figure 3: Ball Assignment 63-Ball VFBGA



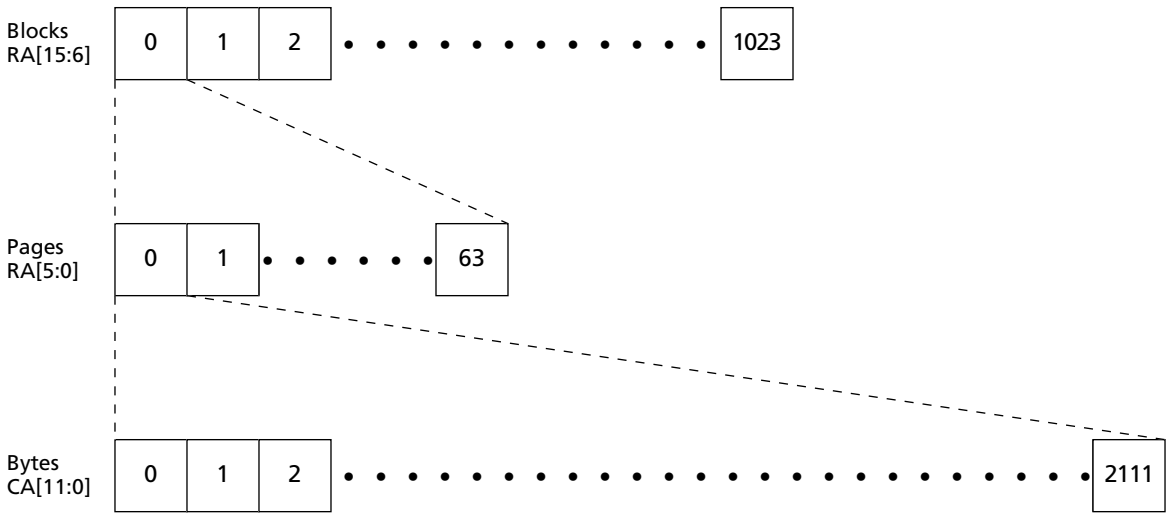
Top View, Ball Down

Table 2: Ball Descriptions

Symbol	Type	Description
CS#	Input	Chip select: Places the device in active power mode when driven LOW. Deselects the device and places SO at high impedance when HIGH. After power-up, the device requires a falling edge on CS# before any command can be written. The device goes to standby mode when no PROGRAM, ERASE, or WRITE STATUS REGISTER operation is in progress. Single command and address sequences and array-based operations are registered on CS#.
DNU	–	Do not use.
HOLD#	Input	Hold: Pauses any serial communication with the device without deselecting it. When driven LOW, SO is at high impedance, and all inputs at SI and SCK are ignored. Requires that CS# also be driven LOW. HOLD# is not available on SPI-ER.
SCK	Input	Serial clock: Provides serial interface timing. Latches commands, addresses, and data on SI on the rising edge of SCK. Triggers output on SO after the falling edge of SCK.
SI	Input	Serial data input: Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK.
SO	Output	Serial data output: Transfers data serially out of the device on the falling edge of SCK.
V_{CC}	Supply	Supply voltage
V_{SS}	Supply	Ground
WP#	Input	Write protect: When LOW, prevents overwriting block-lock bits if BRWD bit is set. WP# is not available on SPI-ER.

Memory Mapping

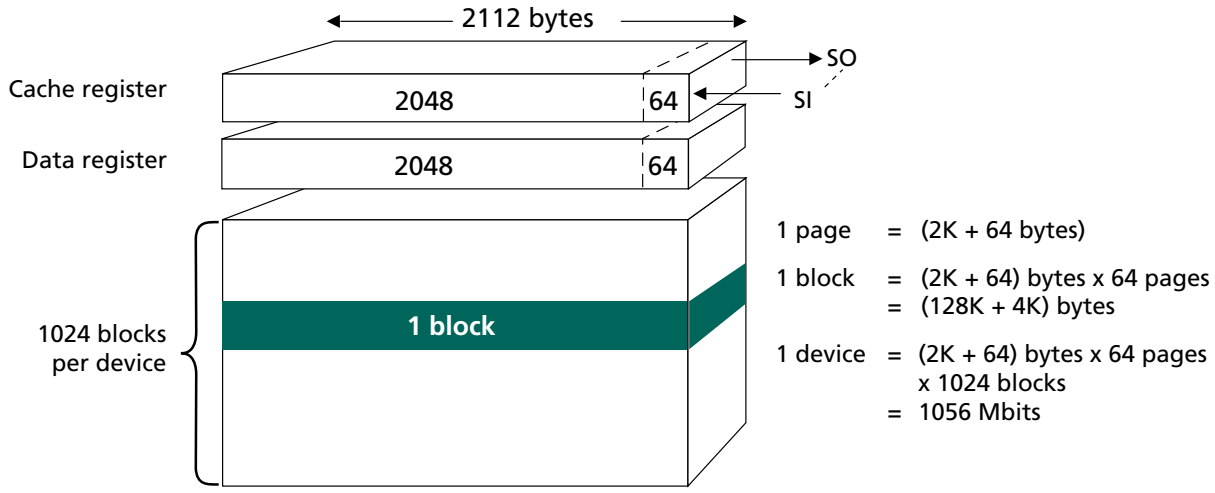
Figure 4: Memory Map



Note: The 12-bit column address is capable of addressing from 0 to 4095 bytes; however, only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are out of bounds, do not exist in the device, and cannot be addressed.

Array Organization

Figure 5: Array Organization



Bus Operation

SPI Modes

SPI NAND supports two SPI modes:

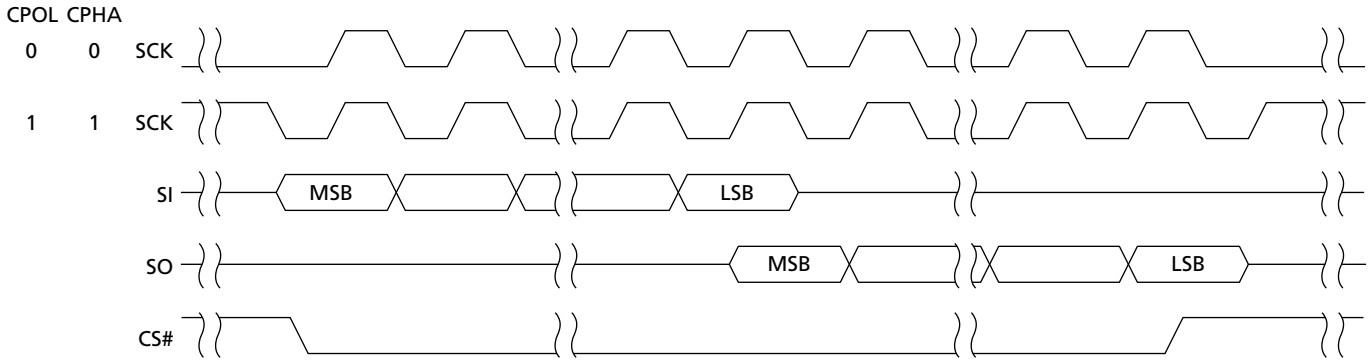
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode:

- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

Figure 6: SPI Modes Timing



Note: While CS# is HIGH, keep SCK at VCC or GND (determined by mode 0 or mode 3). Do not begin toggling SCK until after CS# is driven LOW.

CS#

Chip select (CS#) activates or deactivates the device. When CS goes LOW, the device is placed in active mode. When CS is HIGH, the device is placed in inactive mode and SO is High-Z.

HOLD#

HOLD# input provides a method to pause serial communication with the device but does not terminate any ERASE, READ, or WRITE operation currently in progress.

Hold mode starts at the falling edge of HOLD# provided SCK is also LOW. If SCK is HIGH when HOLD# goes LOW, hold mode begins after the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD# provided SCK is also LOW. If SCK is HIGH, hold mode ends after the next falling edge of SCK.

During hold mode, SO is High-Z and SI and SCK inputs are ignored.

SCK

Serial clock (SCK) provides interface timing for SPI NAND. Addresses, data, and commands are latched on the rising edge of SCK. Data is placed on SO at the falling edge of SCK. When CS# is HIGH, SCK must return either HIGH or LOW.

WP#

Write protect (WP#) prevents the block lock bits (BP0, BP1, and BP2) from being overwritten. If the BRWD bit is set to 1 and WP is LOW, the block protect bits cannot be altered.

SI Address Input and Command Input

Writing to the device is also performed in x1 mode. WRITEs use serial data in (SI). Data, command, and addresses are transferred on SI at the rising edge of SCK.

SO Data Output

Device READs are performed in the x1 mode. READs use serial data out (SO). Data can be clocked out of the device on SO at the falling edge of SCK control signals.

SPI NAND Command Definitions

Table 3: SPI-NAND Command Set

Command	Op Code	Address Bytes	Dummy Bytes	Data Bytes	Comments
BLOCK ERASE	D8h	3	0	0	Block Erase
GET FEATURE	0Fh	1	0	1	Get features
PAGE READ	13h	3	0	0	Array read
PROGRAM EXECUTE	10h	3	0	0	Enter blk/page addr, no data, execute
PROGRAM LOAD	02h	2	0	1 to 2112	Load program data—2kB MAX
PROGRAM LOAD RANDOM DATA	84h	2	0	1 to 2112	Enter cache addr/data
READ FROM CACHE	03h, 0Bh	2	1	1 to 2112	Output cache data at addr
READ ID	9Fh	0	1	2	Read device ID
RESET	FFh	0	0	0	Reset the device
SET FEATURE	1Fh	1	0	1	Set features
WRITE DISABLE	04h	0	0	0	
WRITE ENABLE	06h	0	0	0	

WRITE Operations

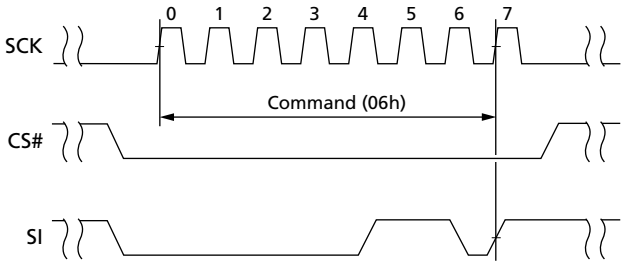
WRITE ENABLE (06h)

The WRITE ENABLE (06H) command sets the WEL bit in the status register to 1.

WRITE ENABLE is required in the following operations that change the contents of the memory array:

- Page program
- OTP program
- BLOCK ERASE

Figure 7: WRITE ENABLE (06h) Timing

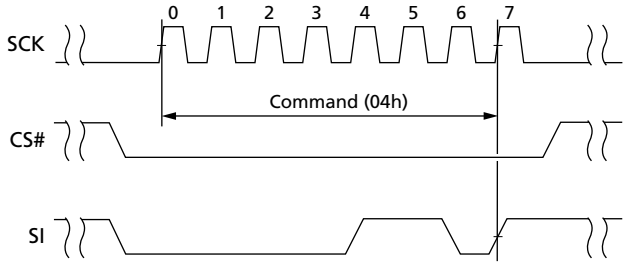


WRITE DISABLE (04h)

The WRITE DISABLE (04H) command clears the WEL bit in the status register by setting it to 0. Clearing the WEL bit disables the following operations:

- Page program
- OTP program
- BLOCK ERASE

Figure 8: WRITE DISABLE (04h) Timing



Features Operations

GET FEATURES (0Fh) and SET FEATURES (1Fh)

The GET FEATURES (0Fh) and SET FEATURES (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and Block Lock can be enabled or disabled by setting specific bits in feature address A0h and B0h (see Table 4). The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to. Unless otherwise specified in Table 4, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Table 4: Features Settings

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	A0h	BRWD[1]	Reserved	BP2	BP1	BP0	Reserved	Reserved	Reserved
OTP	B0h	OTP Protect	OTP Enable	Reserved	ECC Enable	Reserved	Reserved	Reserved	Reserved
Status	C0h	Reserved	Reserved	ECC Status	ECC Status	P_Fail	E_Fail	WEL	OIP

Notes: 1. If BRWD is enabled and WP# is low, then the block lock register cannot be changed. BRWD is not available in SPI-ER.

Figure 9: GET FEATURES (0Fh) Timing

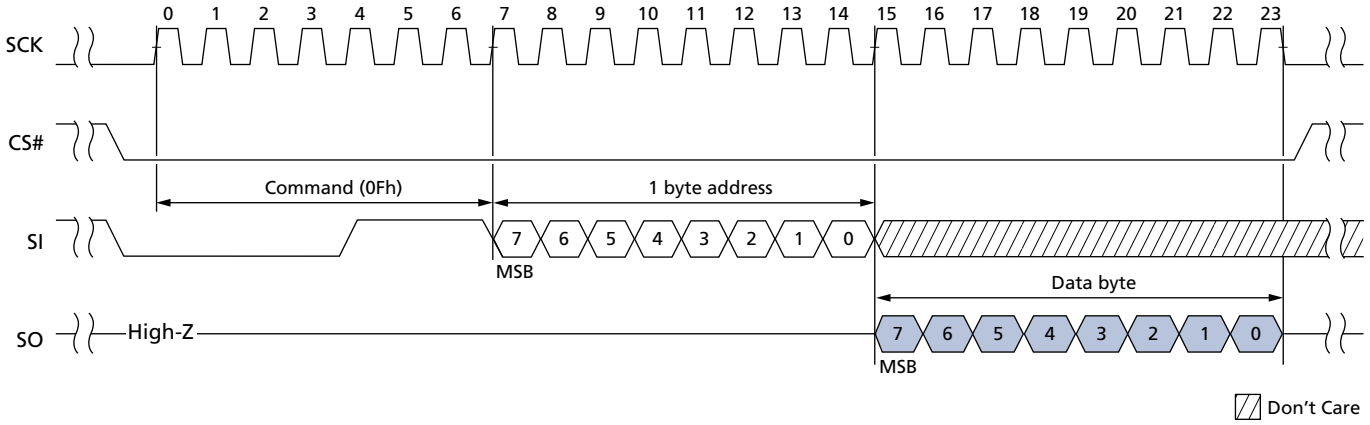
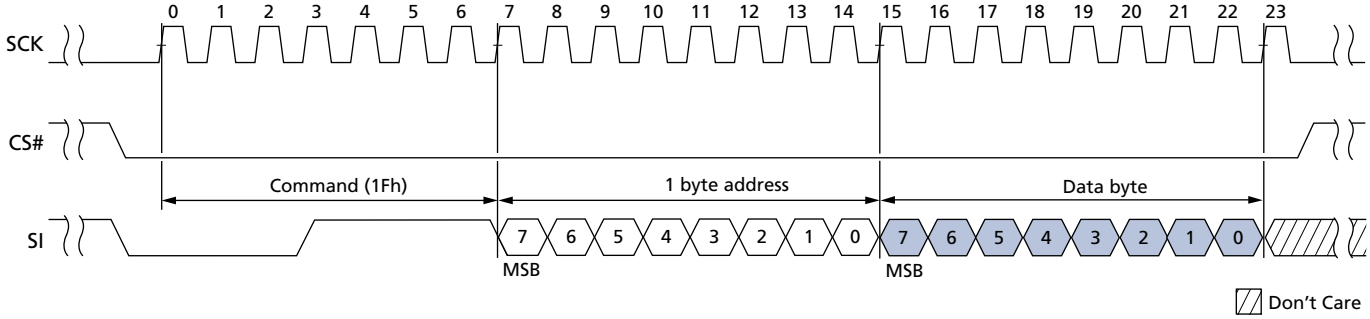


Figure 10: SET FEATURES (1Fh) Timing



READ Operations

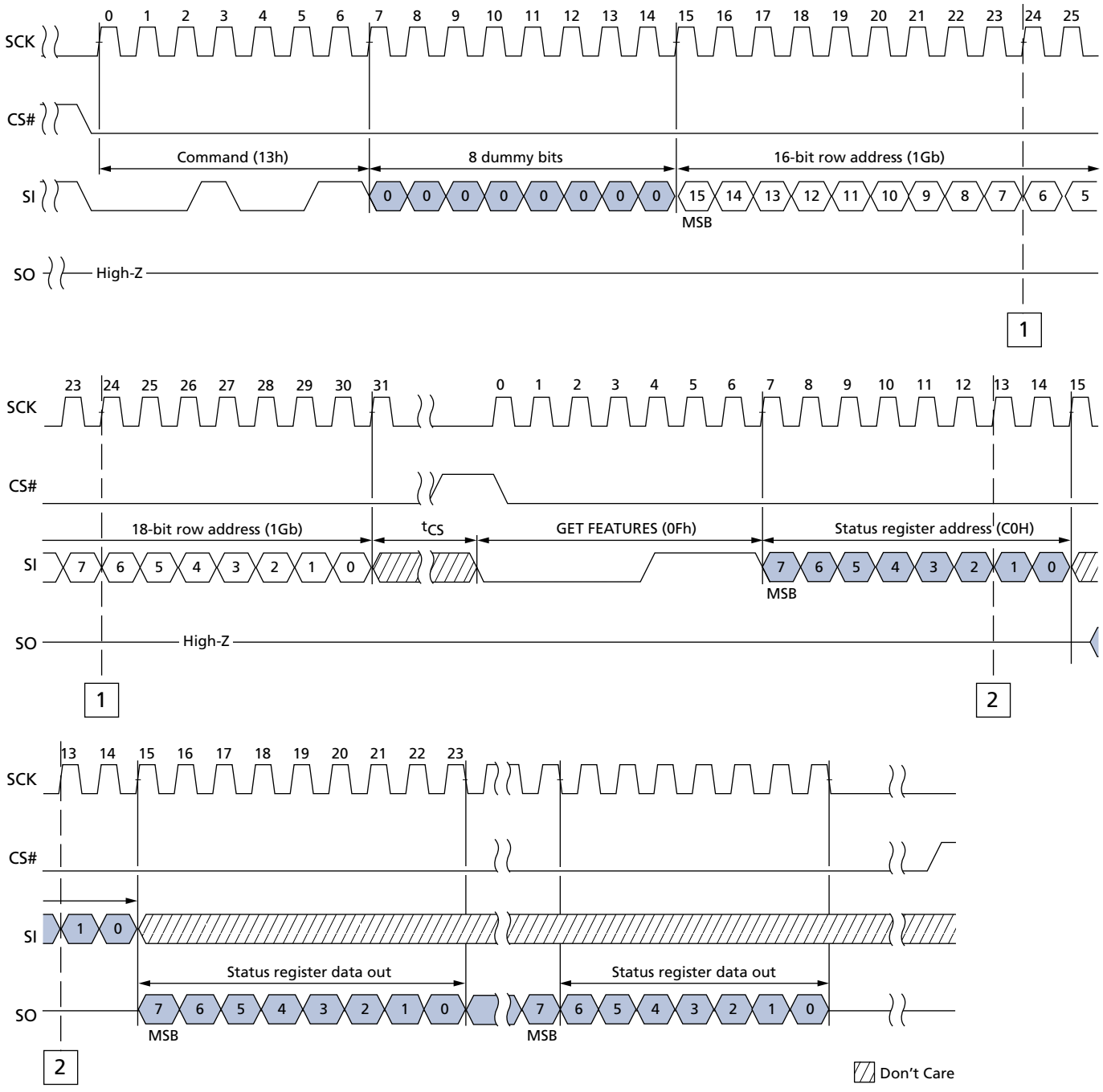
PAGE READ (13h)

The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence is follows:

- 13h (PAGE READ to cache)
- 0Fh (GET FEATURES command to read the status)
- 0Bh or 03h (Random data read)

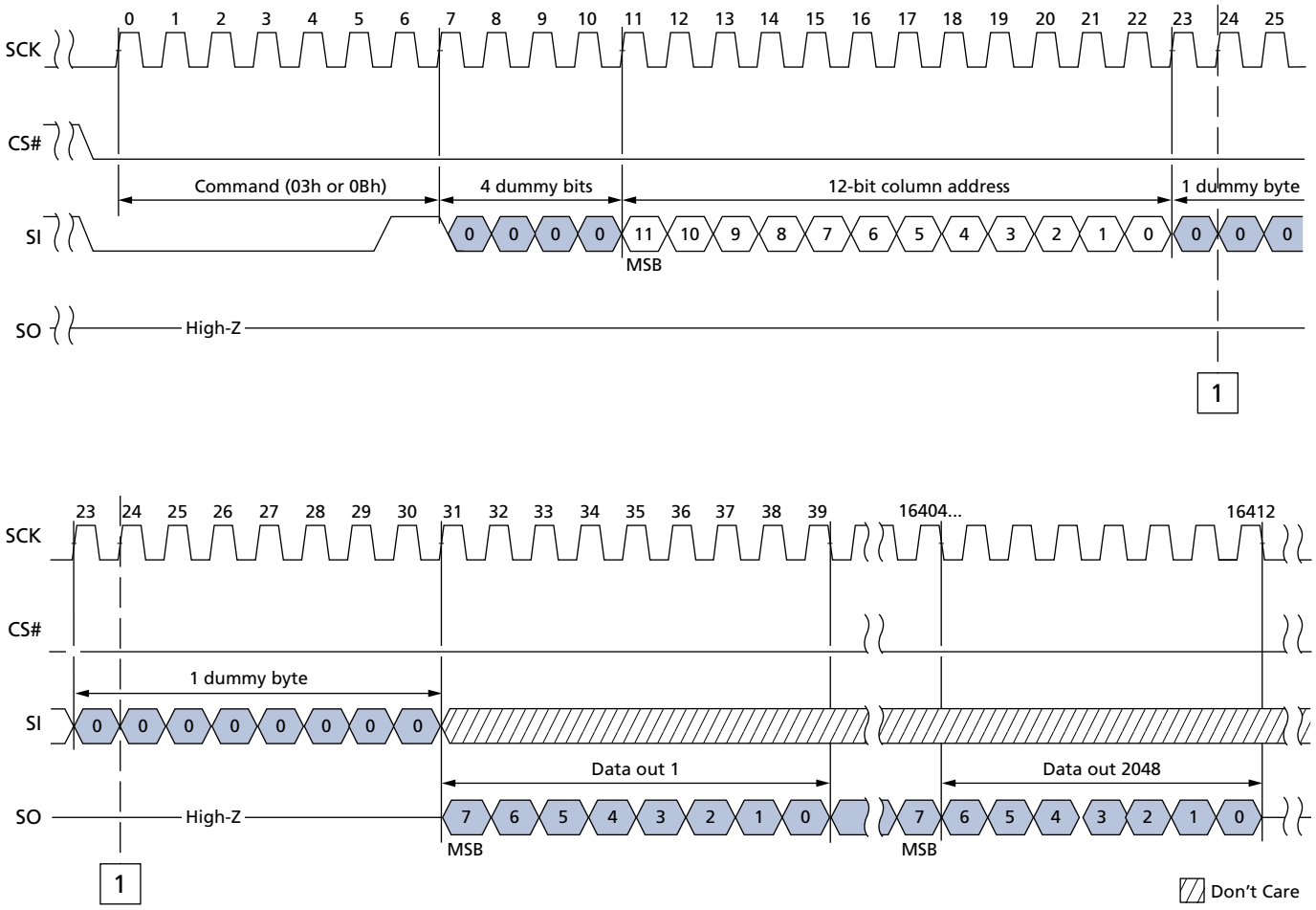
The PAGE READ command requires 8 dummy bits, followed by a 16-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for ^{t}RD time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation. Following a status of successful completion, the RANDOM DATA READ (03h or 0Bh) command must be issued to read the data out of the cache. The RANDOM DATA READ command requires 4 dummy bits, followed by a 12-bit column address for the starting byte address. The starting byte address can be 0 to 2111, but after the end of the cache register is reached, the data does not wrap around and SO goes to a High-Z state. Refer to Figure 11 on page 17 and Figure 12 on page 18 to view the entire READ operation.

Figure 11: PAGE READ (13h) Timing



Note: Timing shown uses Mode 0.

Figure 12: RANDOM DATA READ (03h or 0Bh) Timing



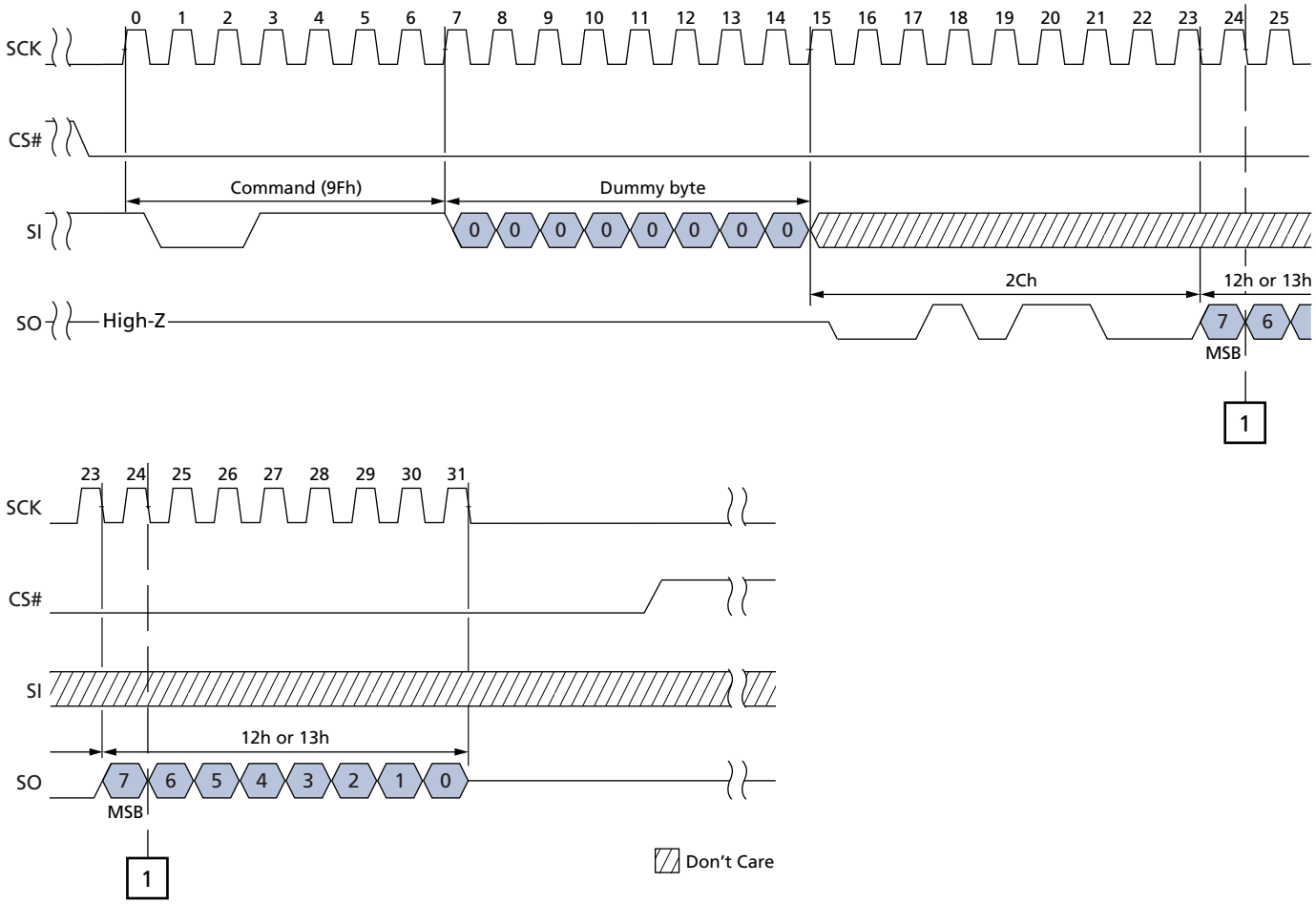
READ ID (9Fh)

The READ ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The READ ID command reads a 2-byte table that includes the Manufacturer ID and the device configuration (see Table 5).

Table 5: READ ID Table

Byte	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value
Byte 0	Manufacturer ID (Micron)	0	0	1	0	1	1	0	0	2Ch
Byte 1	Device ID	0	0	0	1	0	0	1	0	12h

Figure 13: READ ID (9Fh) Timing



Program Operations

Page Program

The page program operation sequence programs 1 byte to 2112 bytes of data within a page. The page program sequence is as follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing the PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed to set the WEL bit. If this command is not issued, then the rest of the program sequence is ignored. WRITE ENABLE must be followed by a PROGRAM LOAD (02h) command. PROGRAM LOAD consists of an 8 bit Op code, followed by 4 dummy bits, a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register that is 2112 bytes long. Only four partial-page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS goes from LOW to HIGH. See Figure 14 on page 21 to see the PROGRAM load operation.

After the data is loaded, a PROGRAM EXECUTE (10h) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by 8 dummy bits and a 16-bit page/block address. After the page/block address is registered, the memory device starts the transfer from the cache register to the main array, and is busy for ^{t}PROG time. This operation is shown in Figure 15 on page 22. During this busy time, the status register can be polled to monitor the status of the operation (refer to “Status Register” on page 27). When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

Figure 14: PROGRAM LOAD (02h) Timing

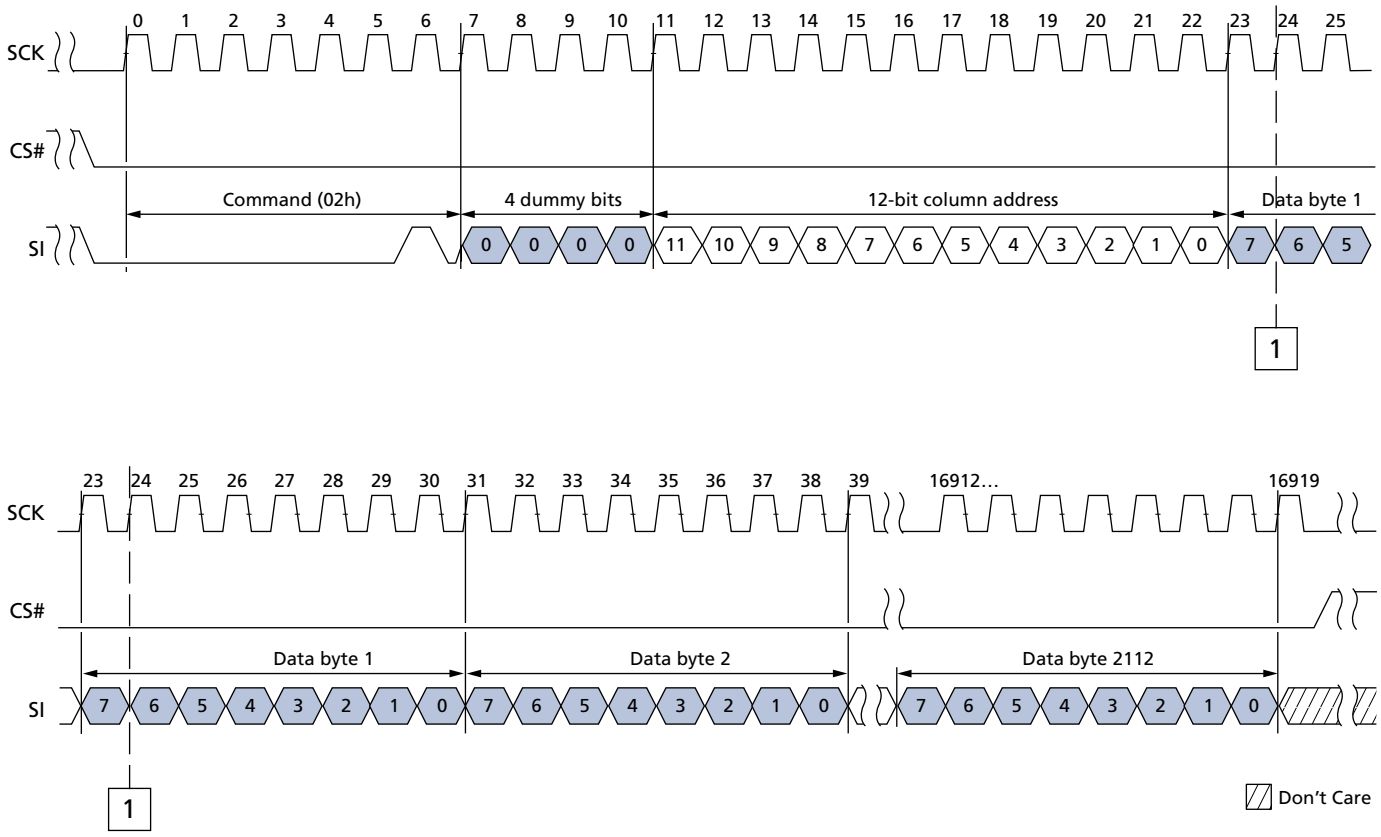
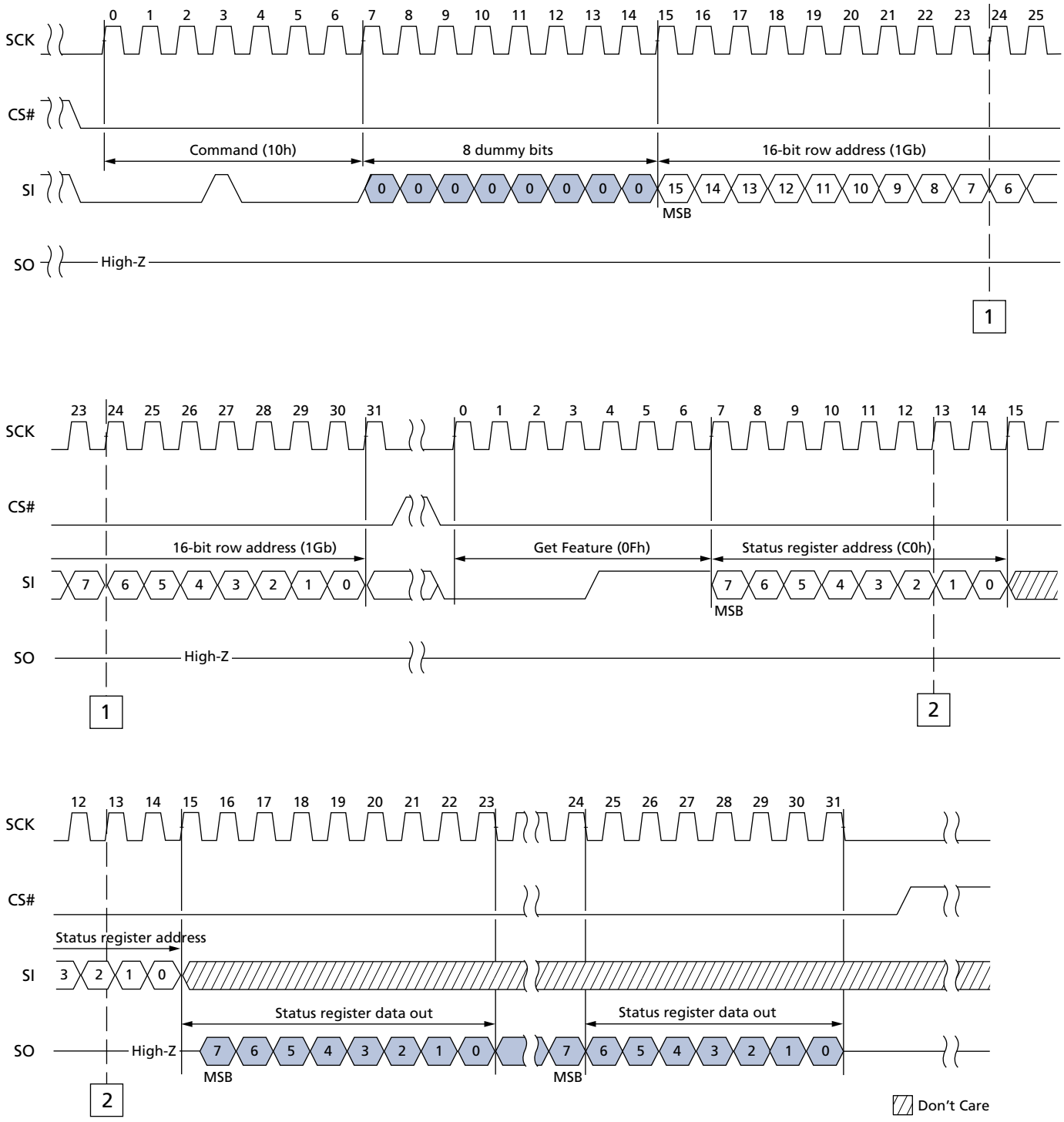


Figure 15: PROGRAM EXECUTE (10h) Timing



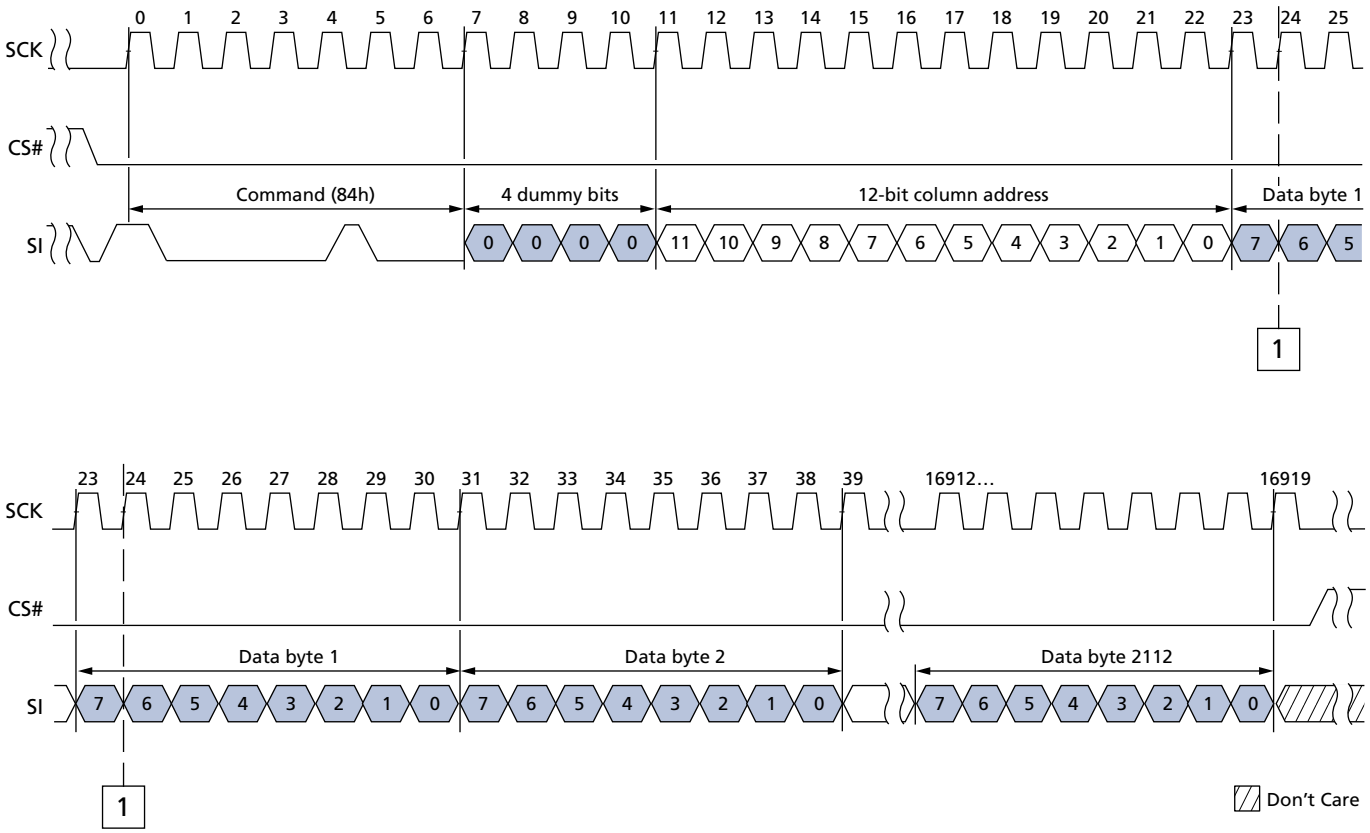
Random Data Program

The random data program operation sequence programs or replaces data in a page with existing data. The random data program sequence is as follows:

- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURES command to read the status)

Prior to performing a PROGRAM LOAD RANDOM DATA operation, a WRITE ENABLE (06h) command must be issued to change the contents of the memory array. Following a WRITE ENABLE (06) command, a PROGRAM LOAD RANDOM DATA (84h) command must be issued. This command consists of an 8-bit Op code, followed by 4 dummy bits with a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h) command must be issued with a new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

Figure 16: PROGRAM LOAD RANDOM DATA (84h) Timing



INTERNAL DATA MOVE

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

- 13h (PAGE READ to cache)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA—Optional)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURES command to read the status)

Prior to performing an INTERNAL DATA MOVE operation, the target page content must be read into the cache register. This is done by issuing a PAGE READ (13h) command (see Figure 11 on page 17). The PAGE READ command must be followed with a WRITE ENABLE (06h) command to change the contents of memory array. After the WRITE ENABLE command is issued, the PROGRAM LOAD RANDOM DATA (84h) command can be issued. This command consists of an 8-bit Op code, followed by 4 dummy bits with a 12-bit column address. New data is loaded in the 12-bit column address. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h) command must be issued with the new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

Block Operations

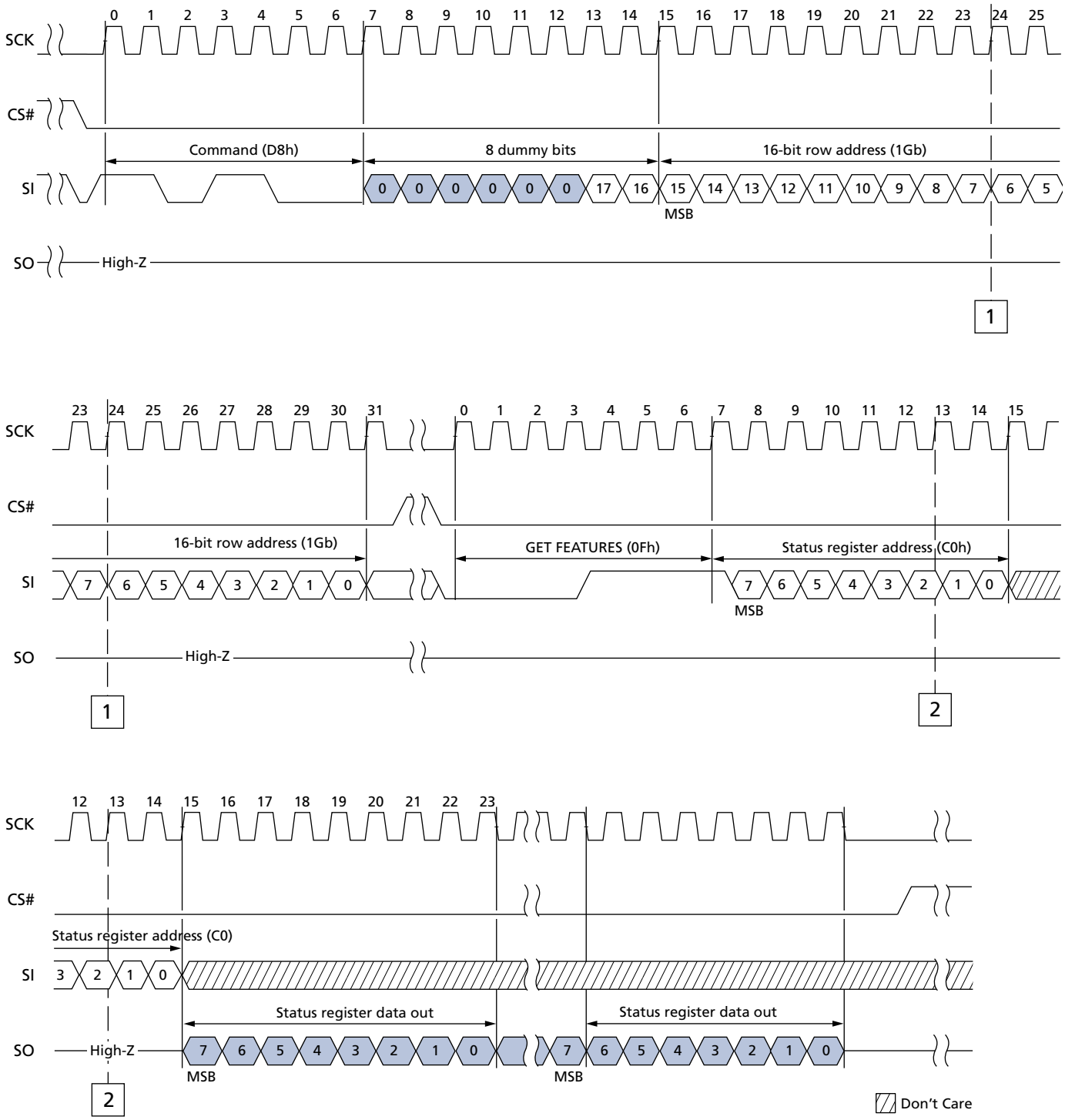
BLOCK ERASE (D8h)

The BLOCK ERASE (D8h) command is used to erase at the block level. MT29F1Gxxx devices have 1024 blocks. They are organized as 64 pages per block, 2112 bytes per page (2048 + 64 bytes). Each block is 132 Kbytes. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENBALE command)
- D8h (BLOCK ERASE command)
- 0Fh (GET FEATURES command to read the status register)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires 24-bit address with 8 dummy bits and 16-bit row addresses. After the row address is registered, the control logic automatically controls the timing and erase-verify operations. The device is busy for ^{t}ERS time during the BLOCK ERASE operation. The GET FEATURES (0Fh) command can be used to monitor the status of the operation (see Figure 17).

Figure 17: BLOCK ERASE (D8h) Timing



Block Lock Feature

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the locked state, i.e., bits 3, 4, and 5 of the block lock register are set to 1. To unlock all the blocks, or a range of blocks, the SET FEATURES command must be issued with the A0h feature address, including the data bits shown in Table 6. The operation for the SET FEATURES command is shown in Figure 10 on page 15. When BRWD is set and WP is LOW, none of the writable bits (3, 4, 5, and 7) in the block lock register can be set. Also, when a PROGRAM/ERASE command is issued to a locked block, a status of 00h is returned. The BWRD feature is not supported in SPI-ER devices.

Table 6: Block Lock Register Block Protect Bits

BP2	BP1	BP0	Protected Rows
0	0	0	None—all unlocked
0	0	1	Upper 1/64 locked
0	1	0	Upper 1/32 locked
0	1	1	Upper 1/16 locked
1	0	0	Upper 1/8 locked
1	0	1	Upper 1/4 locked
1	1	0	Upper 1/2 locked
1	1	1	All locked (default)

For example, if all the blocks need to be unlocked after power-up, the following sequence should be performed:

- Issue SET FEATURES register write (1Fh)
- Issue the feature address to unlock the block (A0h)
- Issue 00h on data bits to unlock all blocks.

One-Time Programmable (OTP) Feature

The serial device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (2112 bytes per page) are available on the device, and the entire range is guaranteed to be good. Customers can use the OTP area any way they want; typical uses include programming serial numbers, or other data, for permanent storage. To access the OTP feature, the user must issue the SET FEATURES command, followed by feature address B0h. When the OTP is ready for access, pages 02h–0Bh can be programmed in sequential order. The PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands can be used to program the pages. Also, the PAGE READ (13h) command can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in Table 7 on page 27.

OTP Access

To access OTP, perform the following command sequence:

- Issue the SET FEATURES register write (1Fh).
- Issue the feature address (B0h).
- Issue the PAGE PROGRAM or PAGE READ command.

It is important to note that after bits 6 and 7 of the OTP register are set by the user, the OTP area becomes read-only and no further programming is supported. For OTP states, see Table 7.

Table 7: OTP States

OTP Protect Bit (7)	OTP Enable Bit (6)	State
0	0	Normal operation
0	1	Access OTP space
1	0	Not applicable
1	1	Use PROGRAM EXECUTE (10h) to lock OTP.

Note: The OTP space cannot be erased and, after it has been protected, cannot be programmed again.

Status Register

The NAND Flash device has an 8-bit status register that software can read during the device operation. The status register can be read by issuing the GET FEATURES (0Fh) command, followed by the feature address C0h (see Figure 9 on page 15).

The status register will output the status of the operation. The description of data bits from status register are shown in Table 8.

Table 8: Status Register Bit Descriptions

Bit	Bit Name	Description
P_Fail	Program fail	When set to 1, this bit indicates that a program failure has occurred. This bit will also be set if the user attempts to program a locked region, including OTP. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command. If the PROGRAM EXECUTE command is issued to an invalid address, when OTP is protected, or if the PROGRAM operation fails, the P_Fail bit is set.
E_Fail	Erase fail	When set to 1, this bit indicates that an erase failure has occurred. This bit will also be set if the user attempts to erase a locked region, or if the ERASE operation fails. This bit is cleared during the BLOCK ERASE command sequence or the RESET command.
WEL	Write enable latch	When set to 1, this bit must be set prior to the following commands. PROGRAM EXECUTE and BLOCK ERASE.
OIP	Operation in progress	When set to 1, this bit is set when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is in the process of executing. The device will read as busy when set to 1. When the bit is 0, the interface is in the ready state.

Table 8: Status Register Bit Descriptions (continued)

Bit	Bit Name	Description
ECC_Status	N/A	A status of 00 means that no bit errors were detected during the previous read algorithm. A status of 01 means that a bit error was detected and corrected. A status of 10 means that multiple bit errors were detected, but and not corrected. During a READ operation or a RESET command, ECC_status is set to 00. ECC_status is invalid if ECC is disabled. After power-up RESET, ECC status is set to reflect the contents of block 0, page 0.
P_Fail	Program fail	When set to 1, this bit indicates that a program failure has occurred. This bit will also be set if the user attempts to program a locked region, including OTP. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command. If the PROGRAM EXECUTE command is issued to an invalid address, when OTP is protected, or if the PROGRAM operation fails, the P_Fail bit is set.
E_Fail	Erase fail	When set to 1, this bit indicates that an erase failure has occurred. This bit will also be set if the user attempts to erase a locked region, or if the ERASE operation fails. This bit is cleared during the BLOCK ERASE command sequence or the RESET command.
WEL	Write enable latch	When set to 1, this bit must be set prior to the following commands. PROGRAM EXECUTE and BLOCK ERASE.
OIP	Operation in progress	When set to 1, this bit is set when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET command is in the process of executing. The device will read as busy when set to 1. When the bit is 0, the interface is in the ready state.

Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in Table 9. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array. NAND Flash devices are shipped from the factory erased. The factory identifies invalidblocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI Factory Defect Mapping requirements. See Table 9 for the bad-block mark.

System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

Table 9: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVB)	1004
Total available blocks per die	1024
First spare area location	byte 2048
Bad-block mark	00h

ECC Protection

The serial device offers data corruption protection by offering 1-bit internal ECC. READs and PROGRAMs with internal ECC can be enabled or disabled by setting the ECC bit in the OTP register. ECC is enabled after device power up, so the default PROGRAM and WRITE commands operate with internal ECC in the active state.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a single-bit data error is discovered, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful. Table 10 shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following considerations:

- Spare area definitions provided in Table 10 on page 30.
- WRITEs to the ECC bytes are prohibited.
- The user areas, defined as user main (0, 1, 2, and 3) area and user spare (0, 1, 2, and 3) area must be programmed within a single partial-page programming operation so the NAND device can calculate the proper ECC bytes.
- The user can perform a maximum of four partial-page programming operation within a page.

Table 10: ECC Protection

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data
3FFh	200h	Yes	Main 1	User data
5FFh	400h	Yes	Main 2	User data
7FFh	600h	Yes	Main 3	User data
800h	800h	No		Reserved
803h	801h	No		ECC bytes for spare area 0
806h	804H	Yes	Spare 0	ECC bytes for main area 0
807h	807h	Yes	Spare 0	Reserved
80Fh	808h	Yes	Spare 0	User meta data 0
810h	810h	No		Reserved
813h	811h	No		ECC bytes for spare area 1
816h	814h	Yes	Spare 1	ECC bytes for main area 1
817h	817h	Yes	Spare 1	Reserved
81Fh	818h	Yes	Spare 1	User meta data 1
820h	820h	No		Reserved
823h	821h	No		ECC bytes for area spare 2
826h	824h	Yes	Spare 2	ECC bytes for main area 2
827h	827h	Yes	Spare 2	Reserved
82Fh	828h	Yes	Spare 2	User data
830h	830h	No		Reserved
833h	831h	No		ECC bytes for area spare 3

Table 10: ECC Protection (continued)

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
836h	834h	Yes	Spare 3	ECC bytes for main area 3
837h	837h	Yes	Spare 3	Reserved
83Fh	838h	Yes	Spare 3	User data
FFFh	840h	No		Reserved

Table 11: ECC Status

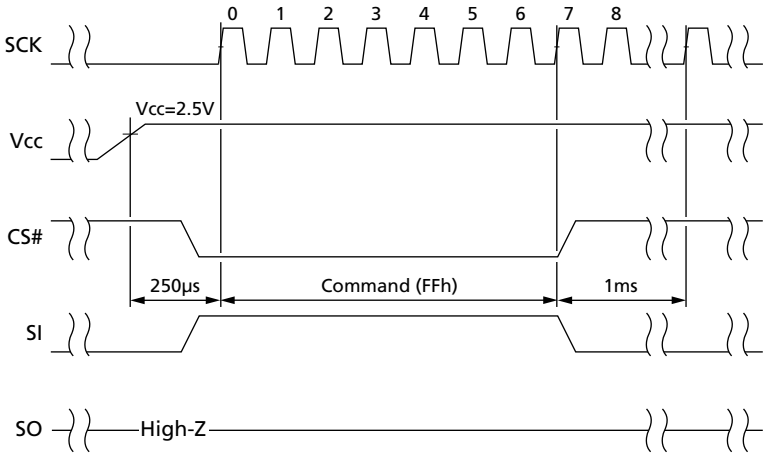
Bit 1	Bit 0	Description
0	0	No errors
0	1	One bit error detected and corrected
1	0	Multiple bit errors detected and not corrected
1	1	Reserved

Power-Up

Power-Up Timing

Micron NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored—when V_{CC} reaches 2.5V on a SPI device, a minimum of 250µs must elapse before issuing a RESET (FFh) command. A RESET must be issued as the first command after the device is powered on. After issuing the RESET command, 1ms must elapse before issuing any other command (see Figure 18).

Figure 18: Power-Up Timing



Electrical Specifications

Table 12: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{CC}	2.7	3.6	V
Operating temperature (ambient)	T_A	–40	85	°C
Junction temperature[1]	T_J		110	°C
Storage temperature	T_S	–40	125	°C

Notes: 1. T_J is calculated based on $T_J = R_{th} * P + T_{Ambient}$ with R_{th} = 180K/W.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 13: SPI Mode Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
SPI					
Supply voltage	V_{CC}	2.7	3	3.6	V
Supply current (READ/PROGRAM/ERASE, MAX ROOT MEAN SQUARE)	I_{CC}		25	35	mA
Standby	I_{SB}		10	50	µA

Table 14: DC Characteristics

Parameter	Symbol	Min	Max	Unit	Conditions
SO, SI, CS	V_{IH} V_{IL}	$0.7 \times V_{CC}$ -0.3	$V_{CC}+0.3$ $0.2 \times V_{CC}$	V	
	V_{OH} V_{OL}	$0.7 \times V_{CC}$	$V_{CC}+0.3$ $0.15 \times V_{CC}$	V	I_{OH} = -20µA I_{OL} = -1mA
Output load			30	pF	

Table 15: General Timing Characteristics

Parameter	Symbol	Min	Max
Clock frequency	^{t}C		50Mhz
Hold# non-active hold time relative to SCK	^{t}CD	5ns	
HOLD# time relative to SCK	^{t}CH	5ns	
Command deselect time	^{t}CS	100ns	
Chip select# hold time	^{t}CSH	5ns	
Chip select# setup time	^{t}CSS	5ns	
Output disable time	^{t}DIS		20ns
Hold# non-active setup time relative to SCK	^{t}HC	5ns	
Hold# setup time relative to SCK	^{t}HD	5ns	
Data input hold time	$^{t}HDDAT$	5ns	
Output hold time	^{t}HO	0ns	
Hold to output High-Z	^{t}HZ		15ns
Hold# to output Low-Z	^{t}LZ		15ns
Rise/fall time	^{t}R, ^{t}F		2ns
Data input setup time	$^{t}SUDAT$	5ns	
Clock LOW to output valid	^{t}V		15ns
Clock HIGH time	^{t}WH	8ns	
Clock LOW time	^{t}WL	8ns	
WP# hold time	^{t}WPH	100ns	
WP# setup time	^{t}WPS	20ns	

Table 16: PROGRAM/READ/ERASE Timing Characteristics

Parameter	Typ	Max	Description
NOP		4[1]	Number of partial-page programming operations supported.
^{t}ERS	4ms	10ms[2]	BLOCK ERASE operation time.
^{t}PROG	400ns	900µs	PROGRAM PAGE operation time (ECC enabled).
^{t}RD		100µs	Data transfer time from NAND Flash array to data register with internal ECC enabled.
^{t}RST (RD/PGM/ERS)		5µs/10µs/500µs[3]	Resetting time for READ, PROGRAM, and ERASE operations.

Notes: 1. Limited to one partial-page program when internal ECC is enabled. When internal ECC is disabled [or none is present], a maximum of four partial-page programs to the same page are supported.
2. 100,000 cycles.
3. For first RESET condition after power up, ^{t}RST will be 1ms max.

Figure 19: WP# Timing

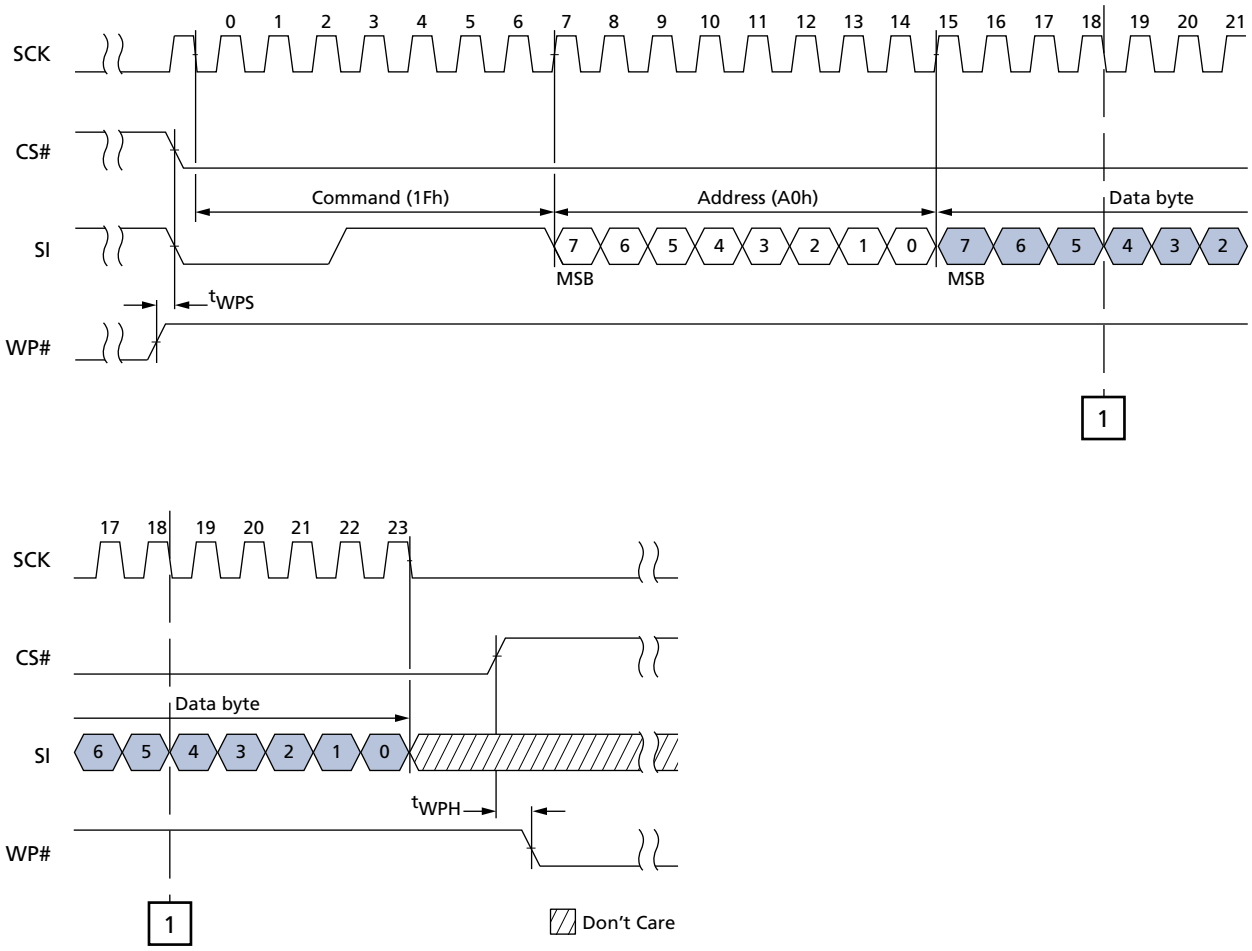


Figure 20: Serial Input Timing

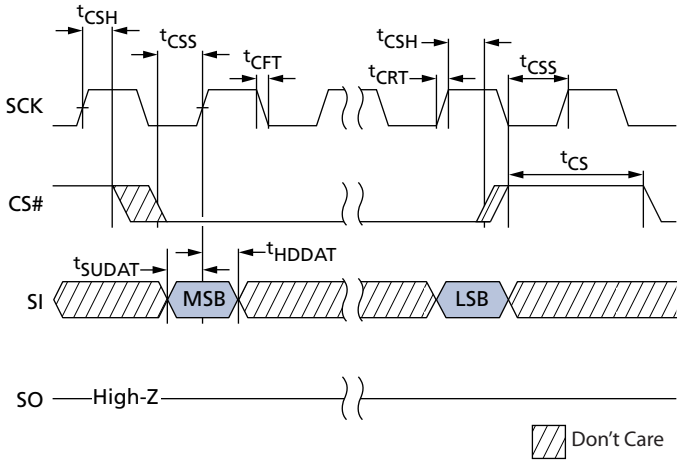


Figure 21: Serial Output Timing

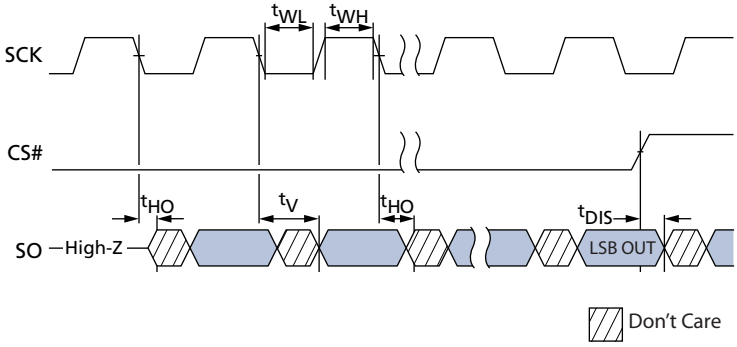
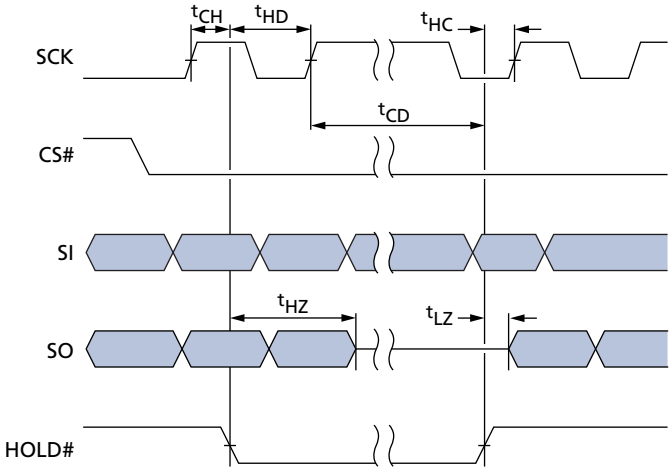
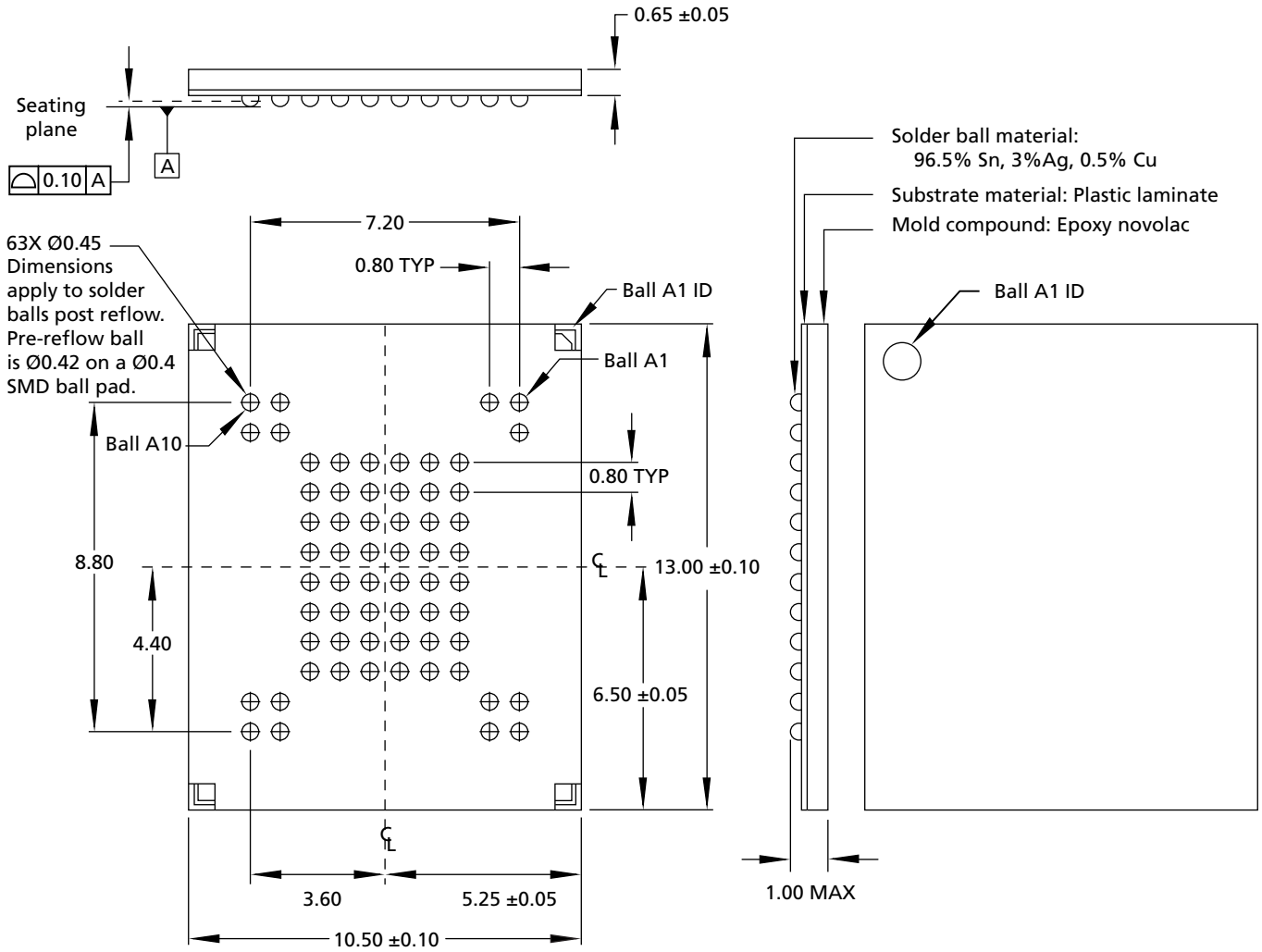


Figure 22: Hold# Timing



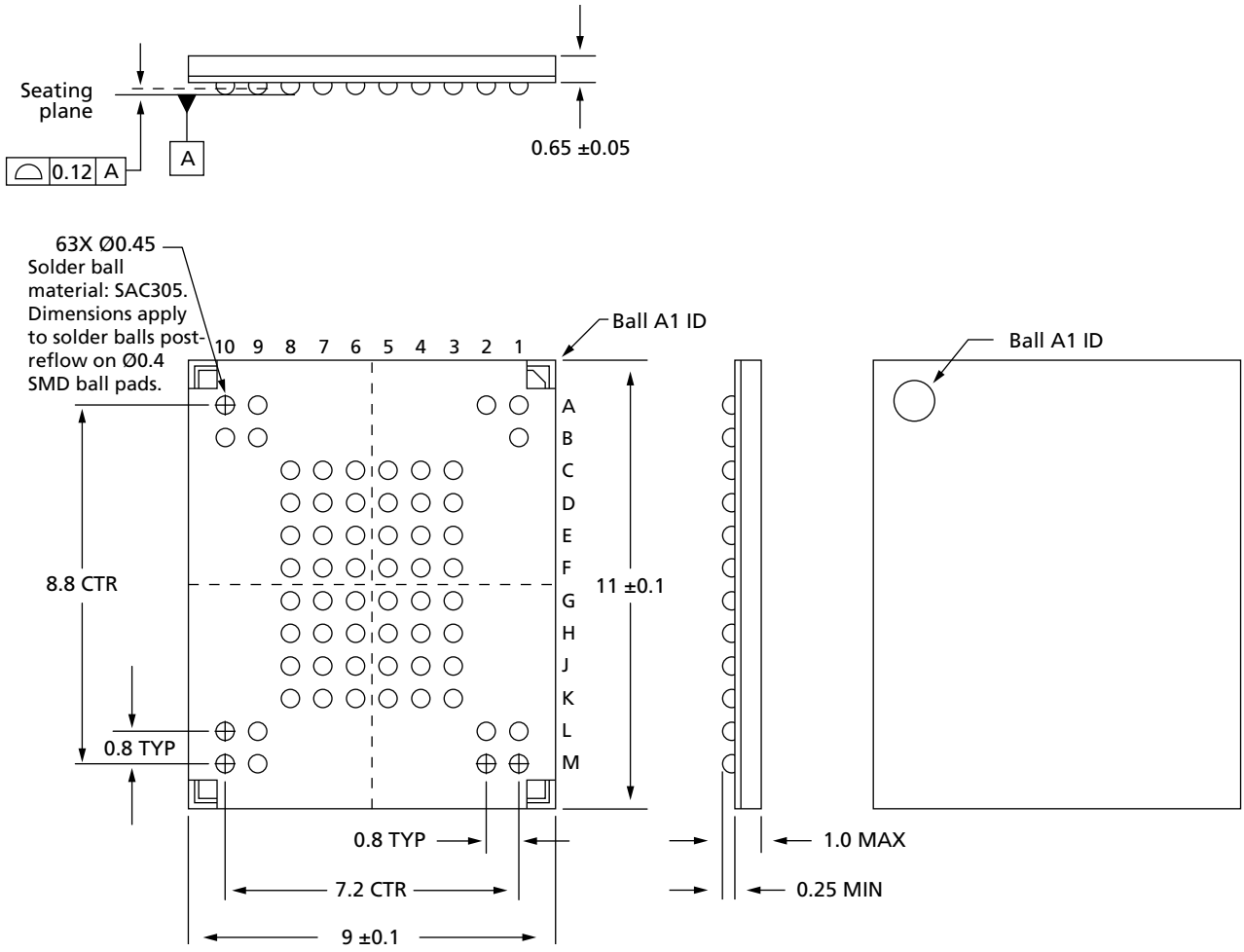
Package Dimensions

Figure 23: 63-Ball VFBGA Package (10.5mm x 13mm)



Notes: 1. All dimensions are in millimeters.
2. Available only for SPI.

Figure 24: 63-Ball VFBGA Package (9mm x 11mm)



Notes: 1. All dimensions are in millimeters.

Revision History

Rev. A, Production. 5/09

- "Options" on page 1: Under package, added dimensions and 9mm x 11mm part; added notes 1 and 2.
- Table 1, "SPI NAND Flash Parameters," on page 1: Conditionalized separate SPI and SPI-ER tables.
- Figure 1, SPI Part Number Chart, on page 2: Updated figure.
- "General Description" on page 6: Updated content.
- Table 2, "Ball Descriptions," on page 9: Per new standard, deleted ball assignments/location column; updated description column content.
- Figure 6, SPI Modes Timing, on page 11: Updated figure and added note.
- "HOLD#" on page 11: Deleted sentence referencing hold support unavailable for SPI-ER.
- "SCK" on page 11: Added last sentence.
- "SO Data Output" on page 12: Added output to heading.
- Figure 7, WRITE ENABLE (06h) Timing, on page 13: Updated figure.
- Figure 8, WRITE DISABLE (04h) Timing, on page 14: Updated figure.
- Figure 9, GET FEATURES (0Fh) Timing, on page 15: Updated figure.
- Figure 10, SET FEATURES (1Fh) Timing, on page 15: Updated figure.
- "PAGE READ (13h)" on page 16: Changed 1 to 2112 to 0 to 2111.
- Figure 11, PAGE READ (13h) Timing, on page 17: Updated figure and added note.
- Figure 12, RANDOM DATA READ (03h or 0Bh) Timing, on page 18: Updated figure.
- Figure 13, READ ID (9Fh) Timing, on page 19: Updated figure.
- "Page Program" on page 20: Deleted sentence referencing loading 528 bytes as a partial page.
- Figure 14, PROGRAM LOAD (02h) Timing, on page 21: Updated figure.
- Figure 15, PROGRAM EXECUTE (10h) Timing, on page 22: Updated figure.
- Figure 16, PROGRAM LOAD RANDOM DATA (84h) Timing, on page 23: Updated figure.
- "Block Lock Feature" on page 26: Changed "The block lock feature is not supported in SPI-ER devices" to "The BWRD feature is not supported in SPI-ER devices."
- Figure 17, BLOCK ERASE (D8h) Timing, on page 25: Updated figure.
- Table 6, "Block Lock Register Block Protect Bits," on page 26: Updated table headings and protected rows column contents.
- "One-Time Programmable (OTP) Feature" on page 26: Added bullet set and last paragraph.
- "OTP Access" on page 27: Added heading and content section.
- Table 7, "OTP States," on page 27: Updated table headings.
- Table 8, "Status Register Bit Descriptions," on page 27: Updated description column contents.
- "Error Management" on page 29: Added heading and content section.
- Table 9, "Error Management Details," on page 29: Added table.
- "ECC Protection" on page 30: Changed text references in first paragraph from WRITE to PROGRAM; added bulleted items as last paragraph.
- Table 10, "ECC Protection," on page 30: Changed column heading from sector to area; updated description column contents.
- Table 11, "ECC Status," on page 31: Added table.

- Table 13, “SPI Mode Electrical Characteristics,” on page 33: Removed supply current spikes row.
- Table 15, “General Timing Characteristics,” on page 34 and Table 16, “General Timing Characteristics,” on page 34: Deleted clock rise and fall times; changed clock HIGH time to HOLD# holding time relative to SCK.
- Table 16, “PROGRAM/READ/ERASE Timing Characteristics,” on page 35: Updated NOP max value to 4; added description column; updated note 3.
- Figure 18, Power-Up Timing, on page 32: Updated figure.
- Figure 19, Power-Up Timing, on page 32: Updated figure.
- Figure 19, WP# Timing, on page 35: Updated figure.
- Figure 23, 63-Ball VFBGA Package (10.5mm x 13mm), on page 37: Added dimensions to figure title.
- Figure 24, 63-Ball VFBGA Package (9mm x 11mm), on page 38: Added figure.
- Updated document status to Production.

Rev. 1.4, Advance 7/30/08

- Figure 1: “SPI Part Number Chart,” on page 2: Updated figure.
- “Block Lock Feature” on page 26: Updated description.
- Table 12, “Absolute Maximum Ratings,” on page 33: Added note superscript to junction temperature.

Rev. 1.3, Advance 7/16/08

- Figure 1: “SPI Part Number Chart,” on page 2: Deleted option A from operating voltage.
- “General Description” on page 6: Updated second part number in first sentence of second paragraph.
- “Ball Assignment 63-Ball VFBGA” on page 8: Updated figure title with SPI only.
- Figure 7: WRITE ENABLE (06h) Timing on page 13: Updated figure.
- Figure 8: WRITE DISABLE (04h) Timing on page 14: Updated figure.
- Figure 13: “READ ID (9Fh) Timing,” on page 19: Updated figure.
- Table 8, “Status Register Bit Descriptions,” on page 27: Updated P_Fail description.
- Figure 19: “Power-Up Timing,” on page 32: Updated figure.
- Table 12: Absolute Maximum Ratings on page 33: Deleted pulse voltage (ESD protection, all pins) parameter.

Rev. 1.2, Advance 7/10/08

- Entire document: Combined SPI and SPI-ER content.
- “Options” on page 1: Updated package description.
- Figure 1: SPI Part Number Chart on page 2: Updated figure.
- “Block Lock Feature” on page 26: Updated description.
- “One-Time Programmable (OTP) Feature” on page 26: Updated description.
- Table 7, “OTP States,” on page 27: Updated states.
- Table 8, “Status Register Bit Descriptions,” on page 27: Updated P_Fail description.
- Table 13, “SPI Mode Electrical Characteristics,” on page 33: Added peak supply current parameter for SPI and SPI-ER.

Rev. 1.1, Advance 6/3/08

- “Options” on page 1: Added packaging information.
- Figure 1: Part Number Chart on page 2: Updated figure with package code HC for 63-ball VFBGA.
- Figure 23: 63-Ball VFBGA Package (10.5mm x 13mm) on page 37: Added figure.

Rev. 1.0, Advance 4/08

- First draft.