SE4120L-AK1 Applications Board User Guide

REVISION HISTORY

Revision	Description of Changes	Revision Date
1.0	Initial QA approved release	Feb-05-2007
1.1	Updated with ENABLE control modification (see Board Modifications), and Test Measurement section referenced for use with the SE4120L-EK4 Evaluation Board.	Feb-22-2008

CONTENTS

1 Introduction

This document covers the specification, description, testing and operation of the SE4120L-AK1 Applications Board, and applies to boards with PCB No. Z142-A.

The SE4120L-AK1 Applications Board is a complete GPS radio front-end system with a range of parallel and serial, real IF and baseband I/Q data output options. The parallel data output modes are suited to hardware baseband implementations, and the serial data output modes allow interfacing to a microprocessor SPI port. There is a choice of GPS or Galileo filter bandwidths.

This applications board is intended to allow customer evaluation of the SiGe SE4120L GPS RFIC in a final form factor design. It supports a 16.368 MHz frequency plan and there are a number of powering options.

Interfacing is via a MMCX RF input connector and a 2 x 6-way 2 mm main connector.

For further details on the SE4120L itself, refer to the SE4120L datasheet [1].

2 Functional and Performance Specification

Parameter	Specification
Overall radio noise figure	2.4 dB (typical, includes 0.3 dB board losses)
Input return loss	6 dB (typical)
Data output	8.184 MSPS 2-bit I/Q pulse sync data output format[1]
IF output frequency	Near-zero IF
IF filter BW select	GPS[1] (Galileo)[2]
Clock output	16.368 MHz
TCXO reference frequency	16.368 MHz Tolerance: ±1.5 ppm Temperature (-40 to +85°C): ±0.5 ppm
Input supply voltage:	3.6 to 5.0 V
Digital I/O:	3.3 V[1] (1.7 V minimum)[2]
Current consumption	12.5 mA (typical, excluding antenna bias)
Active antenna bias:	
Supply voltage:	3.3 V[1] (typical) or 5 V[2] (max)
Short circuit current limit:	40 mA (typical), 300 mA max for 10 ohm load
RF input connector[1]	MMCX (jack)
Main connector	2 x 6-way 2 mm pin header

[1] For default board configuration

[2] Optional, dependent on board configuration

3 Description

3.1 Circuit Description

The SE4120L-AK1 circuit is a standard SE4120L application circuit using minimum external components for RF matching and supply decoupling, but with additional pull-up and pull-down resistors to configure the device in its various modes.

The board is configured for hardware programming of the SE4120L with a choice of four data output modes. It is set in this hardware configuration mode with the SE4120L HW pin (IC pin 20) tied high. These data output modes are in 2-bit or 4-bit I/Q serial data format at a near-zero IF frequency. The SE4120L has three hardware configuration pins (pins 12, 13, and 14) which set the data output mode, and IF filter bandwidth to either narrow (GPS) or wide (Galileo). These can be configured by resistive links.

For software programmed modes (SE4120L HW pin (IC pin 20) pulled low), the SE4120L is 3-wire software programmed via the three pins at the main connector. For simplicity, it can be configured by plugging it into a SE4120L-EK4 evaluation board USB platform.

The clock, data and sync outputs are routed to the main connector. For serial data output modes the sync output is used to identify the sample order, whereas for parallel data output modes it becomes a second data output, when applicable. For 4-bit parallel data output modes in software programming mode, two of the hardware configuration pins additionally become data outputs. The function of these two configuration pins in software programming mode is determined by the third configuration pin setting: as programming inputs when the third configuration pin is pulled low and as data outputs, when applicable, when the pin is high.

The SE4120L only supports 16.368 MHz frequency plan. Depending on the data output mode, the sample clock will be 16.368 MHz or a sub-harmonic of this, or an averaged sub-harmonic in the case of 'bursted' clock modes.

The SE4120L incorporates an AGC system with over 40 dB of gain control range. This maintains the internal MAG output high for about 33 % of the time. The AGC time constant is determined by external capacitor C6.

The SE4120L has been designed to operate under *worst case* conditions, whilst maintaining normal AGC operation, with a maximum of 32 dB excess noise at the mixer input, e.g. with a 1 dB noise figure active antenna with a gain of 31 dB. It is not advisable to operate the SE4120L with excessive gain ahead of the mixer because (in multi-bit modes) it will begin to operate in 1-bit mode, with a corresponding 1-2 dB increase in processing implementation loss, and with degraded interference immunity. The datasheet specifies a maximum signal load of -137 dBm/Hz at the mixer input for normal AGC operation. This is equivalent to -137 + 174 = 37dB excess noise under *typical* conditions. With the SE4120L LNA (18.5 dB typical gain) in circuit ahead of the mixer, therefore, the maximum recommended additional external gain is 12.5 dB (*worst case*) and 17.5 dB (*typical*).

The board is normally powered by a single 3.6 to 5.0 V supply which provides a supply for an external active antenna and is regulated down to 3.3 V for the SE4120L. With component changes the SE4120L can be powered directly, and the digital I/O can be separately powered by an external digital supply.

Active antenna bias short circuit current limit protection is provided by a fold-back current limit circuit internal to the LDO regulator.

The LNA input is matched with L4 and C7 (and optionally C2) for noise figure (NF) vs. input return loss trade-off. The input return loss is typically 5-6 dB for C7=1.5pF and 7 dB for C7=1.8pF. The noise figure is typically 0.15 dB better with 1.5pF than 1.8pF. A 1.5pF capacitor is fitted to the boards.

The LNA supply is locally decoupled with an 8.2pF capacitor (C5). This capacitor tunes out the parasitics in the supply line to maximize the gain at 1575 MHz, since the 'on-chip' LNA decoupling has been 'de-Q'd'. A second general purpose decoupling capacitor (C4) on the LNA supply line is isolated from C5 by

the series self resonant inductor L3 in order to avoid affecting the supply tuning. A 10nF capacitor across C5 is likely to produce an adjacent minor peak in the gain response, whilst a smaller value capacitor is more likely to short out the tuning affect of C8. Nevertheless, it is possible to replace L1 with a 0 R link with minimal affect on the LNA gain. It is possible to reduce the gain of the LNA by around 2 dB by increasing C5 to 100pF. This tends to improve the input return loss with only minor degradation to the LNA noise figure. This is a useful method for reducing the overall front-end gain when an additional external LNA is used ahead of the SE4120L.

A SAW filter has been fitted between the LNA output and mixer input to improve overall out of band blocking performance. The SAW has a typical insertion loss of 0.5 dB (0.8 dB max) and will increase the overall radio noise figure by about 0.05 dB. A higher attenuation SAW at this is point is unlikely to improve the overall blocking performance as it then becomes limited by the LNA stage.[1]

Also provided on the main connector is an enable line (ENABLE) for radio power control either using the LDO regulator enable or with an optional transistor switch.

The synthesizer loop filter consists of two components: R12 and C15.

3.2 Power Supply Options

The board is powered by a 3.6 V to 5.0 V supply to pin 2 of the main connector J2.

The SE4120L is designed to operate over the range 2.7 V to 3.6 V, with a digital I/O supply range down to 1.7V. Note that it is essential to continuously maintain *both* the radio VCC and digital I/O VDDN supplies for powered-up mode. With the power to the SE4120L removed, the power to any I/O lines should also be removed.

It is possible to reference the SE4120L digital interface pins 6 (AGC_DIS), 7 (VSSN), 8 (VDDN), 9 (CLK_OUT), 10 (DATA_OUT), 11 (SYNC), 12 (Fs_SEL0), 13 (Fs_SEL1), 14 (FILT_BW), 19 (OSC_EN) and 23 (RX_EN) to a separate digital supply with a minimum supply voltage of 1.7 V. In this case remove R26 and apply an external supply to pin 1 of J2.

Note: If R26 is fitted do not apply a supply to pin 1 of J2.

Note that the SE4120L digital interface pins RX_EN and OSC_EN are tolerant to the analog radio supply (2.7 to 3.6 V).

It is possible to feed in a raw VCC supply by removing the regulator U2 and fitting R22 = 0R (0603).

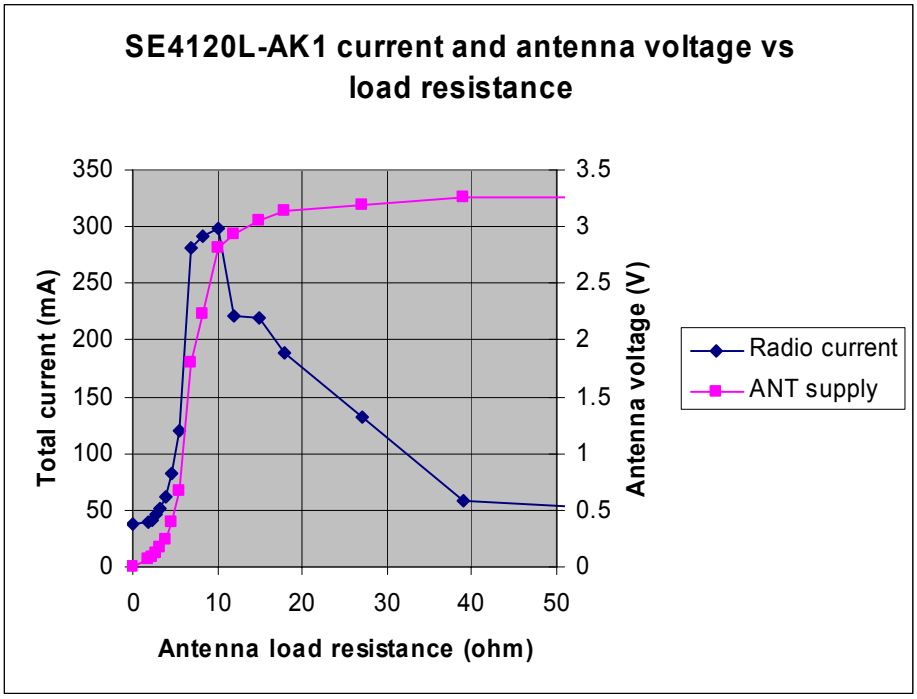
3.3 Active Antenna Supply

The antenna active bias supply can be configured with a resistor links. The default set-up is from the LDO regulator output. This affords current limit protection from the regulator. For powering from the higher raw supply voltage on pin 2 of J2, move the 0R link from position R27 to R26.

Short circuit antenna protection (typically 40 mA) is provided by the on-board Torex regulator. This regulator is specified for 150 mA current, but can source as much as 300 mA. Due to the nature of the MMCX connector it is possible to short the antenna supply to ground when inserting the MMCX plug of an external antenna. The resulting high instantaneous current can sometimes cause the 0402 multi-layer inductor choke L1 to fuse open circuit. It is sometimes prudent to fit a 0603 multi-layer choke with a higher current rating. For software programming of the SE4120L, an antenna short may result in the programmed data output mode being lost, requiring a reprogram.

[1] Note: The output of the LNA is internally DC blocked whilst the mixer input pin has a DC bias on it. It is advisable not to connect the LNA output directly to the mixer input without a DC blocking capacitor because the LNA output has 10K to ground at its output to reference the ESD diodes to 0 V. There would be a slight increase in mixer current as a result.

The plot below shows the total radio current vs. antenna load resistance. For a complete short circuit on the bias line the current is limited to around 40 mA. The maximum current is around 300 mA for a 10 ohm resistance to ground.



3.4 Power Management

The board is configured as fully active. Power control is via ENABLE on pin 7 of J2. The regulator is a useful means for powering down the SE4120L, TCXO and active antenna bias.

For power control of the board with a separate digital I/O there is a transistor switch for the TCXO supply. In this case fit TR1, and remove R25 and R23. This does not power down the antenna bias supply so it has limited use. Note also that the ENABLE line needs to be pulled high with a strong pull-up otherwise the SE4120L will remain powered down. (Strictly, the SE4120L RXENABLE should be routed to the output of the transistor switch).

OSCENABLE is tracked to the SE4120L ground flag so it is not possible to run the SE4120L in oscillator only mode with this circuit.

3.5 RF Input

The RF input is MMCX connector J1. This has DC bias for active antenna use. For RF measurements a DC block should used as a precaution to avoid short circuit conditions and potential damage to test equipment. Alternatively, inductor L1 can be removed.

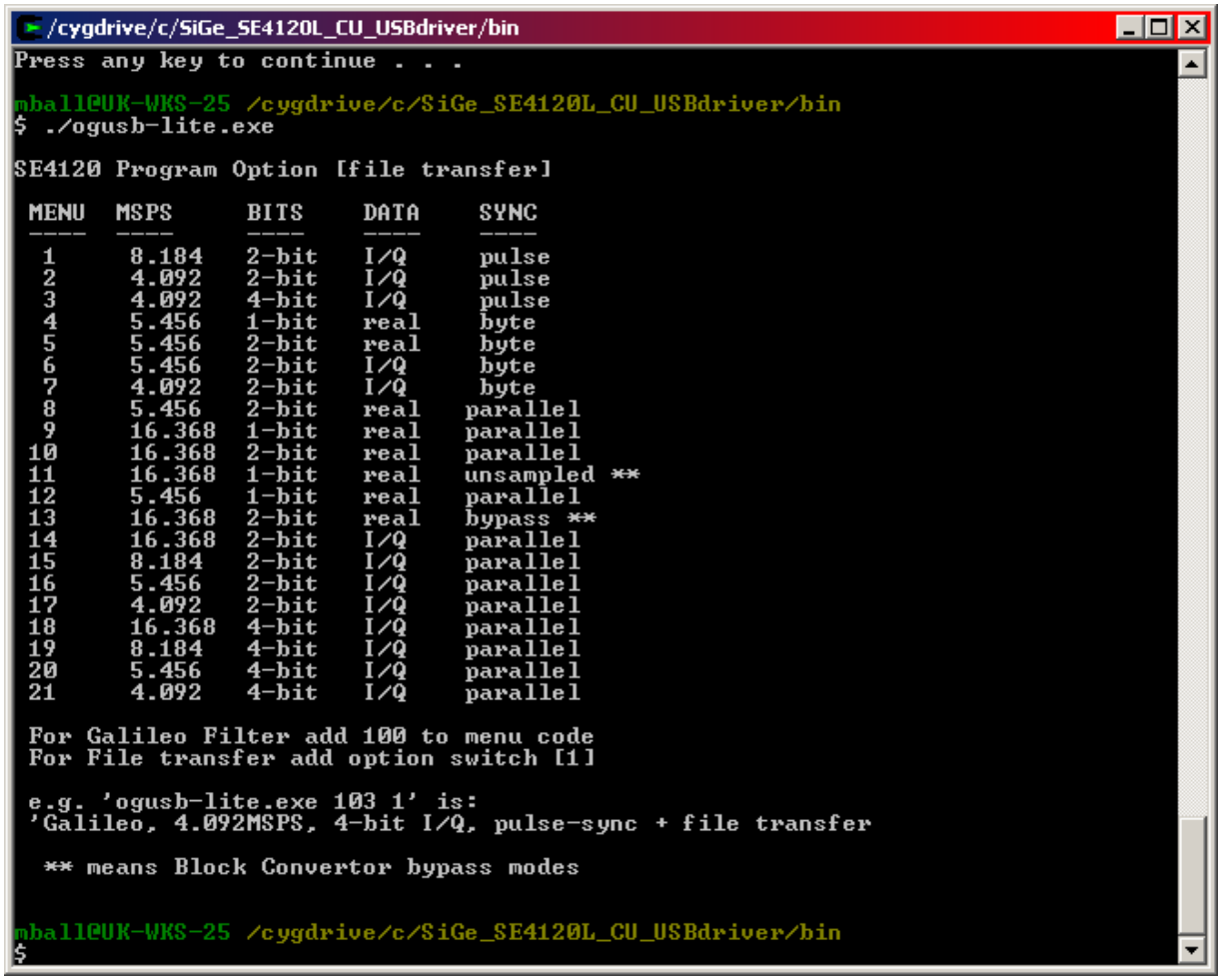
For an accurate measurement of the LNA or overall radio noise figure it is recommended to connect a short low-loss, SMA 'pig-tail' directly to the input of the LNA matching network.

3.6 Data Output Modes

3.6.1 Software Programming Mode

Software programming can be conveniently performed by plugging the SE4120L-AK1 board into a SE4120L-EK4 USB programming board, or else with the user's own proprietary 3-wire programmer. The 3-wire interface on the main connector is 3W_CLK (pin 10), 3W_DATA (pin 12) and 3W_ENB (pin 9).

The screen capture below shows the data output modes available from the SE4120L-EK4 programming perspective.



The SE4120L-EK4 USB programming board allows the SE4120L to be programmed into all of its data output modes, with either GPS or Galileo filter, and clock/data output drive set to maximum. For further information on programming, and the data output modes available in software mode, refer to the SE4120L-EK4 Evaluation Board User Guide [3] and the SE4120L Programming Guide [2].

Note that the SE4120L HW pin (IC pin 20) should be pulled low with a 'strong' pull-down (≤ 4.7K) to ensure that is in software programming mode. When using the SE4120L-EK4, a pull-down *should not* be fitted on the SE4120L-AK1 as one of the GPIOs on the SE4120L-EK4 is set to pull the HW pin low via J2 pin 11. In a final design it is convenient to route this to the ground flag. Meta-stable data output modes may occur if the HW pin is not pulled down correctly or if the 3-wire programming is not correct. A common symptom of this is a 'weak' clock output. There is no default data output mode in software mode and a mode must be explicitly programmed.

3.6.2 Hardware Programming Mode

The board is configured for hardware programming mode with the HW pin (IC pin 20) pulled high, i.e. R19=100K. For maximum output drive in hardware mode R19 (or R10) should be changed to 0R.

The table below shows data output modes available in hardware configuration mode. The data output mode is configured for four different modes by changing the pull-up / pull-down resistors on pins 12 and 13 of the SE4120L, Fs_SEL0 (3W_CLK) and Fs_SEL1 (3W_DATA) respectively.

Fs_SEL [1:0]	Data Output Sampling Rate	Data Output Format	Serial Output Format
00	8.184 MSPS	2 bit I/Q	Pulse
01	5.456 MSPS	2 bit I/Q	Byte
10	4.092 MSPS	2 bit I/Q	Byte
11	4.092 MSPS	4-bit I/Q	Pulse

Additionally, the pull-up / pull-down resistor on SE4120L pin 14 (FILT_BW (3W_ENB)), sets the IF filter bandwidth to either narrow (GPS) or wide (Galileo), see the table below.

FILT_BW (3W_ENB)	Filter Mode	Filter BW (MHz)
0	GPS	2.2
1	Galileo	4.4

Refer to the SE4120L datasheet [1] or SE4120L Programming Guide [2] for more information on hardware programming mode.

3.7 Loop Filter

The table below shows the recommended loop filter component values. These values have been chosen for minimum overall phase noise, and not for a minimum phase solution.

Fref (MHz)	Fcomp (MHz)	Main divider N	Fvco (MHz)	Charge pump (uA)	Loop BW (kHz)	C15 (pF)	R12
16.368	16.368	192	3142.656	100	245	220	33K

Note:

1) There is 16pF on-chip shunt capacitance internally between VTUNE and ground.
2) VCO tuning sensitivity assumed to be 120 MHz/V

3.8 Clock and Data Interfacing

The clock, data and sync outputs of the SE4120L are specified to drive up to 10pF load, the maximum standard CMOS input capacitance specification. GPS hardware basebands and applications processors with smaller geometry processes will tend to have much lower typical input capacitance than this. The PCB track interconnect capacitance needs to be additionally taken into account.

In software programming mode the output drive can be programmed between minimum and maximum output drive in four steps. Using the SE4120L-EK4 evaluation board, the output drive is set to maximum. The minimum and maximum output drives align with those for hardware programming mode.

In hardware programming mode the output drive is set by pull-ups R19 (or R10) on HW (IC pin 20). For 10pF load capacitance, ensure R19 (or R10) is be set to 0R. See the table below.

Current Setting Resistor Value (HW (Pin 20) to VDDQ (Pin 17)) (Ω)	**Maximum Allowable Capacitive Loading** (pF)	**Current Drive Level**
Not Fitted	5	Nominal
100K	6	X 1.2
39K	7	X 1.4
0R	10	X 2.0

It is possible to compute the absolute maximum load capacitance that can be driven by the slew rate limited outputs:

$C = I/(dV/dt) = I*\Delta T/\Delta V$

Where I = output drive current

V = minimum required voltage swing from supply rail to Vil or Vih

T = 0.5 * clock period

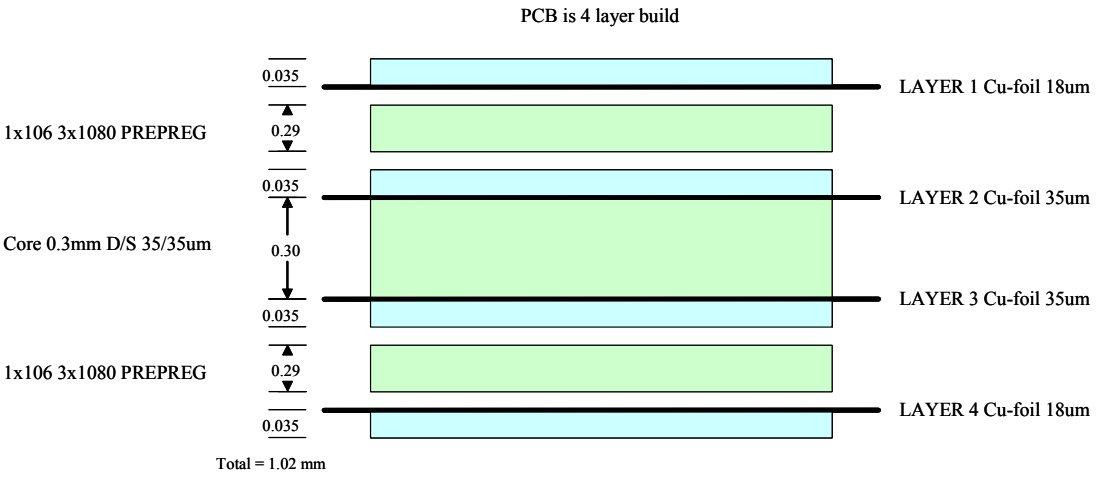
Note that there may be issues with jitter if the edges are slow, and the set-up and hold times may be significantly affected, though there should be adequate margin.

Sampled harmonics of the data outputs may fall in the 1575.42 MHz input band and cause de-sensitization of the radio front end. Care should be taken with data and clock output drive level, routing of any data or clock output cabling and RF input arrangements.

3.9 Board Layout

The PCB is 4-layer FR4, 1 mm thick, with tracking on layer 1 (component side) and layer 3, and ground fill on layer 2 and layer 4 (underside). The PCB lay-up is shown below. See Appendices for component placement and tracking layer plots.

1mm PCB build



PREPREG:
106 0.05 mm
1080 0.08 mm

Overall thickness approx 1.0mm

LAYER 1 and LAYER 4 are 35um after plating

THE ORDER OF THE LAYERS IS VITAL

Finish (for prototype builds) 3-5um Nickel, 0.03-0.05um gold

PCB dielectric is standard FR4, typical permittivity (Er) is 4.2 to 4.3

Note:
um = micron
Cu = copper
D/S = Double-sided

50 ohm track widths				
	Track layer	**GND layer(s)**	**mm**	**thou**
Microstrip	1	2	0.533	21
Stripline	3	2,4	0.203	8

4 Board Configuration

4.1 Connector Details

4.1.1 Main Connector (J2)

Pin No	Pin Name	Comment
1	P1V8	Digital I/O VDDN power supply (+1.7 V to analog VCC): Regulated output or optional input.
2	P3V6	+3.6 to +5 V main power supply input (for on board regulator)
3	GND	GND
4	CLK	Clock output
5	GND	GND
6	DATA	Data output
7	ENABLE	Radio enable (active high)
8	SYNC	Sync output
9	FILT_BW	HW mode: Filter BW select (GPS = low, Galileo = high) SW mode: 3-wire ENABLE
10	Fs_SEL0	HW mode: Data output mode select (Fs_SEL0) SW mode: 3-wire CLK
11	RVI / HW	Output drive setting pin Configures SE4120L into HW or SW mode. HW mode when N/C or pulled High SW mode when pulled low
12	Fs_SEL1	HW mode: Data output mode select (Fs_SEL1) SW mode: 3-wire DATA

4.2 Configuration with SE4120L-EK4

- Apply a GPS RF input to MMCX connector J1
- Refer to the SE4120L-EK4 Evaluation Board User Guide [3]

4.3 Configuration without SE4120L-EK4

- Apply a 3.6 to 5.0 V supply to J2 pin 2, and an RF input to MMCX connector J1.
- The CLK, DATA and SYNC outputs appear on pins 4, 6 and 8 of J2 respectively. The default configuration for the board is 8.184 MSPS 2-bit I/Q pulse sync mode. For other data output modes and IF filter bandwidth in hardware mode, change the configuration of the pull-up / pull-down resistors R13 to R18.
- For software programming mode, connect a 3-wire programming interface to Fs_SEL0 (pin 10), Fs_SEL1 (pin 12) and FILT_BW (pin 9) on connector J2.

5 Test Measurements

5.1 Test Equipment

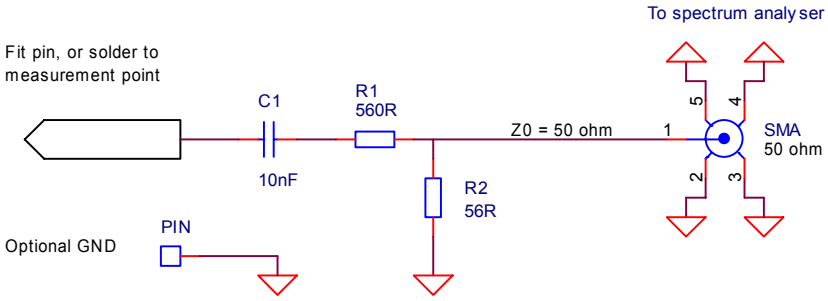
5.1.1 Requirements

The following equipment is recommended:

- SE4120L-EK4 Evaluation Board USB platform
- Power Supply (PSU) capable of delivering 60 mA, 5 V
- RF CW signal generator to 1.6 GHz
- DC block
- MMCX (male) to SMA (female) adaptor
- Spectrum analyzer (3.5 MHz to 1.6 GHz)
- Digital Multi Meter (DMM)
- RF probe
- Frequency counter (optional)
- Digital sampling scope
- GPS simulator (e.g. Spirent STR4500 12 channel simulator)
- Baseband platform (e.g. SE4120L-EK4 + host PC running software GPS)

5.1.2 RF Probe

The RF probe should be high impedance to avoid loading the point under test. Either a commercially available FET probe (e.g. Agilent 85024A) or a passive RF probe of the type shown below may be used. Care should be taken not to exceed the DC input specification of the commercial probes.



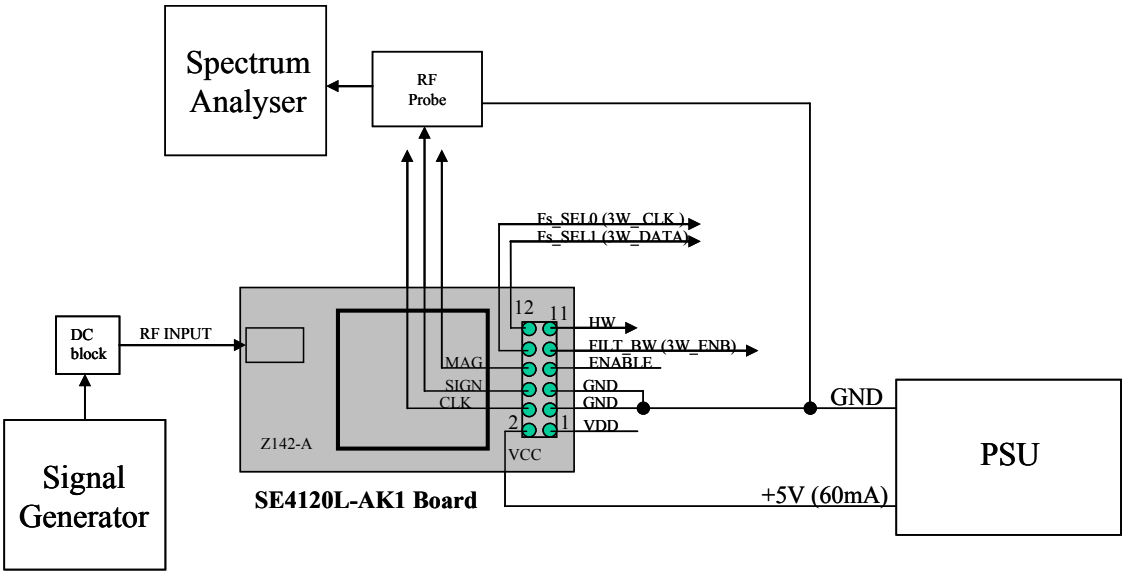
X10 RF probe with DC block

It is essential to have a good ground connection for this circuit when observing the SIGN and MAG output spectrum.

This probe will attenuate the output signal level by approximately 20 dB.

5.1.3 Board Configuration Setup

The diagram below shows a minimum configuration of the standalone SE4120L-AK1 for test purposes. The simplest solution to performing the tests described below is to plug the board via the main connector J2 into a SE4120L-EK4 evaluation board.



SE4120L-AK1 Interfacing

5.1.4 SIGN and MAG Related Measurements

The CLK, SIGN and MAG related measurements in subsequent sections assume that the SE4120L-AK1 has been programmed into 2-bit SIGN/MAG real, parallel data output mode at 16.368 MHz, with the CLK in a continuous, non-bursted mode. This corresponds to the normal SE4110 data output mode.

For simplicity it is recommended that the SE4120L-EK4 evaluation board is used to program the SE4120L-AK1 board into this data output mode (Menu selection 10). The SE4120L-EK4 evaluation board has the probe 'pot-down' circuit integrated on-board to facilitate CLK, SIGN and MAG testing. For more details refer to the SE4120L-EK4 Evaluation Board User Guide [3].

5.2 Test Items

The test list and expected values are itemized below:

Measurement	Test procedure	Test Point	Expected value	Lower limit	Upper limit	Unit	Comments
Supply current	5.4	-	12.5	10	14	mA	Dependent on clock and data output loading
Control voltage	5.5	TP1	1.4	1.0	1.8	V	
AGC voltage	5.5	TP2	1.2	0.9	1.5	V	No RF connection
Mixer bias	5.5	TP3	0.36	0.32	0.40	V	
LNA bias	5.5	TP4	0.82	0.76	0.89	V	
Antenna current limit	5.6	J1	31.5	29	34	mA	Antenna shorted to GND
CLK output level	5.7	J2 pin 4	-15	-22	-10	dBm	With RF probe or EK4
CLK freq	5.7	J2 pin 4	16.368	16.3679	16.3681	MHz	Determined by TCXO
AGC range (no RF input)	5.8	TP2	1.2	0.9	1.5	V	
AGC range (-88 dBm in)	5.8	TP2	0.8	0.5	1.1	V	
MAG duty cycle (no RF input)	5.8	J2 pin 8	33	30	37	%	
MAG duty cycle (-88 dBm in)	5.8	J2 pin 8	36	32	42	%	
MAG output level	5.9	J2 pin 8	-15	-25	-10	dBm	With RF probe or EK4
SIGN output level	5.9	J2 pin 6	-15	-25	-10	dBm	With RF probe or EK4
CLK, SIGN, MAG visual check	5.10	J2 pins 4, 6, 8	-	-	-	-	Visual check
SIGN and MAG output spectrum	5.11	J2 pins 6, 8	-	-	-	-	Visual check (see expected plot)
NF: 3 dB down test	5.12.3	J2 pin 6	2.4	1.8	3.0	dB	Referred to J1
NF: CNR system test	5.13	-	2.4	1.8	3.0	dB	Referred to J1. Requires a baseband platform.

5.3 RF Calibration

The connector plus track loss from the RF input connector J1 to the input of the LNA matching network is 0.3 dB. This should be taken into account when determining the overall noise figure of the radio, but is less important for other measurements.

All RF levels specified below are referenced the RF input connector J1.

5.4 Supply Current

1) Connect a 5 V DC supply to pin 2 of main connector J2 and ground pin 3 as shown above. Ensure the current limit of the supply is set to 60 mA to minimize accidental damage. All other connector pins should be left open circuit.
2) Measure the current consumption with a calibrated PSU reading or use a DMM in series. (Beware that a series ammeter may drop several hundred millivolts). The 5 V supply is required for all subsequent measurements.

If a SE4120L-EK4 evaluation board is available, a DMM can be inserted between pins 2 and 3 of JP7. Alternatively, connect a calibrated PSU between pins 2 (+5V) and 3 (GND) of JP7. Note there will be some increase in current due to the additional loading on the clock and data outputs compared with the standalone measurement above.

5.5 DC Conditions

Measure the bias voltages with a DMM on the following test points to verify correct DC operation:

1) TP1: Synthesizer control voltage
2) TP2: AGC voltage (no RF input)
3) TP3: Mixer bias voltage
4) TP4: LNA bias voltage

5.6 Antenna Current Limit

1) Fit a MMCX to SMA adapter onto J1, followed by SMA to BNC adapter and BNC to double 4 mm plug adapter.
2) Connect a DMM across the 4 mm plug adapter set to measure current.
3) Measure the antenna current, allowing time for the current reading to stabilize if necessary.

The total current consumption from the PSU with maximum antenna bias current should be approx 44 mA.

5.7 CLK Output Level and Frequency

This measurement checks the level and frequency of the CLK output. See Section 5.1.4 for details of how to configure the board into the appropriate CLK, SIGN and MAG mode.

1) Probe J2 pin 4 using an RF probe connected to a spectrum analyzer set to 16.368 MHz centre frequency and measure the level of the CLK tone. Alternatively using a SE4120L-EK4, connect SMA J103 directly to the spectrum analyzer and fit jumper J102 5<>6.
2) Using frequency counter function on the analyzer, measure the frequency of the CLK tone, setting the counter resolution if necessary (N.B. a 10 Hz resolution should give 5 decimal places).
3) Alternatively, use the RF probe and a standalone frequency counter with sufficient sensitivity.
4) In both cases ensure that the reference standard in the instrument has sufficient stability for the measurement accuracy required.

5.8 AGC Range and MAG Duty Cycle

5.8.1 Measurement

This measurement checks the AGC and MAG operation over the normal AGC range. See Section 5.1.4 for details of how to configure the board into the appropriate CLK, SIGN and MAG mode.

1) Ensure a DC block is fitted between J1 and any test equipment
2) Connect a signal generator at 1575.42 MHz (CW) to J1.
3) With the source output switched off, measure the AGC voltage on TP2. The AGC should set the gain of the internal VGA close to maximum. This result should be similar but slightly lower than in section 5.5 because in this case the RF input has been terminated in 50 ohm rather than left open circuit.
4) Measure the MAG DC voltage on J2 pin 8 using a DMM. The MAG duty cycle is given by (V_{MAG}/VCC)*100%, where VCC = 3.3 V.
5) Set the source to deliver -88 dBm at J1. Measure the AGC voltage on TP2. The AGC should set the gain of the internal VGA close to minimum, i.e. the VGA is still operating within the linear range of the AGC.
6) Re-measure the MAG voltage and calculate the MAG duty cycle.

5.8.2 Theory

The MAG duty cycle should be 33% over the normal AGC range, though will increase somewhat at the high input level end of the range.

The maximum specified MIX_IN input signal level for AGC for normal operation is -137 dBm/Hz.

For 2.2 MHz IF BW, this is equivalent to an input tone at the LNA input of

$$-137 + 10\log(2.2\times10^{6}) - 15 = -88.6 \text{ dBm}.$$

The LNA gain is assumed to be 15 dB to take into account PCB input track loss and present a slightly worse case condition.

5.9 SIGN and MAG Output Level

This measurement checks the level of the SIGN and MAG outputs. See Section 5.1.4 for details of how to configure the board into the appropriate CLK, SIGN and MAG mode.

1) Ensure a DC block is fitted between J1 and any test equipment
2) Connect a signal generator at 1575.42 MHz (CW) set to deliver -75 dBm at J1.
3) Using an RF probe connected to a spectrum analyzer measure the tone amplitude at the following points. Alternatively using a SE4120L-EK4, connect SMA J103 directly to the spectrum analyzer and fit the appropriate J102 jumper.
4) Measure the MAG amplitude at J2 pin 8, with analyzer centre frequency set to 8.184 MHz (i.e. 2 x 4.092 MHz). Note that two peaks will appear if the frequencies of the RF input, applications board reference and spectrum analyzer are not locked together. If necessary finely adjust the signal generator frequency until the peaks coincide.
5) Measure the SIGN amplitude at J2 pin 6 (or fit jumper J102 3<>4 on the SE4120L-EK4), with analyzer centre frequency set to 4.092 MHz.

5.10 CLK/SIGN/MAG Waveform Check

This measurement checks the CLK, SIGN and MAG outputs using a scope. See Section 5.1.4 for details of how to configure the board into the appropriate CLK, SIGN and MAG mode.

1) Ensure a DC block is fitted between J1 and any test equipment.
2) Connect a signal generator at 1575.42 MHz (CW) to J1.

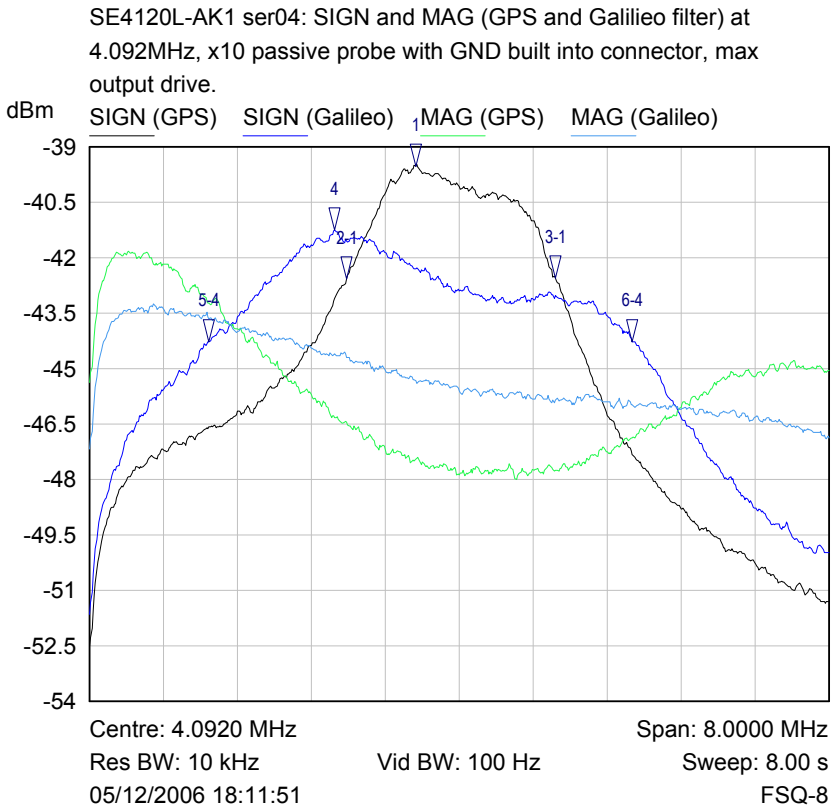
3) Connect a digital sampling scope to monitor CLK, SIGN and MAG with X10 probes on pin 4, pin 6 and pin 8 of J2 respectively (ensuring that the pins are not shorted together). Set the scope to trigger on SIGN.

4) With the source output switched off, verify that the three waveforms are present with pk-pk amplitude of about 3.3 V. CLK should be 50% duty cycle, SIGN a PRBS waveform also with 50% duty cycle and MAG a PRBS waveform of approx 33% duty cycle.

5) Set the source to deliver -75 dBm at J1. Verify that the three waveforms are present with pk-pk amplitude of about 3.3 V. The SIGN output should now be a periodic 50% duty cycle waveform. The MAG duty cycle may be higher than 33%, but at this input level it is undefined.

5.11 SIGN and MAG Output Spectrum

This measurement is an optional sanity check for the SIGN and MAG output spectrum. See Section 5.1.4 for details of how to configure the board into the appropriate CLK, SIGN and MAG mode. Below is a typical plot of the SIGN and MAG output spectrum for the SE4120L-AK1 for both GPS and Galileo filters.



Mkr	Trace	X-Axis	Value	Notes
1	SIGN (GPS)	3.6176 MHz	-39.53 dBm	
2-1	SIGN (GPS)	-0.7436 MHz	-3.04 dB	
3-1	SIGN (GPS)	1.5128 MHz	-3.01 dB	
4	SIGN (Galileo)	2.7458 MHz	-41.25 dBm	
5-4	SIGN (Galileo)	-1.3590 MHz	-3.02 dB	
6-4	SIGN (Galileo)	3.2179 MHz	-3.04 dB	

Peaking in the SIGN filter response shape indicates EMC feed-round of SIGN harmonics at 1575.42 MHz into the LNA input. For a proven board design, peaking is only likely to occur if there is a circuit board fault. The feed-round within the SE4120L itself is not significant. Note the IF filters naturally have a slight downward slope across the pass-band with increasing frequency. The MAG output has no components at 4.092 MHz and therefore does not contribute to any EMC effects.

It is recommended that this measurement is made using either the SE4120L-EK4 evaluation board, or the passive RF probe circuit described in Section 5.1.2 above, built onto a crimp socket which also powers the board. It is essential to have a GND connection otherwise the GND bounce may distort the result causing a distorted MAG spectrum to be supposed on the SIGN output. Ensure the spectrum analyzer is not overloaded before the video BW is reduced from the auto setting, otherwise the filter response may be compressed.

5.12 Overall RF Noise Figure using 3 dB Down Method

This measurement determines the overall noise figure from RF input to data output using the 3 dB down method. Some means of extracting the SIGN output is required to measure this correctly. See Section 5.1.4 for details of how to configure the board into the appropriate CLK, SIGN and MAG mode.

5.12.1 Measurement

1) Ensure a DC block is fitted between J1 and any test equipment.
2) Connect a signal generator at **1575.52** MHz (CW), i.e. +100kHz offset from 1575.42 MHz, set to deliver -75 dBm at J1.
3) Using an RF probe connected to a spectrum analyzer probe the SIGN amplitude at J2 pin 6. Alternatively using a SE4120L-EK4, connect SMA J103 directly to the spectrum analyzer and fit the jumper J102 3<>4.
4) Set the spectrum analyzer to **4.192** MHz centre freq, 10 kHz span, 3 kHz RBW, 30 Hz VBW, ref level –15 dBm, scale 1 dB/div. If necessary set the tone peak to centre frequency and adjust the reference level. Ensure the analyzer is not overloaded prior to reducing the VBW from the auto setting.
5) Measure the tone amplitude using the peak marker.
6) Select marker delta, or use another equivalent marker function. Reduce the signal generator output power until the SIGN amplitude drops by exactly 3 dB. Averaging is recommended to get a steady reading.
7) NF_{RX} = Rfin + 110.6 dB (At J1, assuming all cable losses have been accounted for)

5.12.2 Theory

With a large RF signal input applied to the SE4120L beyond the range of the AGC, the device behaves as though it is in 1-bit limiter mode. In this mode, the backend acts like a saturated amplifier and the overall gain is lower than the sum of the individual gain stages.

With a **1575.52** MHz input tone, of for example -75 dBm, the SIGN output is a saturated **4.192** MHz tone and the noise is suppressed.

If the input tone level is reduced so that the SIGN output tone fails by 3 dB, then the input noise power must be equal to the input signal power to maintain saturation, i.e. the signal and noise powers add to give the same total input power.

The noise power in the channel BW is given by

$$-174 \text{ dBm/Hz} + 10\log(\text{BW}) + NF_{RX}$$

Assuming the IF has a 3 dB BW of 2.2 MHz, the overall noise figure at J1 is given by:

$$NF_{RX} = \text{Rfin} - (-174 + 10\log(2.2e6))$$
$$= \text{Rfin} - (-174+63.4)$$
$$= \text{Rfin} + 110.6$$

Strictly, to put the SE4120L in 1-bit (limiter) mode the VAGC pin should be tied high (> 2 V) to ensure maximum gain at all times, but the 3 dB down measurement works well without this as the radio is either saturated by the tone, or the gain (with no tone input) is close to max anyway, i.e. the AGC operation does not distort the result.

Note also that the 3 dB BW of the IF channel filter within the SE4120L varies from part to part.

5.12.3 Measurement Correction

In order to get an accurate measurement it may be necessary to calibrate the set-up. Even if cable loss has been corrected for, the signal generator output level calibration may not be very accurate at these low levels. The following method uses a measurement with and without a calibrated LNA (with known noise figure and gain) placed ahead of J1. It takes out the uncertainties of cable loss, signal generator accuracy and actual IF filter bandwidth.

1) Ensure a DC block is fitted between J1 and any test equipment.
2) Select an accurately calibrated LNA or use a noise figure meter to measure noise figure and gain (preferred). Ideally the LNA should have a gain of >12 dB, and a noise figure of < 2 dB to ensure that the radio noise figure has negligible effect on the overall noise figure with LNA in front, making the correction easier to verify.
3) Perform the 3 dB down measurement with the LNA in front of the radio and record $Rfin_{RX+LNA}$. Ensure all cable losses are accounted for to verify the final result.
4) Repeat the 3 dB down measurement for the radio alone and record $Rfin_{RX}$. Again ensure all cable losses are accounted for to verify the final result.
5) The corrected radio noise figure can be calculated from the following three equations:

$$NF_{RX+LNA} = Rfin_{RX+LNA} - x + 110.6$$

$$NF_{RX} = Rfin_{RX} - x + 110.6$$

$$NF_{RX+LNA} = 10\log((10^{(NF_{RX}/10)} - 1) / (10^{(G/10)}) + 10^{(NF/10)}) \quad \text{cascaded NF calculation}$$

Where x = correction factor for signal generator output

G = measured gain of external LNA

NF= measured noise figure of external LNA

Solving this in spreadsheet format gives:

$$NF_{RX} = 10*LOG((10\text{^}((G+NF)/10)-1)/((10\text{^}((Rfin_{RX+LNA}-Rfin_{RX}+G)/10))-1))$$

For multiple board measurements during the same measurement session it is possible just to apply the correction factor from the first measurement provided the external LNA has high gain and low noise figure, and the resulting NF_{RX} are all typical. The correction factor for the first measurement is given by:

$$x = (Rfin_{RX+LNA}+110.6)-(10*LOG((10\text{^}(NF_{RX}/10)-1)/(10\text{^}(G/10)) + 10\text{^}(NF/10)))$$

5.12.4 SE4120L Cascaded Noise Figure Calculation

It is possible to accurately and independently measure the LNA noise figure and gain, and the backend (mixer input to SIGN output) 3 dB down noise figure, and use these results to compute the theoretical overall SE4120L noise figure. This requires a short SMA 'pig-tail' located between the LNA output and mixer input, and another at the LNA matching network input. All cable losses need to be corrected for.

Cascaded NF equation:

$$NF_{RX} = 10*LOG((10\text{^}(NF_{backend}/10)-1)/(10\text{^}(G_{LNA}/10))+ 10\text{^}(NF_{LNA}/10))$$

Assuming all losses have been accounted for, the cascaded calculation and the overall measured result should correspond, as the interference effects are negligible.

Comparing noise figure measurements between those with an SMA 'pig-tail' at the input of the LNA matching network and those at J1, it has been determined that the correction factor between these points is 0.3 dB. This mainly accounts for the associated loss of the PCB tracking and MMCX connector, but there is also a small contribution due to mismatches which degrade the LNA noise match. For accurate

measurement of the LNA and overall SE4120L noise figure it is recommended to use an SMA 'pig-tail' at the LNA matching network.

The table below helps to summarise typical results for cascaded noise figure calculation and measured 3 dB down results for various inter-stage SAW (F1) and LNA matching capacitor (C7) combinations:

C7 (pF)	SAW filter loss (F1) (dB)	LNA			Calculated overall NF (dB)	Rfin (expected) (dBm)	Overall NF	
		NF (dB)	Gain (dB)	i/p RL (dB)			At J1 (dB)	Pig-tailed LNA (dB)
1.5	0	1.65	18.0	5.5	2.05	-108.23	2.35	2.05
1.5	0.5	1.65	18.0	5.5	2.11	-108.17	2.41	2.11
1.8	0	1.80	18.5	7.0	2.15	-108.13	2.45	2.15
1.8	0.5	1.80	18.5	7.0	2.20	-108.08	2.50	2.20

Assumptions: Thermal noise floor = -174 dBm/Hz

IF filter BW = 2.2 MHz

Backend noise figure = 10 dB

Losses between J1 and LNA input matching network = 0.3 dB

Note: the SE4120L-AK1 is fitted with C7=1.5pF

5.13 Overall RF Noise Figure using a Baseband

5.13.1 Measurement

A third party baseband with known implementation loss can be used to determine the overall RF noise figure of the radio using a calibrated GPS source. It is possible to run a third party software GPS solution using the SE4120L-EK4 evaluation board and host PC. The SE4120L would need to be software programmed to the appropriate data output mode, typically 2-bit SIGN/MAG real, parallel mode at 16.368 MHz for the hardware baseband, and 2-bit SIGN/MAG real, parallel mode at 5.456 MHz for the SE4120L-EK4 USB platform.

Note that it may take time for the system to acquire satellites and achieve a fix, though the process can be speeded up by sending NMEA commands to preset the time, date, position and oscillator frequency, or by battery back-up of the almanac and ephemeris from a previous fix.

1) Ensure a DC block is fitted between J1 and any test equipment.
2) Set the simulator level for -130 dBm at RF input J1.
3) Record the average CNR reading over all satellites.
4) NF_{RX} = 44 – CNR – (implementation loss of baseband)

5.13.2 Theory

The overall noise figure at J1 is given by:

NF_{RX} = (Rfin – CNR) – (thermal noise) – (implementation loss of baseband)

= (-130 – CNR) + 174 – (implementation loss of baseband)

= 44 – CNR – (implementation loss of baseband)

(To refer this result to the LNA input matching network apply 0.3 dB correction factor).

The reported CNR value may not be the true absolute CNR in dB/Hz, and may not have the digital implementation loss factored in. Typically the baseband implementation loss will be 0-3 dB, depending on whether it is factored into the CNR or not.

Note there is a theoretical 0.6 dB advantage for 2-bit implementation over 1-bit at 16.368 MHz using ideal correlators for the complete RF + baseband system. In practice this may be 1-2 dB.

5.13.3 Measurement Correction

To calibrate the measurement for CNR reading and baseband implementation loss a measurement with an LNA in front can be used as described in the previous section.

1) Ensure a DC block is fitted between J1 and any test equipment.
2) Select an accurately calibrated LNA or use a noise figure meter to measure noise figure and gain (preferred). Ideally the LNA should have a gain of >12 dB, and a noise figure of < 2 dB to ensure that the radio noise figure has negligible effect on the overall noise figure with LNA in front, making the correction easier to verify.
3) Perform the CNR measurement with the LNA in front of the radio and record CNR_{RX+LNA}. Ensure all cable losses are accounted for to verify the final result.
4) Repeat the CNR measurement for the radio alone and record CNR_{RX}. Again ensure all cable losses are accounted for to verify the final result.
5) The corrected radio noise figure can be calculated from the following three equations:

$NF_{RX+LNA} = 44 - CNR_{RX+LNA}$ – (implementation loss of baseband) – x

$NF_{RX} = 44 - CNR_{RX}$ – (implementation loss of baseband) – x

$NF_{RX+LNA} = 10\log((10^{(NF_{RX}/10)} - 1) / (10^{(G/10)}) + 10^{(NF/10)})$ cascaded NF calculation

Where x = correction factor for reported CNR and implementation loss

G = measured gain of external LNA

NF= measured noise figure of external LNA

Solving this in spreadsheet format gives:

NF_{RX} = 10*LOG((10^((G+NF)/10)-1)/((10^((CNR$_{RX}$-CNR$_{RX+LNA}$+G)/10))-1))

For multiple board measurements during the same measurement session it is possible just to apply the correction factor from the first measurement provided the external LNA has high gain and low noise figure, and the resulting NF_{RX} are all typical. The correction factor for the first measurement is given by:

x = (44-CNR_{RX+LNA})-(10*LOG((10^(NF_{RX}/10)-1)/(10^(G/10)) + 10^(NF/10)))

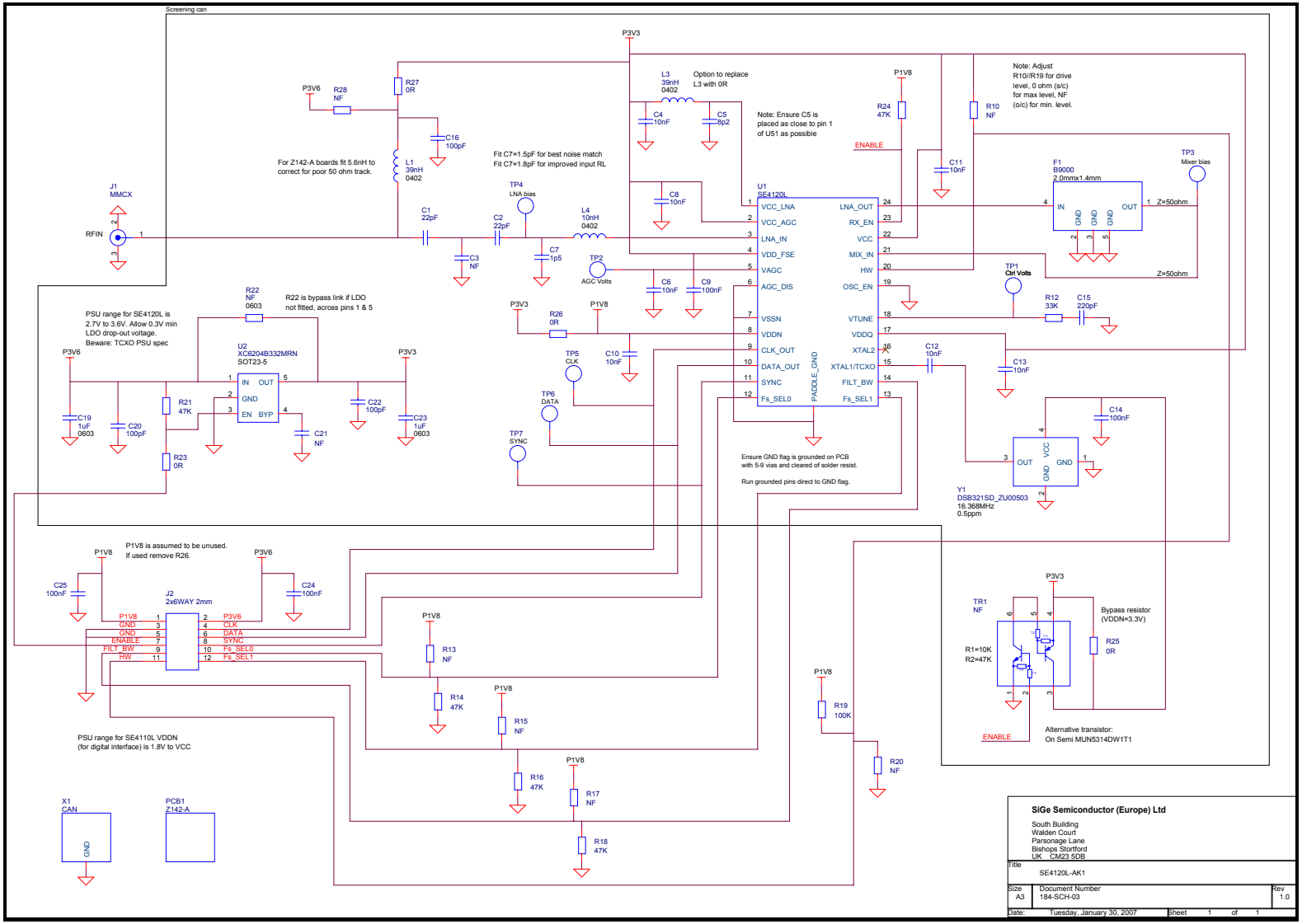
6 References

[1] SE4120L PointChargerTM GNSS Receiver IC, 184-DST-01, Rev 3.2, Oct-18-2007

[2] SE4120L Programming Guide, 184-DOC-08, Rev 2.0, Mar-27-2007

[3] SE4120L-EK4 Evaluation Board User Guide, 184-DOC-18, Rev 1.0, Jul-03-2007

Appendix A: Schematic



Appendix B: Bill of Materials

SE4120L-AK1 Revised: Tuesday, January 30, 2007
184-SCH-03 Revision: 1.0

SiGe Semiconductor (Europe) Ltd
South Building
Walden Court
Parsonage Lane
Bishops Stortford

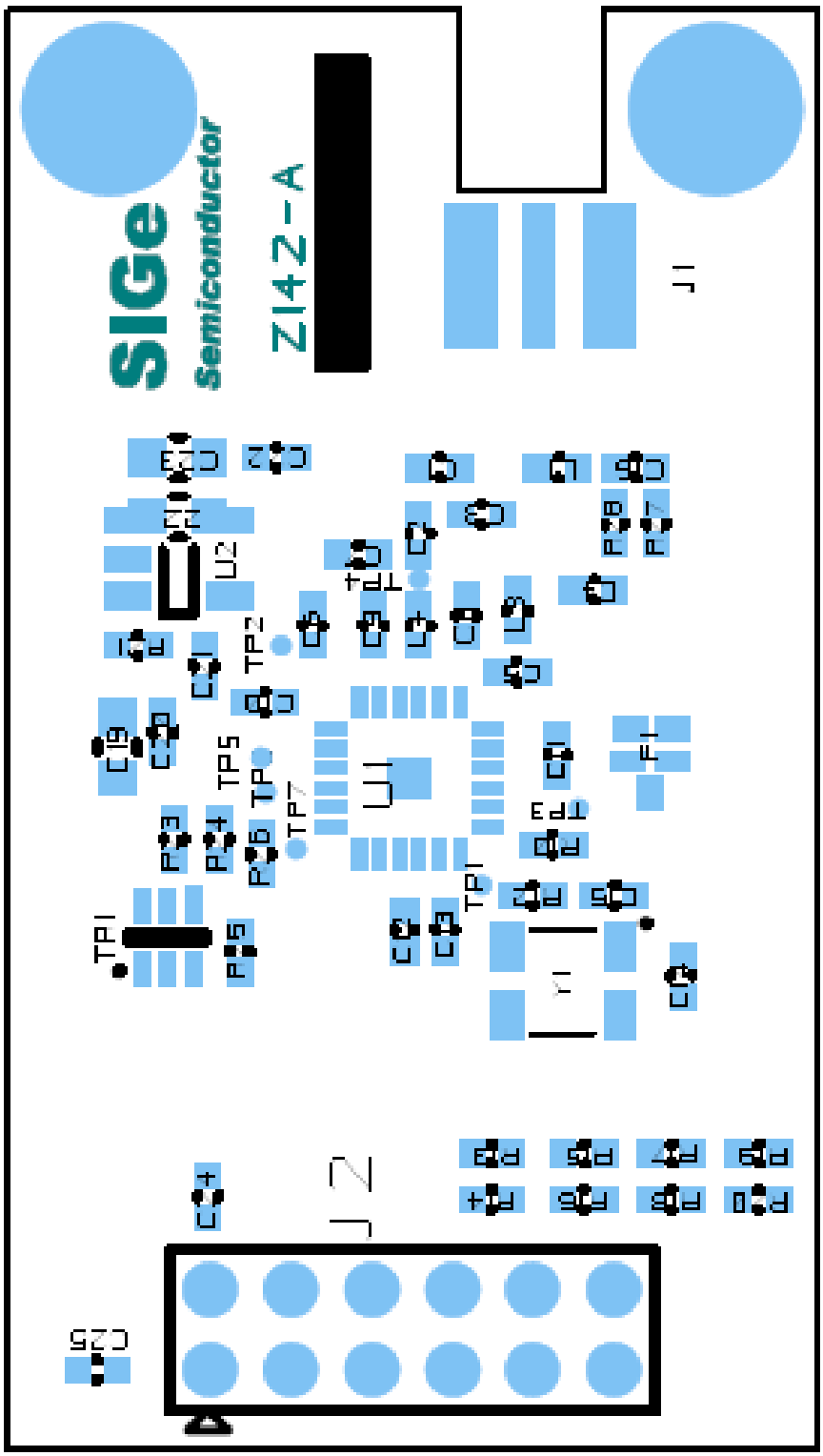
Bill O Page1

Item	Quantity	Reference	Value	PCB Footprint	Manufacturer	Part No.	Package	Tolerance	Rating	Material	Farnell	Digikey
1	2	C1,C2	22pF	C0402	Murata	GRM1555C1H220JZ01D	0402	5%	50V	C0G	8819629	
2	2	C3,C21	NF	C0402			0402					
3	7	C4,C6,C8,C10,C11,C12,C13	10nF	C0402	Murata	GRM155R71E103KA01D	0402	10%	16V	X7R	8819734	
4	1	C5	8p2	C0402	Murata	GRM1555C1H8R2DZ01D	0402	+/-0p5	50V	C0G		490-3213-1-ND
5	1	C7	1p5	C0402	Murata	GRM1555C1H1R5CZ01D	0402	+/-0p25	50V	C0G		490-1266-1-ND
6	4	C9,C14,C24,C25	100nF	C0402	Murata	GRM155R71C104KA88D	0402	10%	16V	X7R	8819742	
7	1	C15	220pF	C0402	Murata	GRM1555C1H221JA01D	0402	5%	16V	C0G	8819580	
8	3	C16,C20,C22	100pF	C0402	Murata	GRM1555C1H101JD01D	0402	5%	50V	C0G	8819572	
9	2	C19,C23	1uF	C0603	Murata	GRM185R61A105KE36D	0603	10%	10V	X5R		490-3893-1-ND
10	1	F1	B9000	SAW_2x1.4mm	Epcos	B39162-B9000-C710	2.0mmx1.4mm					
11	1	J1	MMCX	MMCX_edge	Amphenol	908-22100	MMCX_edge				1674810	
12	1	J2	2x6WAY 2mm	2x6WAY_2mm	Harwin	M22F2020605	2x6WAY_2mm				672051	
13	2	L3,L1	39nH	L0402	Toko	LL1005-FHL39NJ	0402	5%		Multilayer		
14	1	L4	10nH	L0402	Toko	LL1005-FHL10NJ	0402	5%		Multilayer		
15	1	PCB1	Z142-A									
16	6	R10,R13,R15,R17,R20,R28	NF	R0402			0402					
17	1	R12	33K	R0402	Phycomp	232270570333	0402	5%	0.063W	Thick film	9232940	
18	5	R14,R16,R18,R21,R24	47K	R0402	Phycomp	232270570473	0402	5%	0.063W	Thick film	9232966	
19	1	R19	100K	R0402	Phycomp	232270570104	0402	5%	0.063W	Thick film	9233008	
20	1	R22	NF	R0603			0603					
21	4	R23,R25,R26,R27	0R	R0402	Phycomp	232270591001	0402	5%	0.063W	Thick film	9232516	
22	7	TP1,TP2,TP3,TP4,TP5,TP6, TP7	NF	RND20			RND20					
23	1	TR1	NF	SOT-363	Rohm	UMD9NTR	SOT-363					UMD9NCT-ND
24	1	U1	SE4120L	QFN24	SiGe	SE4120L	QFN24					
25	1	U2	XC6204B332MRN	SOT23-5	Torex	XC6204B332MRN	SOT23-5		150mA		1106658	
26	1	X1	CAN	BMIS-102	LairdTech	BMIS-102	BMIS-102					
27	1	Y1	DSB321SD_ZU00503	TCXO_3.2_2.5	KDS	DSB321SD_ZU00503	TCXO_3.2_2.5	0.5ppm	16.368MHz			

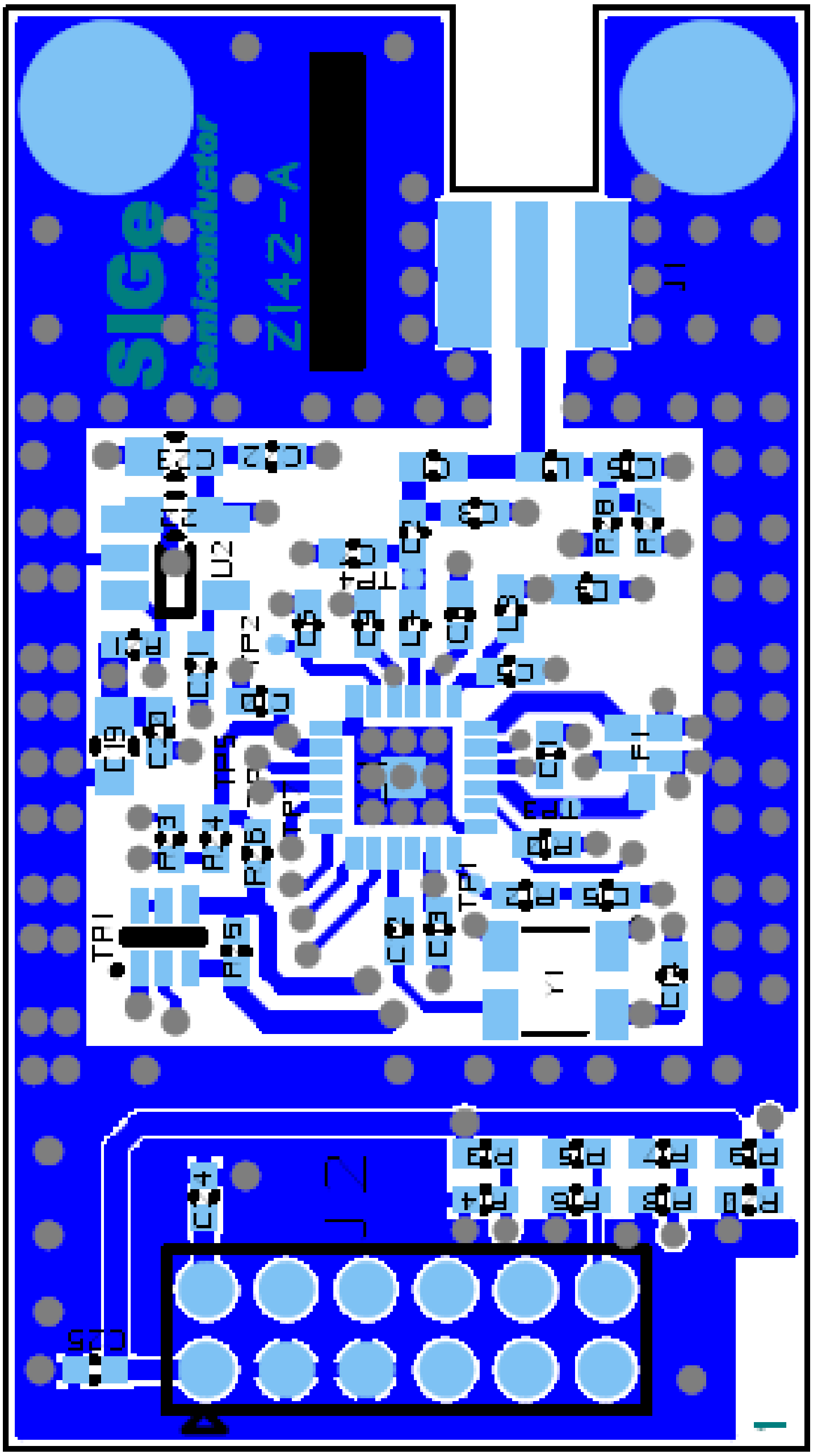
Appendix C: Board Modifications

No	Component reference	Description	Comment
1	L1	Fit 5.6nH instead of 39nH on Z142-A PCB	Poor 50 ohm PCB track is affecting LNA input match.
2	U1	Cut PCB track between U1 pin 23 and adjacent via. Connect U1 pin 23 to U1 pin 22 (P3V3) with a short wire or solder blob.	SE4120L RX_EN pin 23 is being pulled to raw VCC (P3V6) via R23 and R21. If raw VCC is high, then this can cause SW programming problems.
3	R24	Remove R24 pull-up as this is now redundant.	With R24 removed, J2 pin 7 (ENABLE) will be pulled to raw VCC supply (P3V6).

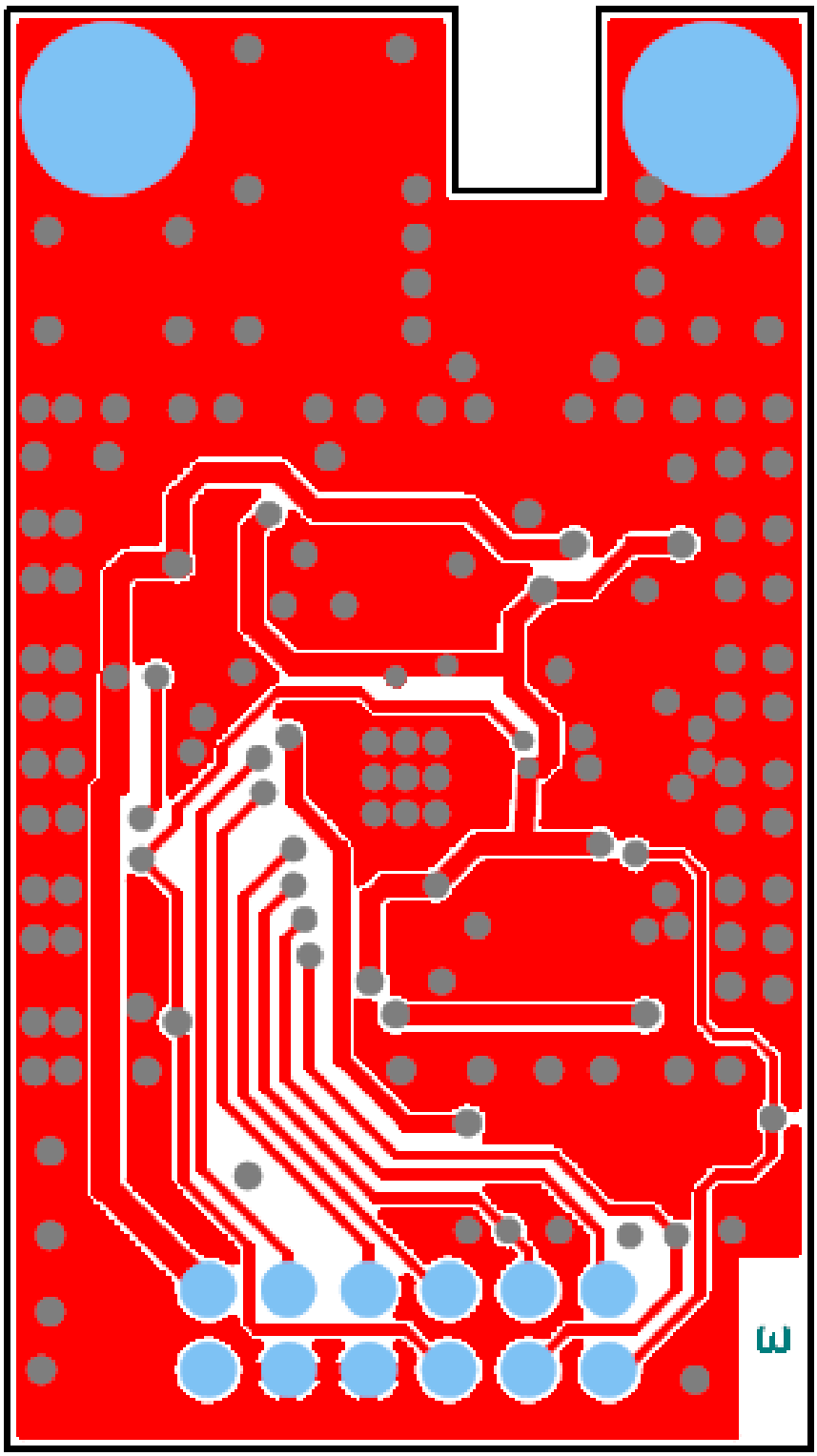
Appendix D: Assembly Drawing - Top



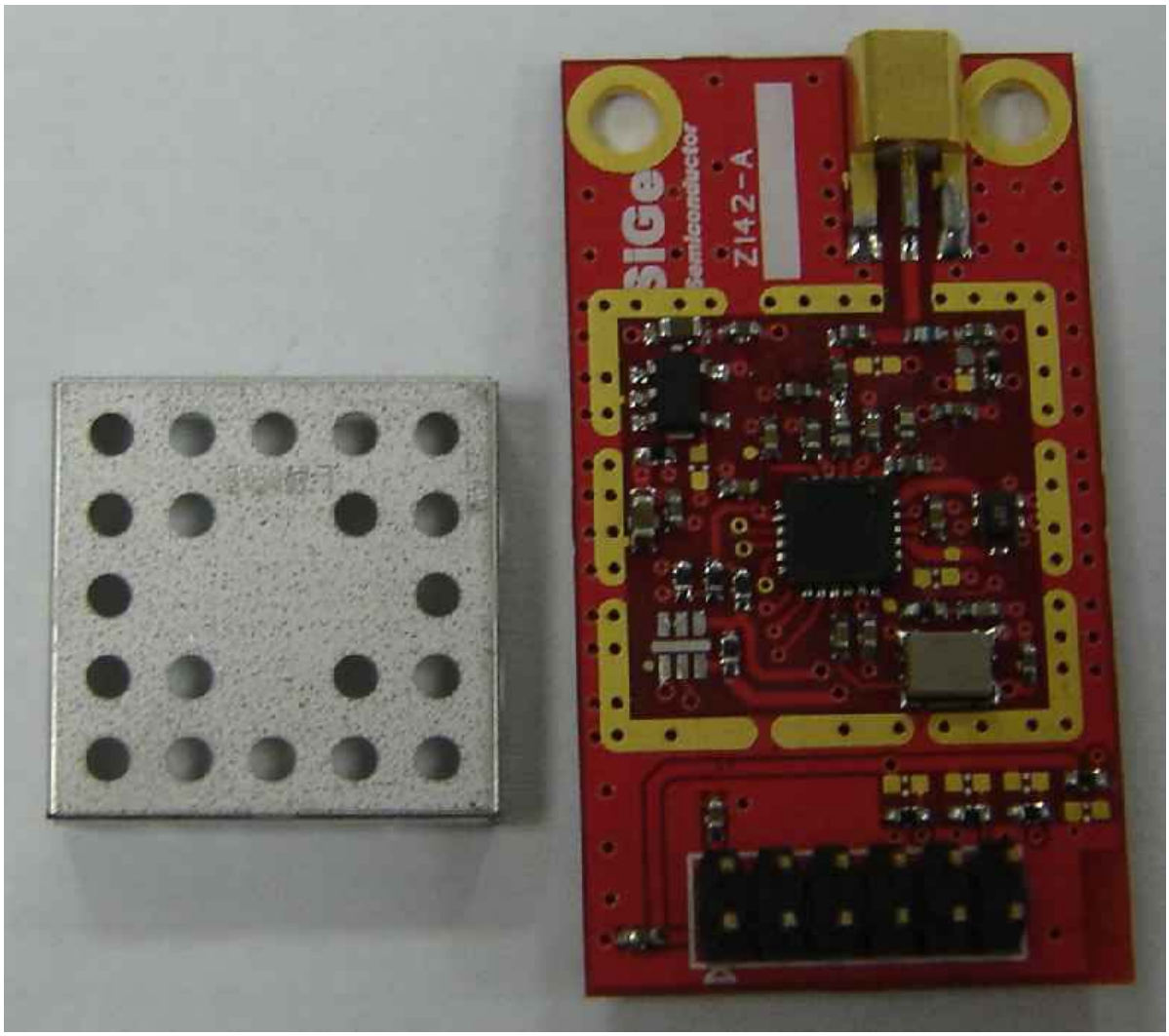
Appendix E: Component Side Tracking



Appendix F: Layer 3 Tracking



Appendix G: Top side photograph



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