- **Low Supply-Voltage Range, 1.8 V . . . 3.6 V**
- **Ultralow-Power Consumption:**
  - **Active Mode: 330 μA at 1 MHz, 2.2 V**
  - **Standby Mode: 1.1 μA**
  - **Off Mode (RAM Retention): 0.2 μA**
- **Five Power-Saving Modes**
- **Wake-Up From Standby Mode in less than 6 μs**
- **16-Bit RISC Architecture, 125-ns Instruction Cycle Time**
- **Three-Channel Internal DMA**
- **12-Bit A/D Converter With Internal Reference, Sample-and-Hold and Autoscan Feature**
- **Dual 12-Bit D/A Converters With Synchronization**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **16-Bit Timer_B With Three or Seven Capture/Compare-With-Shadow Registers**
- **On-Chip Comparator**
- **Serial Communication Interface (USART0), Functions as Asynchronous UART or Synchronous SPI or I²C™ Interface**
- **Serial Communication Interface (USART1), Functions as Asynchronous UART or Synchronous SPI Interface**
- **Supply Voltage Supervisor/Monitor With Programmable Level Detection**
- **Brownout Detector**
- **Bootstrap Loader**

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- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Family Members Include:**
  - **MSP430F155:**
    16KB+256B Flash Memory
    512B RAM
  - **MSP430F156:**
    24KB+256B Flash Memory
    1KB RAM
  - **MSP430F157:**
    32KB+256B Flash Memory,
    1KB RAM
  - **MSP430F167:**
    32KB+256B Flash Memory,
    1KB RAM
  - **MSP430F168:**
    48KB+256B Flash Memory,
    2KB RAM
  - **MSP430F169:**
    60KB+256B Flash Memory,
    2KB RAM
  - **MSP430F1610:**
    32KB+256B Flash Memory
    5KB RAM
  - **MSP430F1611:**
    48KB+256B Flash Memory
    10KB RAM
  - **MSP430F1612:**
    55KB+256B Flash Memory
    5KB RAM
- **Available in 64-Pin Quad Flat Pack (QFP) and 64-pin QFN (see Available Options)**
- **For Complete Module Descriptions, See the *MSP430x1xx Family User's Guide*, Literature Number SLAU049**

description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 6μs.

The MSP430x15x/16x/161x series are microcontroller configurations with two built-in 16-bit timers, a fast 12-bit A/D converter, dual 12-bit D/A converter, one or two universal serial synchronous/asynchronous communication interfaces (USART), I²C, DMA, and 48 I/O pins. In addition, the MSP430x161x series offers extended RAM addressing for memory-intensive applications and large C-stack requirements.

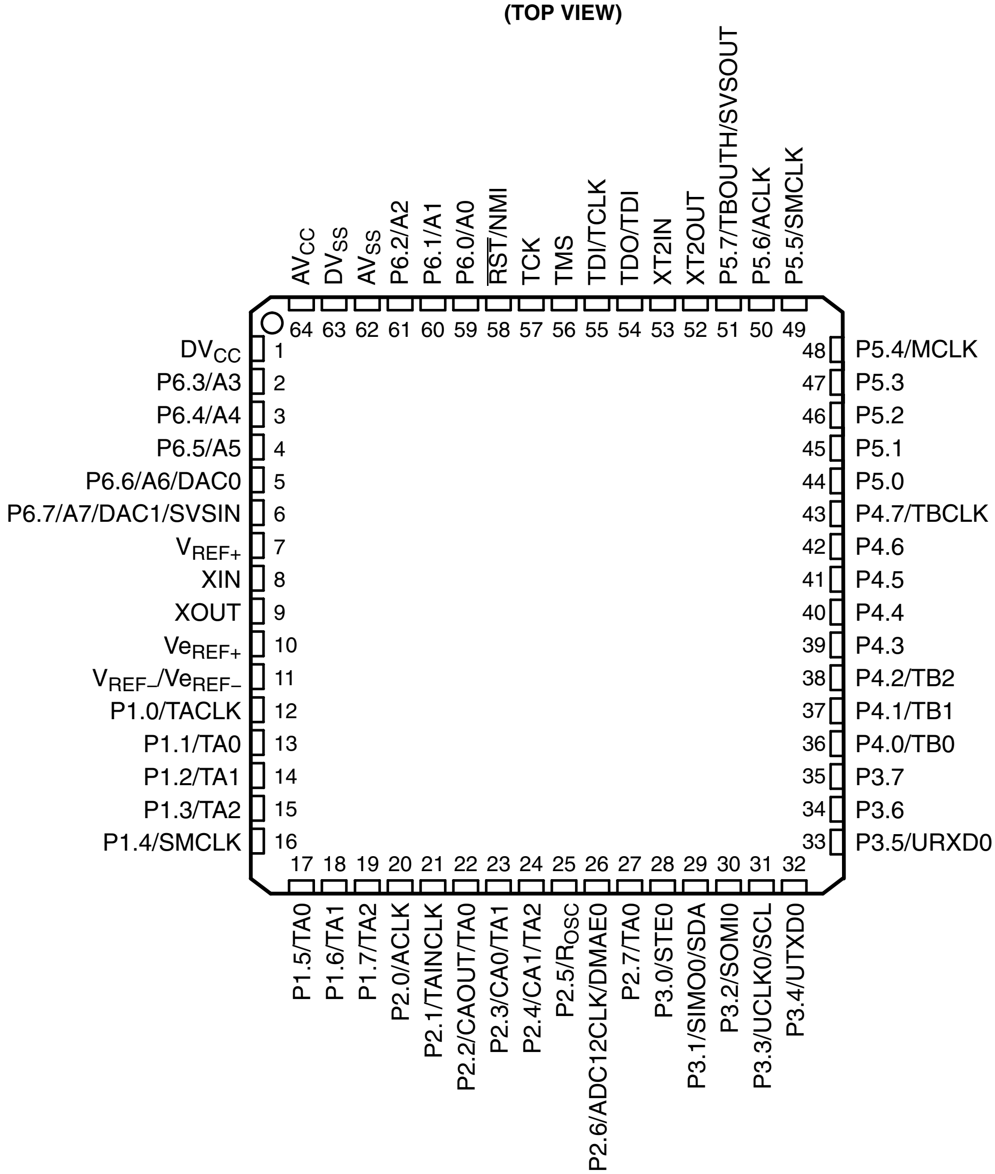
Typical applications include sensor systems, industrial control applications, hand-held meters, etc.

AVAILABLE OPTIONS

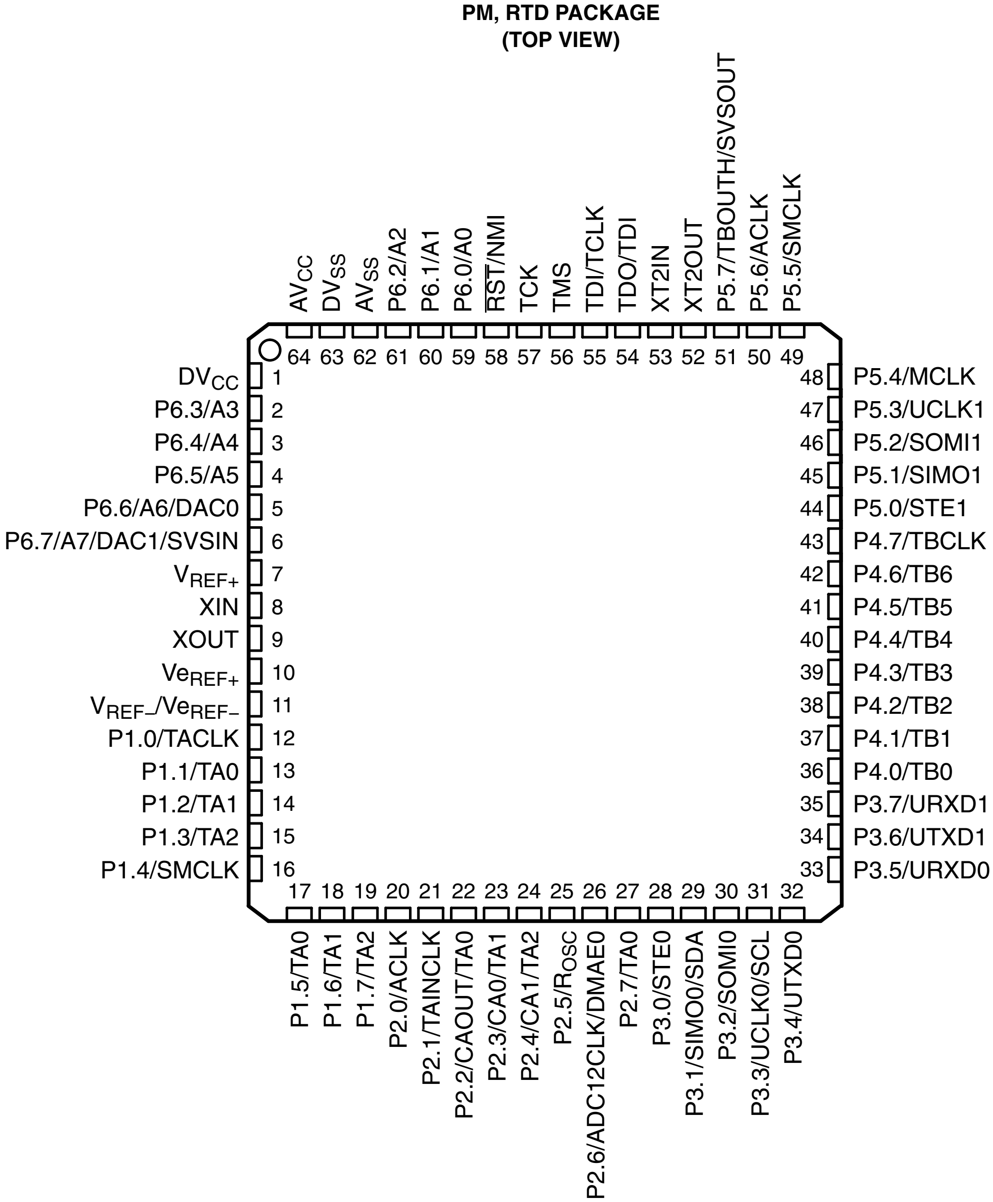
T_A	PACKAGED DEVICES	
	PLASTIC 64-PIN QFP (PM)	PLASTIC 64-PIN QFN (RTD)
−40°C to 85°C	MSP430F155IPM MSP430F156IPM MSP430F157IPM MSP430F167IPM MSP430F168IPM MSP430F169IPM MSP430F1610IPM MSP430F1611IPM MSP430F1612IPM	MSP430F155IRTD MSP430F156IRTD MSP430F157IRTD MSP430F167IRTD MSP430F168IRTD MSP430F169IRTD MSP430F1610IRTD MSP430F1611IRTD MSP430F1612IRTD

pin designation, MSP430F155, MSP430F156, and MSP430F157

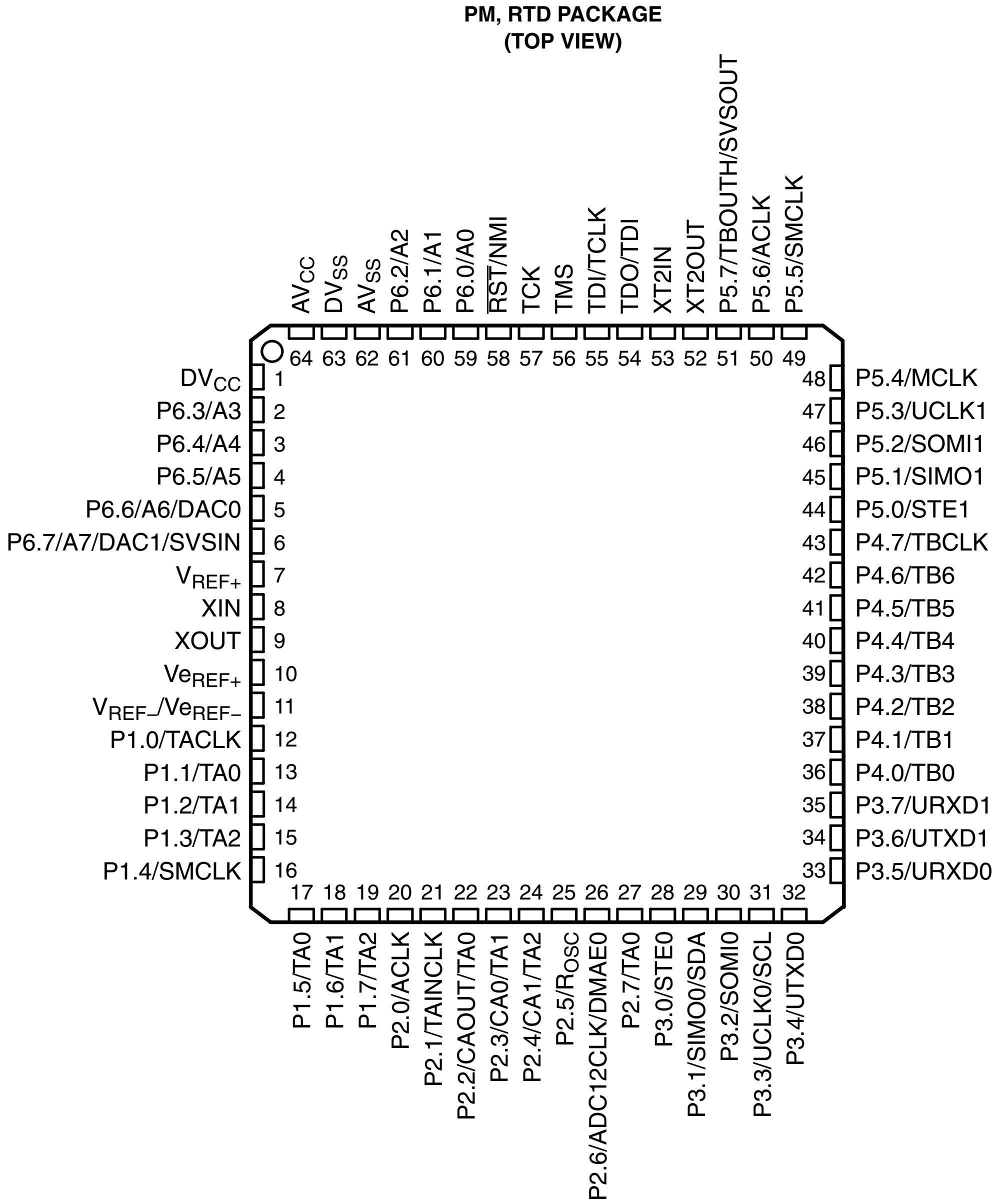
PM, RTD PACKAGE
(TOP VIEW)



pin designation, MSP430F167, MSP430F168, MSP430F169

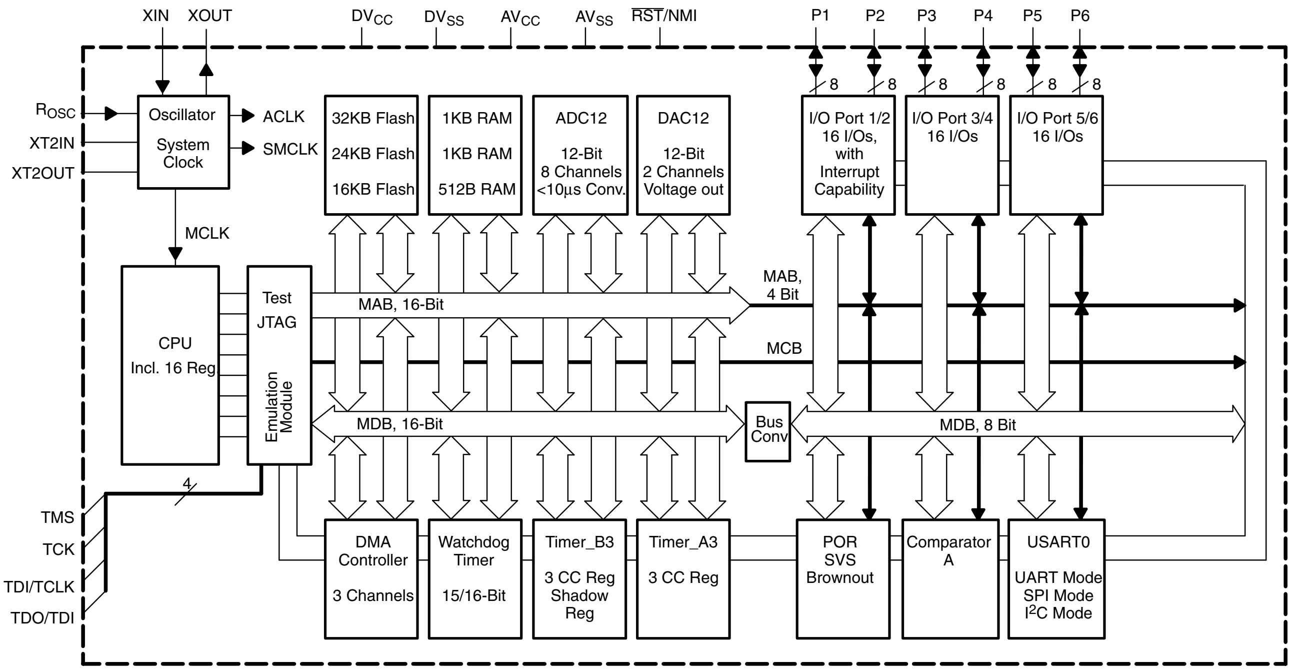


pin designation, MSP430F1610, MSP430F1611, MSP430F1612

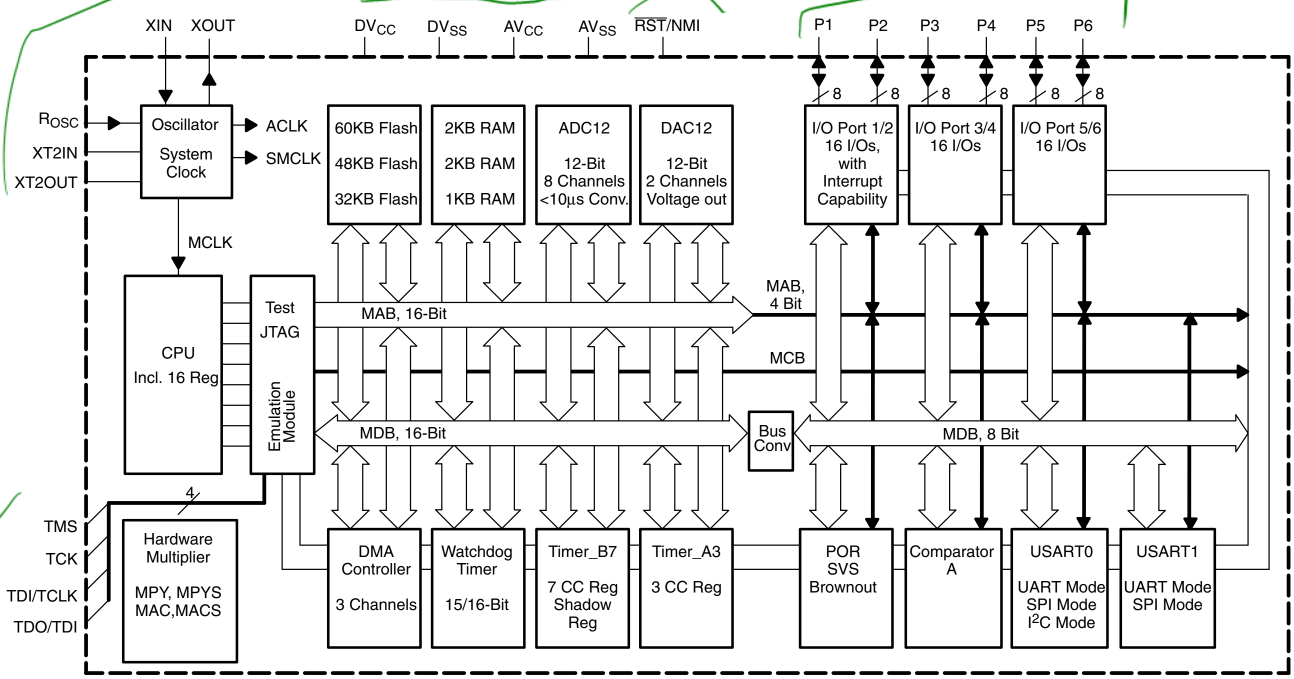


functional block diagrams

MSP430x15x

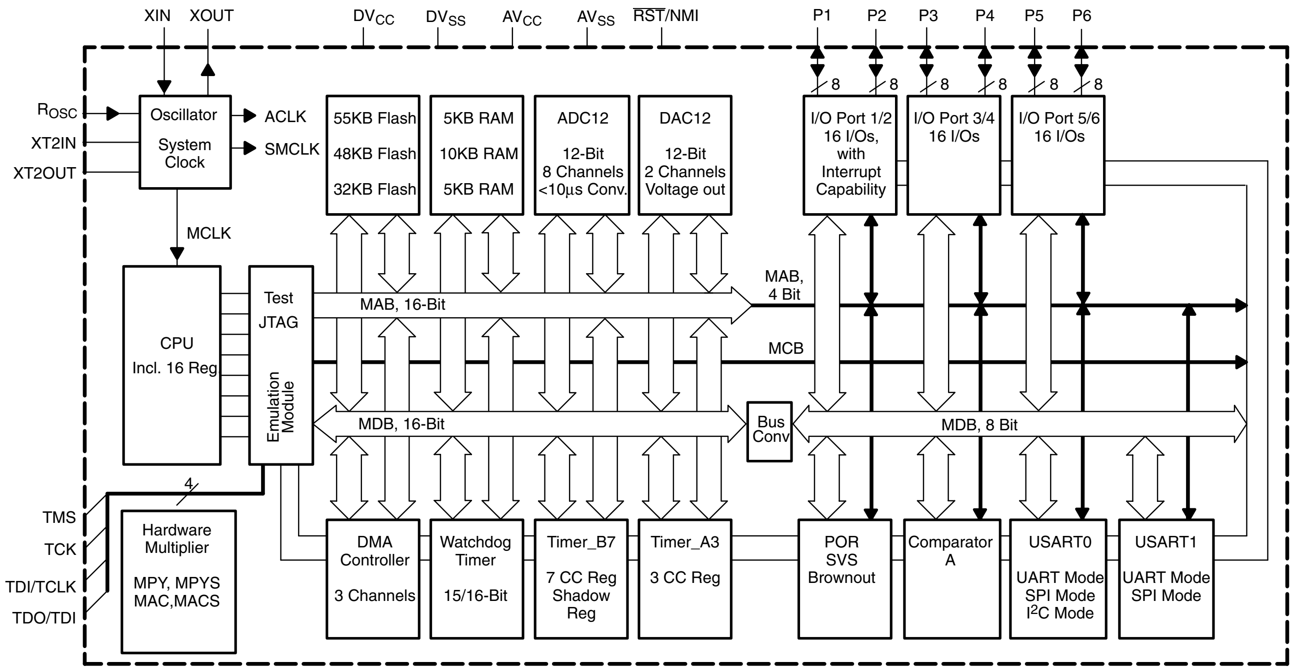


MSP430x16x



functional block diagrams (continued)

MSP430x161x



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies only the analog portion of ADC12 and DAC12.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies only the analog portion of ADC12 and DAC12.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin/SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output
P2.0/ACLK	20	I/O	General-purpose digital I/O pin/ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/Comparator_A output/BSL receive
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/Comparator_A input
P2.5/Rosc	25	I/O	General-purpose digital I/O pin/input for external resistor defining the DCO nominal frequency
P2.6/ADC12CLK/ DMAE0	26	I/O	General-purpose digital I/O pin/conversion clock – 12-bit ADC/DMA channel 0 external trigger
P2.7/TA0	27	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O pin/slave transmit enable – USART0/SPI mode
P3.1/SIMO0/SDA	29	I/O	General-purpose digital I/O pin/slave in/master out of USART0/SPI mode, I^2C data – USART0/I^2C mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O pin/slave out/master in of USART0/SPI mode
P3.3/UCLK0/SCL	31	I/O	General-purpose digital I/O pin/external clock input – USART0/UART or SPI mode, clock output – USART0/SPI mode, I^2C clock – USART0/I^2C mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O pin/transmit data out – USART0/UART mode
P3.5/URXD0	33	I/O	General-purpose digital I/O pin/receive data in – USART0/UART mode
P3.6/UTXD1†	34	I/O	General-purpose digital I/O pin/transmit data out – USART1/UART mode
P3.7/URXD1†	35	I/O	General-purpose digital I/O pin/receive data in – USART1/UART mode
P4.0/TB0	36	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI0A/B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI1A/B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI2A/B input, compare: Out2 output
P4.3/TB3†	39	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI3A/B input, compare: Out3 output
P4.4/TB4†	40	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI4A/B input, compare: Out4 output
P4.5/TB5†	41	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI5A/B input, compare: Out5 output
P4.6/TB6†	42	I/O	General-purpose digital I/O pin/Timer_B, capture: CCI6A input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin/Timer_B, clock signal TBCLK input
P5.0/STE1†	44	I/O	General-purpose digital I/O pin/slave transmit enable – USART1/SPI mode
P5.1/SIMO1†	45	I/O	General-purpose digital I/O pin/slave in/master out of USART1/SPI mode
P5.2/SOMI1†	46	I/O	General-purpose digital I/O pin/slave out/master in of USART1/SPI mode
P5.3/UCLK1†	47	I/O	General-purpose digital I/O pin/external clock input – USART1/UART or SPI mode, clock output – USART1/SPI mode

† 16x, 161x devices only

PWR
DATA
Flash
mux
WP Flash
SPI
SYNC
DATA
CLK

GPS → MV
CLK (master)
slave

Terminal Functions (Continued)

TERMINAL NAME	NO.	I/O	DESCRIPTION
P5.4/MCLK	48	I/O	General-purpose digital I/O pin/main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin/submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O pin/auxiliary clock ACLK output
P5.7/TBOUTH/ SVSOUT	51	I/O	General-purpose digital I/O pin/switch all PWM digital output ports to high impedance – Timer_B TB0 to TB6/SVS comparator output
P6.0/A0	59	I/O	General-purpose digital I/O pin/analog input a0 – 12-bit ADC
P6.1/A1	60	I/O	General-purpose digital I/O pin/analog input a1 – 12-bit ADC
P6.2/A2	61	I/O	General-purpose digital I/O pin/analog input a2 – 12-bit ADC
P6.3/A3	2	I/O	General-purpose digital I/O pin/analog input a3 – 12-bit ADC
P6.4/A4	3	I/O	General-purpose digital I/O pin/analog input a4 – 12-bit ADC
P6.5/A5	4	I/O	General-purpose digital I/O pin/analog input a5 – 12-bit ADC
P6.6/A6/DAC0	5	I/O	General-purpose digital I/O pin/analog input a6 – 12-bit ADC/DAC12.0 output
P6.7/A7/DAC1/ SVSIN	6	I/O	General-purpose digital I/O pin/analog input a7 – 12-bit ADC/DAC12.1 output/SVS input
$\overline{\text{RST}}$/NMI	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices).
TCK	57	I	Test clock. TCK is the clock input port for device programming test and bootstrap loader start
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
Ve_{REF+}	10	I	Input for an external reference voltage
V_{REF+}	7	O	Output of positive terminal of the reference voltage in the ADC12
V_{REF-}/Ve_{REF-}	11	I	Negative terminal for the reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2
QFN Pad	NA	NA	QFN package pad connection to DV_{SS} recommended (RTD package only)

short-form description

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g. CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 −−> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)−−> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) −−> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) −−> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) −−> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) −−> R11 R10 + 2−−> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 −−> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh – 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External Reset Watchdog Flash memory	WDTIFG KEYV (see Note 1)	Reset	0FFFEh	15, highest
NMI Oscillator Fault Flash memory access violation	NMIIFG (see Notes 1 & 3) OFIFG (see Notes 1 & 3) ACCVIFG (see Notes 1 & 3)	(Non)maskable (Non)maskable (Non)maskable	0FFFCh	14
Timer_B7 (see Note 5)	TBCCR0 CCIFG (see Note 2)	Maskable	0FFFAh	13
Timer_B7 (see Note 5)	TBCCR1 to TBCCR6 CCIFGs, TBIFG (see Notes 1 & 2)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF6h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit I^2C transmit/receive/others	UTXIFG0 I2CIFG (see Note 4)	Maskable	0FFF0h	8
ADC12	ADC12IFG (see Notes 1 & 2)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG (see Note 2)	Maskable	0FFECh	6
Timer_A3	TACCR1 and TACCR2 CCIFGs, TAIFG (see Notes 1 & 2)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 1 & 2)	Maskable	0FFE8h	4
USART1 receive	URXIFG1	Maskable	0FFE6h	3
USART1 transmit	UTXIFG1	Maskable	0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 1 & 2)	Maskable	0FFE2h	1
DAC12 DMA	DAC12_0IFG, DAC12_1IFG DMA0IFG, DMA1IFG, DMA2IFG (see Notes 1 & 2)	Maskable	0FFE0h	0, lowest

NOTES:
1. Multiple source flags
2. Interrupt flags are located in the module.
3. (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
4. I^2C interrupt flags located in the module
5. Timer_B7 in MSP430x16x/161x family has 7 CCRs; Timer_B3 in MSP430x15x family has 3 CCRs; in Timer_B3 there are only interrupt flags TBCCR0, 1 and 2 CCIFGs and the interrupt-enable bits TBCCR0, 1 and 2 CCIEs.

special function registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h	UTXIE0	URXIE0	ACCVIE	NMIIE			OFIE	WDTIE
	rw-0	rw-0	rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured as general-purpose timer.

OFIE: Oscillator-fault-interrupt enable

NMIIE: Nonmaskable-interrupt enable

ACCVIE: Flash memory access violation interrupt enable

URXIE0: USART0: UART and SPI receive-interrupt enable

UTXIE0: USART0: UART and SPI transmit-interrupt enable

Address	7	6	5	4	3	2	1	0
01h			UTXIE1	URXIE1				
			rw-0	rw-0				

URXIE1†: USART1: UART and SPI receive-interrupt enable

UTXIE1†: USART1: UART and SPI transmit-interrupt enable

† URXIE1 and UTXIE1 are not present in MSP430x15x devices.

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h	UTXIFG0	URXIFG0		NMIIFG			OFIFG	WDTIFG
	rw-1	rw-0		rw-0			rw-1	rw-(0)

WDTIFG: Set on watchdog-timer overflow (in watchdog mode) or security key violation
Reset on V_{CC} power-on, or a reset condition at the $\overline{RST}$/NMI pin in reset mode

OFIFG: Flag set on oscillator fault

NMIIFG: Set via $\overline{RST}$/NMI pin

URXIFG0: USART0: UART and SPI receive flag

UTXIFG0: USART0: UART and SPI transmit flag

Address	7	6	5	4	3	2	1	0
03h			UTXIFG1	URXIFG1				
			rw-1	rw-0				

URXIFG1‡: USART1: UART and SPI receive flag

UTXIFG1‡: USART1: UART and SPI transmit flag

‡ URXIFG1 and UTXIFG1 are not present in MSP430x15x devices.

module enable registers 1 and 2

Address	7	6	5	4	3	2	1	0
04h	UTXE0	URXE0 USPIE0						
	rw-0	rw-0						

URXE0: USART0: UART mode receive enable

UTXE0: USART0: UART mode transmit enable

USPIE0: USART0: SPI mode transmit and receive enable

Address	7	6	5	4	3	2	1	0
05h			UTXE1	URXE1 USPIE1				
			rw-0	rw-0				

URXE1†: USART1: UART mode receive enable

UTXE1†: USART1: UART mode transmit enable

USPIE1†: USART1: SPI mode transmit and receive enable

† URXE1, UTXE1, and USPIE1 are not present in MSP430x15x devices.

Legend:

rw:	**Bit Can Be Read and Written**
rw-0:	**Bit Can Be Read and Written. It Is Reset by PUC.**
(shaded box)	**SFR Bit Not Present in Device**

memory organization (MSP430F15x)

		MSP430F155	MSP430F156	MSP430F157
Memory Main: interrupt vector Main: code memory	Size Flash Flash	16KB 0FFFFh – 0FFE0h 0FFFFh – 0C000h	24KB 0FFFFh – 0FFE0h 0FFFFh – 0A000h	32KB 0FFFFh – 0FFE0h 0FFFFh – 08000h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM	Size	512B 03FFh – 0200h	1KB 05FFh – 0200h	1KB 05FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

memory organization (MSP430F16x)

		MSP430F167	MSP430F168	MSP430F169
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32KB 0FFFFh – 0FFE0h 0FFFFh – 08000h	48KB 0FFFFh – 0FFE0h 0FFFFh – 04000h	60KB 0FFFFh – 0FFE0h 0FFFFh – 01100h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM	Size	1KB 05FFh – 0200h	2KB 09FFh – 0200h	2KB 09FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

memory organization (MSP430F161x)

		MSP430F1610	MSP430F1611	MSP430F1612
Memory Main: interrupt vector Main: code memory	Size Flash Flash	32KB 0FFFFh – 0FFE0h 0FFFFh – 08000h	48KB 0FFFFh – 0FFE0h 0FFFFh – 04000h	55KB 0FFFFh – 0FFE0h 0FFFFh – 02500h
RAM (Total)	Size	5KB 024FFh – 01100h	10KB 038FFh – 01100h	5KB 024FFh – 01100h
Extended	Size	3KB 024FFh – 01900h	8KB 038FFh – 01900h	3KB 024FFh – 01900h
Mirrored	Size	2KB 018FFh – 01100h	2KB 018FFh – 01100h	2KB 018FFh – 01100h
Information memory	Size Flash	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h	256 Byte 010FFh – 01000h
Boot memory	Size ROM	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h	1KB 0FFFh – 0C00h
RAM (mirrored at 018FFh - 01100h)	Size	2KB 09FFh – 0200h	2KB 09FFh – 0200h	2KB 09FFh – 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h	01FFh – 0100h 0FFh – 010h 0Fh – 00h

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

BSL Function	PM, RTD Package Pins
Data Transmit	13 - P1.1
Data Receive	22 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0–n.
  Segments A and B are also called *information memory.*
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

MSP430F15x and MSP430F16x					MSP430F161x				
16KB	24KB	32KB	48KB	60KB	32KB	48KB	55KB		
0FFFFh	0FFFFh	0FFFFh	0FFFFh	0FFFFh	0FFFFh	0FFFFh	0FFFFh	Segment 0 w/ Interrupt Vectors	Main Memory
0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh	0FE00h 0FDFFh	Segment 1	
0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh	0FC00h 0FBFFh	Segment 2	
0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh	0FA00h 0F9FFh	⋮	
0C400h 0C3FFh	0A400h 0A3FFh	08400h 083FFh	04400h 043FFh	01400h 013FFh	08400h 083FFh	04400h 043FFh	02800h 027FFh	Segment n-1	
0C200h 0C1FFh	0A200h 0A1FFh	08200h 081FFh	04200h 041FFh	01200h 011FFh	08200h 081FFh	04200h 041FFh	02600h 025FFh	Segment n†	
0C000h	0A000h	08000h	04000h	01100h	08000h 024FFh	04000h 038FFh	02500h 024FFh		RAM ('F161x only)
010FFh	010FFh	010FFh	010FFh	010FFh	01100h 010FFh	01100h 010FFh	01100h 010FFh	Segment A	Info Memory
01080h 0107Fh	01080h 0107Fh	01080h 0107Fh	01080h 0107Fh	01080h 0107Fh	01080h 0107Fh	01080h 0107Fh	01080h 0107Fh	Segment B	
01000h	01000h	01000h	01000h	01000h	01000h	01000h	01000h		

† MSP430F169 and MSP430F1612 flash segment n = 256 bytes.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, see the *MSP430x1xx Family User's Guide*, literature number SLAU049.

DMA controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12 conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode without having to awaken to move data to or from a peripheral.

oscillator and system clock

The clock system in the MSP430x15x and MSP430x16x(x) family of devices is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

brownout, supply voltage supervisor

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off. The supply voltage supervisor (SVS) circuitry detects if the supply voltage drops below a user selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (SVM, the device is not automatically reset).

The CPU begins code execution after the brownout circuit releases the device reset. However, V_{CC} may not have ramped to $V_{CC(min)}$ at that time. The user must insure the default DCO settings are not changed until V_{CC} reaches $V_{CC(min)}$. If desired, the SVS circuit can be used to determine when V_{CC} reaches $V_{CC(min)}$.

digital I/O

There are six 8-bit I/O ports implemented—ports P1 through P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read/write access to port-control registers is supported by all instructions.

watchdog timer

The primary function of the watchdog timer (WDT) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

hardware multiplier (MSP430x16x/161x Only)

The multiplication operation is supported by a dedicated peripheral module. The module performs 16×16, 16×8, 8×16, and 8×8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

USART0

The MSP430x15x and the MSP430x16x(x) have one hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin), asynchronous UART and I2C communication protocols using double-buffered transmit and receive channels.

The I^2C support is compliant with the Philips I^2C specification version 2.1 and supports standard mode (up to 100 kbps) and fast mode (up to 400 kbps). In addition, 7-bit and 10-bit device addressing modes are supported, as well as master and slave modes. The USART0 also supports 16-bit-wide I^2C data transfers and has two dedicated DMA channels to maximize bus throughput. Extensive interrupt capability is also given in the I^2C mode.

USART1 (MSP430x16x/161x Only)

The MSP430x16x(x) devices have a second hardware universal synchronous/asynchronous receive transmit (USART1) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels. With the exception of I2C support, operation of USART1 is identical to USART0.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections

Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
21 - P2.1	TAINCLK	INCLK			
13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1
22 - P2.2	TA0	CCI0B			17 - P1.5
	DV_{SS}	GND			27 - P2.7
	DV_{CC}	V_{CC}			
14 - P1.2	TA1	CCI1A	CCR1	TA1	14 - P1.2
	CAOUT (internal)	CCI1B			18 - P1.6
	DV_{SS}	GND			23 - P2.3
	DV_{CC}	V_{CC}			ADC12 (internal)
15 - P1.3	TA2	CCI2A	CCR2	TA2	15 - P1.3
	ACLK (internal)	CCI2B			19 - P1.7
	DV_{SS}	GND			24 - P2.4
	DV_{CC}	V_{CC}			

timer_B3 (MSP430x15x Only)

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

timer_B7 (MSP430x16x/161x Only)

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing. Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_B3/B7 Signal Connections[†]

Input Pin Number	Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	$\overline{TBCLK}$	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3
39 - P4.3	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4
40 - P4.4	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5
41 - P4.5	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

† Timer_B3 implements three capture/compare blocks (CCR0, CCR1 and CCR2 only).

comparator_A

The primary function of the comparator_A module is to support precision slope analog−to−digital conversions, battery−voltage supervision, and monitoring of external analog signals.

ADC12

The ADC12 module supports fast, 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator and a 16 word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12

The DAC12 module is a 12-bit, R-ladder, voltage output DAC. The DAC12 may be used in 8- or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12 modules are present, they may be grouped together for synchronous operation.

peripheral file map

PERIPHERAL FILE MAP			
DMA	DMA channel 2 transfer size	DMA2SZ	01F6h
	DMA channel 2 destination address	DMA2DA	01F4h
	DMA channel 2 source address	DMA2SA	01F2h
	DMA channel 2 control	DMA2CTL	01F0h
	DMA channel 1 transfer size	DMA1SZ	01EEh
	DMA channel 1 destination address	DMA1DA	01ECh
	DMA channel 1 source address	DMA1SA	01EAh
	DMA channel 1 control	DMA1CTL	01E8h
	DMA channel 0 transfer size	DMA0SZ	01E6h
	DMA channel 0 destination address	DMA0DA	01E4h
	DMA channel 0 source address	DMA0SA	01E2h
	DMA channel 0 control	DMA0CTL	01E0h
	DMA module control 1	DMACTL1	0124h
	DMA module control 0	DMACTL0	0122h
DAC12	DAC12_1 data	DAC12_1DAT	01CAh
	DAC12_1 control	DAC12_1CTL	01C2h
	DAC12_0 data	DAC12_0DAT	01C8h
	DAC12_0 control	DAC12_0CTL	01C0h
ADC12	Interrupt-vector-word register	ADC12IV	01A8h
	Inerrupt-enable register	ADC12IE	01A6h
	Inerrupt-flag register	ADC12IFG	01A4h
	Control register 1	ADC12CTL1	01A2h
	Control register 0	ADC12CTL0	01A0h
	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
ADC12 (continued)	ADC memory-control register15	ADC12MCTL15	08Fh
	ADC memory-control register14	ADC12MCTL14	08Eh
	ADC memory-control register13	ADC12MCTL13	08Dh
	ADC memory-control register12	ADC12MCTL12	08Ch
	ADC memory-control register11	ADC12MCTL11	08Bh
	ADC memory-control register10	ADC12MCTL10	08Ah
	ADC memory-control register9	ADC12MCTL9	089h
	ADC memory-control register8	ADC12MCTL8	088h
	ADC memory-control register7	ADC12MCTL7	087h
	ADC memory-control register6	ADC12MCTL6	086h
	ADC memory-control register5	ADC12MCTL5	085h
	ADC memory-control register4	ADC12MCTL4	084h
	ADC memory-control register3	ADC12MCTL3	083h
	ADC memory-control register2	ADC12MCTL2	082h
	ADC memory-control register1	ADC12MCTL1	081h
	ADC memory-control register0	ADC12MCTL0	080h
Timer_B7/ Timer_B3 (see Note 1)	Capture/compare register 6	TBCCR6	019Eh
	Capture/compare register 5	TBCCR5	019Ch
	Capture/compare register 4	TBCCR4	019Ah
	Capture/compare register 3	TBCCR3	0198h
	Capture/compare register 2	TBCCR2	0196h
	Capture/compare register 1	TBCCR1	0194h
	Capture/compare register 0	TBCCR0	0192h
	Timer_B register	TBR	0190h
	Capture/compare control 6	TBCCTL6	018Eh
	Capture/compare control 5	TBCCTL5	018Ch
	Capture/compare control 4	TBCCTL4	018Ah
	Capture/compare control 3	TBCCTL3	0188h
	Capture/compare control 2	TBCCTL2	0186h
	Capture/compare control 1	TBCCTL1	0184h
	Capture/compare control 0	TBCCTL0	0182h
	Timer_B control	TBCTL	0180h
	Timer_B interrupt vector	TBIV	011Eh
Timer_A3	Reserved		017Eh
	Reserved		017Ch
	Reserved		017Ah
	Reserved		0178h
	Capture/compare register 2	TACCR2	0176h
	Capture/compare register 1	TACCR1	0174h
	Capture/compare register 0	TACCR0	0172h
	Timer_A register	TAR	0170h
	Reserved		016Eh
	Reserved		016Ch
	Reserved		016Ah
	Reserved		0168h

NOTE 1: Timer_B7 in MSP430x16x/161x family has 7 CCRs, Timer_B3 in MSP430x15x family has 3 CCRs.

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
Timer_A3 (continued)	Capture/compare control 2	TACCTL2	0166h
	Capture/compare control 1	TACCTL1	0164h
	Capture/compare control 0	TACCTL0	0162h
	Timer_A control	TACTL	0160h
	Timer_A interrupt vector	TAIV	012Eh
Hardware Multiplier (MSP430x16x and MSP430x161x only)	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Second operand	OP2	0138h
	Multiply signed +accumulate/operand1	MACS	0136h
	Multiply+accumulate/operand1	MAC	0134h
	Multiply signed/operand1	MPYS	0132h
	Multiply unsigned/operand1	MPY	0130h
Flash	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog	Watchdog Timer control	WDTCTL	0120h
USART1 (MSP430x16x and MSP430x161x only)	Transmit buffer	U1TXBUF	07Fh
	Receive buffer	U1RXBUF	07Eh
	Baud rate	U1BR1	07Dh
	Baud rate	U1BR0	07Ch
	Modulation control	U1MCTL	07Bh
	Receive control	U1RCTL	07Ah
	Transmit control	U1TCTL	079h
	USART control	U1CTL	078h
USART0 (UART or SPI mode)	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate	U0BR1	075h
	Baud rate	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
USART0 (I^2C mode)	I2C interrupt vector	I2CIV	011Ch
	I2C slave address	I2CSA	011Ah
	I2C own address	I2COA	0118h
	I2C data	I2CDR	076h
	I2C SCLL	I2CSCLL	075h
	I2C SCLH	I2CSCLH	074h
	I2C PSC	I2CPSC	073h
	I2C data control	I2CDCTL	072h
	I2C transfer control	I2CTCTL	071h
	USART control	U0CTL	070h
	I2C data count	I2CNDAT	052h
	I2C interrupt flag	I2CIFG	051h
	I2C interrupt enable	I2CIE	050h

peripheral file map (continued)

PERIPHERAL FILE MAP (CONTINUED)			
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control2	CACTL2	05Ah
	Comparator_A control1	CACTL1	059h
Basic Clock	Basic clock system control2	BCSCTL2	058h
	Basic clock system control1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
BrownOUT, SVS	SVS control register (reset by brownout signal)	SVSCTL	055h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt-edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt-edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag2	IFG2	003h
	SFR interrupt flag1	IFG1	002h
	SFR interrupt enable2	IE2	001h
	SFR interrupt enable1	IE1	000h

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Voltage applied at V_{CC} to V_{SS} . . . . −0.3 V to 4.1 V
Voltage applied to any pin (see Note) . . . . −0.3 V to V_{CC} + 0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature, T_{stg}: (unprogrammed device) . . . . −55°C to 150°C
(programmed device) . . . . −40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE: All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

recommended operating conditions

			MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		MSP430F15x/16x/161x	1.8		3.6	V
Supply voltage during flash memory programming, V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		MSP430F15x/16x/161x	2.7		3.6	V
Supply voltage during program execution, SVS enabled (see Note 1), V_{CC} ($AV_{CC} = DV_{CC} = V_{CC}$)		MSP430F15x/16x/161x	2		3.6	V
Supply voltage, V_{SS} ($AV_{SS} = DV_{SS} = V_{SS}$)			0		0	V
Operating free-air temperature range, T_A		MSP430F15x/16x/161x	−40		85	°C
LFXT1 crystal frequency, $f_{(LFXT1)}$ (see Notes 2 and 3)	LF selected, XTS=0	Watch crystal		32.768		kHz
	XT1 selected, XTS=1	Ceramic resonator	450		8000	kHz
	XT1 selected, XTS=1	Crystal	1000		8000	kHz
XT2 crystal frequency, $f_{(XT2)}$		Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
Processor frequency (signal MCLK), $f_{(System)}$		V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	

NOTES: 1. The minimum operating supply voltage is defined according to the trip point where POR is going active by decreasing the supply voltage. POR is going inactive when the V_{CC} is raised above the minimum supply voltage plus the hysteresis of the SVS circuitry.
2. In LF mode, the LFXT1 oscillator requires a watch crystal. A 5.1MΩ resistor from XOUT to V_{SS} is recommended when V_{CC} < 2.5 V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 4.15MHz at $V_{CC} \geq 2.2$ V. In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 8MHz at $V_{CC} \geq 2.8$ V.
3. In LF mode, the LFXT1 oscillator requires a watch crystal. In XT1 mode, LFXT1 accepts a ceramic resonator or a crystal.

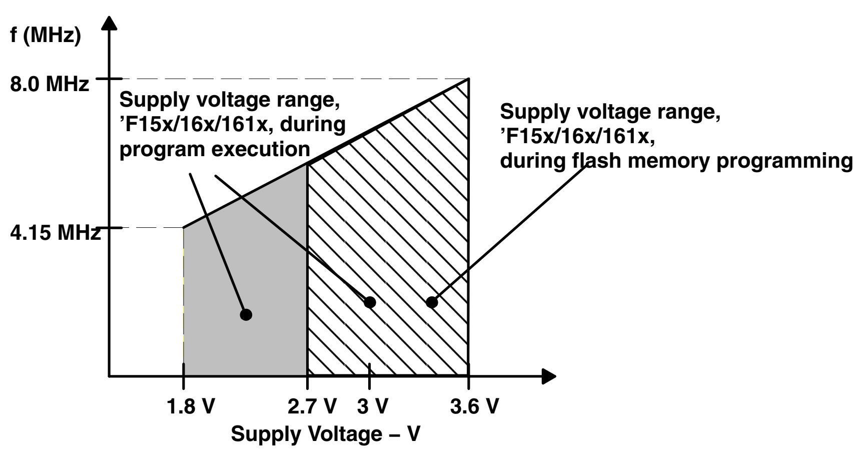


Figure 1. Frequency vs Supply Voltage, MSP430F15x/16x/161x

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

MSP430F15x/16x supply current into AV_{CC} + DV_{CC} excluding external current ($AV_{CC} = DV_{CC} = V_{CC}$)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		330	400	µA
			V_{CC} = 3 V		500	600	
	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 4,096 Hz, $f_{(ACLK)}$ = 4,096 Hz XTS=0, SELM=3	T_A = –40°C to 85°C	V_{CC} = 2.2 V		2.5	7	µA
			V_{CC} = 3 V		9	20	
$I_{(LPM0)}$	Low-power mode, (LPM0) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1) (see Note 1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		50	60	µA
			V_{CC} = 3 V		75	90	
$I_{(LPM2)}$	Low-power mode, (LPM2), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32.768 Hz, SCG0 = 0	T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 2)	T_A = –40°C	V_{CC} = 2.2 V		1.1	1.6	µA
		T_A = 25°C			1.1	1.6	
		T_A = 85°C			2.2	3.0	
		T_A = –40°C	V_{CC} = 3 V		2.2	2.8	
		T_A = 25°C			2.0	2.6	
		T_A = 85°C			3.0	4.3	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	T_A = –40°C	V_{CC} = 2.2V / 3 V		0.1	0.5	µA
		T_A = 25°C			0.2	0.5	
		T_A = 85°C			1.3	2.5	

NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. WDT is clocked by $f_{(ACLK)}$ = 32,768 Hz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency, F-version

$$I(AM) = I(AM)\ [1\ MHz] \times f(System)\ [MHz]$$

Current consumption of active mode versus supply voltage, F-version

$$I_{(AM)} = I_{(AM)\ [3\ V]} + 210\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

MSP430F161x supply current into AV_{CC} + DV_{CC} excluding external current (AV_{CC} = DV_{CC} = V_{CC})

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$I_{(AM)}$	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		330	400	µA
			V_{CC} = 3 V		500	600	
	Active mode, (see Note 1) $f_{(MCLK)} = f_{(SMCLK)}$ = 4,096 Hz, $f_{(ACLK)}$ = 4,096 Hz XTS=0, SELM=3	T_A = –40°C to 85°C	V_{CC} = 2.2 V		2.5	7	µA
			V_{CC} = 3 V		9	20	
$I_{(LPM0)}$	Low-power mode, (LPM0) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32,768 Hz XTS=0, SELM=(0,1) (see Note 1)	T_A = –40°C to 85°C	V_{CC} = 2.2 V		50	60	µA
			V_{CC} = 3 V		75	95	
$I_{(LPM2)}$	Low-power mode, (LPM2), $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32.768 Hz, SCG0 = 0	T_A = –40°C to 85°C	V_{CC} = 2.2 V		11	14	µA
			V_{CC} = 3 V		17	22	
$I_{(LPM3)}$	Low-power mode, (LPM3) $f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32,768 Hz, SCG0 = 1 (see Note 2)	T_A = –40°C	V_{CC} = 2.2 V		1.3	1.6	µA
		T_A = 25°C			1.3	1.6	
		T_A = 85°C			3.0	6.0	
		T_A = –40°C	V_{CC} = 3 V		2.6	3.0	
		T_A = 25°C			2.6	3.0	
		T_A = 85°C			4.4	8.0	
$I_{(LPM4)}$	Low-power mode, (LPM4) $f_{(MCLK)}$ = 0 MHz, $f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 0 Hz, SCG0 = 1	T_A = –40°C	V_{CC} = 2.2V / 3 V		0.2	0.5	µA
		T_A = 25°C			0.2	0.5	
		T_A = 85°C			2.0	5.0	

NOTES: 1. Timer_B is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
2. WDT is clocked by $f_{(ACLK)}$ = 32,768 Hz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency, F-version

$$I(AM) = I(AM)\,[1\ \text{MHz}] \times f(\text{System})\,[\text{MHz}]$$

Current consumption of active mode versus supply voltage, F-version

$$I_{(AM)} = I_{(AM)\,[3\ V]} + 210\ \mu A/V \times (V_{CC} - 3\ V)$$

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

SCHMITT-trigger inputs – Ports P1, P2, P3, P4, P5, P6; $\overline{RST}$/NMI; JTAG: TCK, TMS, TDI/TCLK, TDO/TDI

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 2.2 V	1.1		1.5	V
		V_{CC} = 3 V	1.5		1.98	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 2.2 V	0.4		0.9	V
		V_{CC} = 3 V	0.9		1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.3		1.1	V
		V_{CC} = 3 V	0.5		1	

inputs Px.x, TAx, TBx

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, external trigger signal for the interrupt flag, (see Note 1)	2.2 V	62			ns
			3 V	50			
$t_{(cap)}$	Timer_A, Timer_B capture timing	TA0, TA1, TA2	2.2 V	62			ns
		TB0, TB1, TB2, TB3, TB4, TB5, TB6 (see Note 2)	3 V	50			
$f_{(TAext)}$	Timer_A, Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V			8	MHz
$f_{(TBext)}$			3 V			10	
$f_{(TAint)}$	Timer_A, Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V			8	MHz
$f_{(TBint)}$			3 V			10	

NOTES: 1. The external signal sets the interrupt flag every time the minimum $t_{(int)}$ parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$.
2. Seven capture/compare registers in ’x16x/161x and three capture/compare registers in ’x15x.

leakage current – Ports P1, P2, P3, P4, P5 and P6 (see Note 1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{lkg(Px.y)}$	Leakage current	Port Px	$V_{(Px.y)}$ (see Note 2)	V_{CC} = 2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The port pin must be selected as input.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3, P4, P5, and P6

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH(max)} = -1.5$ mA,	$V_{CC} = 2.2$ V,	See Note 1	$V_{CC}-0.25$		V_{CC}	V
		$I_{OH(max)} = -6$ mA,	$V_{CC} = 2.2$ V,	See Note 2	$V_{CC}-0.6$		V_{CC}	
		$I_{OH(max)} = -1.5$ mA,	$V_{CC} = 3$ V,	See Note 1	$V_{CC}-0.25$		V_{CC}	
		$I_{OH(max)} = -6$ mA,	$V_{CC} = 3$ V,	See Note 2	$V_{CC}-0.6$		V_{CC}	
V_{OL}	Low-level output voltage	$I_{OL(max)} = 1.5$ mA,	$V_{CC} = 2.2$ V,	See Note 1	V_{SS}		$V_{SS}+0.25$	V
		$I_{OL(max)} = 6$ mA,	$V_{CC} = 2.2$ V,	See Note 2	V_{SS}		$V_{SS}+0.6$	
		$I_{OL(max)} = 1.5$ mA,	$V_{CC} = 3$ V,	See Note 1	V_{SS}		$V_{SS}+0.25$	
		$I_{OL(max)} = 6$ mA,	$V_{CC} = 3$ V,	See Note 2	V_{SS}		$V_{SS}+0.6$	

NOTES: 1. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±12 mA to satisfy the maximum specified voltage drop.
2. The maximum total current, $I_{OH(max)}$ and $I_{OL(max)}$, for all outputs combined, should not exceed ±48 mA to satisfy the maximum specified voltage drop.

output frequency

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$f_{(Px.y)}$	$(1 \le x \le 6,\ 0 \le y \le 7)$	$C_L = 20$ pF, $I_L = \pm1.5$ mA	$V_{CC} = 2.2$ V / 3 V	DC		f_{System}	MHz
$f_{(ACLK)}$ $f_{(MCLK)}$ $f_{(SMCLK)}$	P2.0/ACLK, P5.6/ACLK P5.4/MCLK, P1.4/SMCLK, P5.5/SMCLK	$C_L = 20$ pF	$V_{CC} = 2.2$ V / 3 V			f_{System}	MHz
$t_{(Xdc)}$	Duty cycle of output frequency	P1.0/TACLK $C_L = 20$ pF $V_{CC} = 2.2$ V / 3 V	$f_{(ACLK)} = f_{(LFXT1)} = f_{(XT1)}$	40%		60%	
			$f_{(ACLK)} = f_{(LFXT1)} = f_{(LF)}$	30%		70%	
			$f_{(ACLK)} = f_{(LFXT1)}$		50%		
		P1.1/TA0/MCLK, $C_L = 20$ pF, $V_{CC} = 2.2$ V / 3 V	$f_{(MCLK)} = f_{(XT1)}$	40%		60%	
			$f_{(MCLK)} = f_{(DCOCLK)}$	50%– 15 ns	50%	50%+ 15 ns	
		P1.4/TBCLK/SMCLK, $C_L = 20$ pF, $V_{CC} = 2.2$ V / 3 V	$f_{(SMCLK)} = f_{(XT2)}$	40%		60%	
			$f_{(SMCLK)} = f_{(DCOCLK)}$	50%– 15 ns	50%	50%+ 15 ns	

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

outputs – Ports P1, P2, P3, P4, P5, and P6 (continued)

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

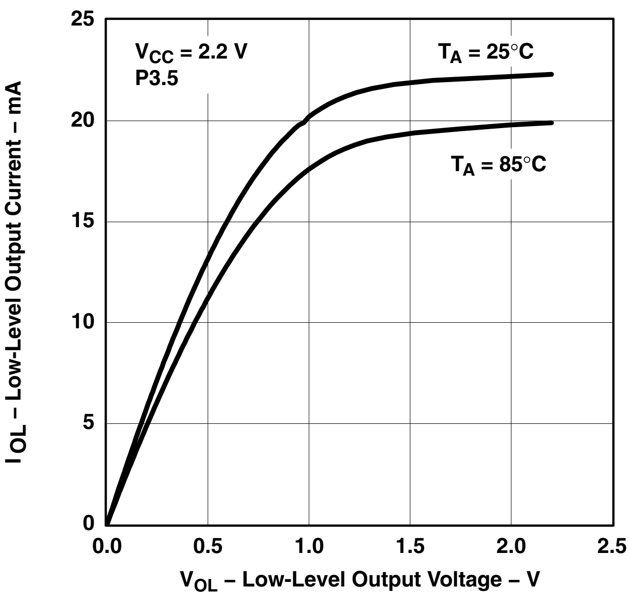


Figure 2

TYPICAL LOW-LEVEL OUTPUT CURRENT
vs
LOW-LEVEL OUTPUT VOLTAGE

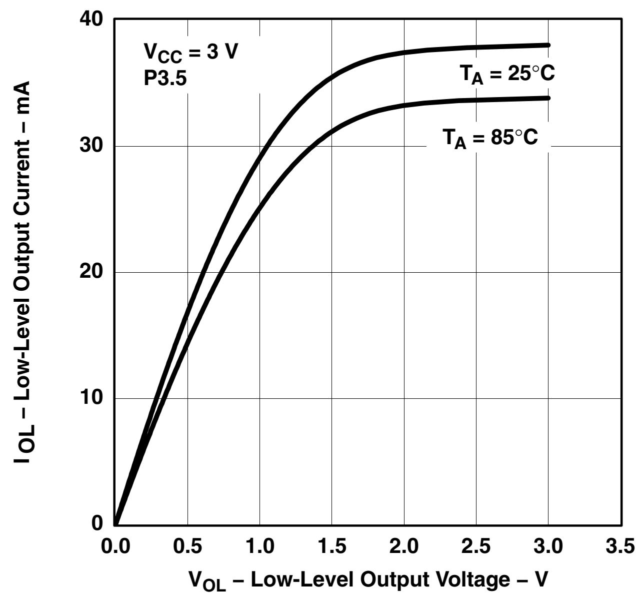


Figure 3

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

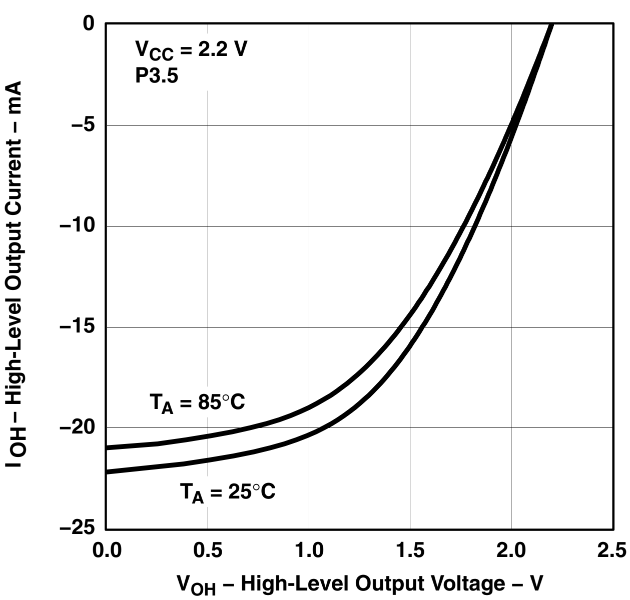


Figure 4

TYPICAL HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

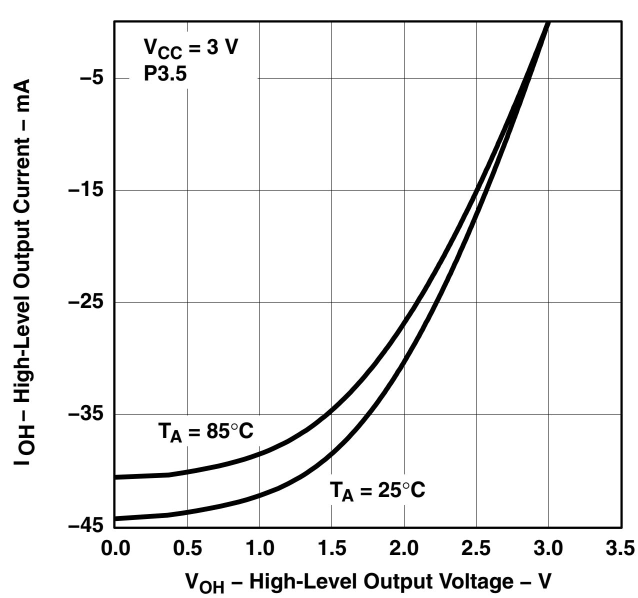


Figure 5

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

wake-up LPM3

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(LPM3)}$	Delay time	V_{CC} = 2.2 V/3 V, $f_{DCO} \geq f_{DCO43}$			6	μs

RAM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VRAMh	CPU HALTED (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

Comparator_A (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	V_{CC} = 2.2 V		25	40	μA
			V_{CC} = 3 V		45	60	
$I_{(Refladder/Refdiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V		30	50	μA
			V_{CC} = 3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON =1	V_{CC} = 2.2 V/3 V	0		V_{CC}–1	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5} V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	V_{CC} = 2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	(see Figure 6 and Figure 7)	PCA0=1, CARSEL=1, CAREF=3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2 T_A = 85°C	V_{CC} = 2.2 V	390	480	540	mV
			V_{CC} = 3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	V_{CC} = 2.2 V/3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON=1	V_{CC} = 2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	μs
			V_{CC} = 3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	V_{CC} = 2.2 V	130	210	300	ns
			V_{CC} = 3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	V_{CC} = 2.2 V	1.4	1.9	3.4	μs
			V_{CC} = 3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

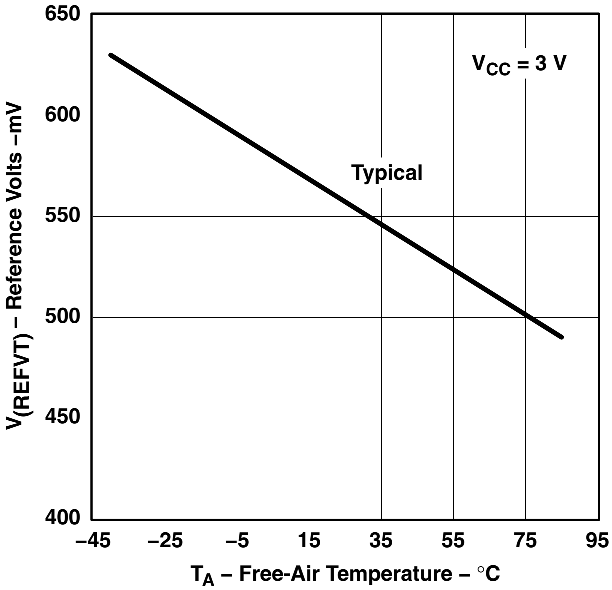


Figure 6. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

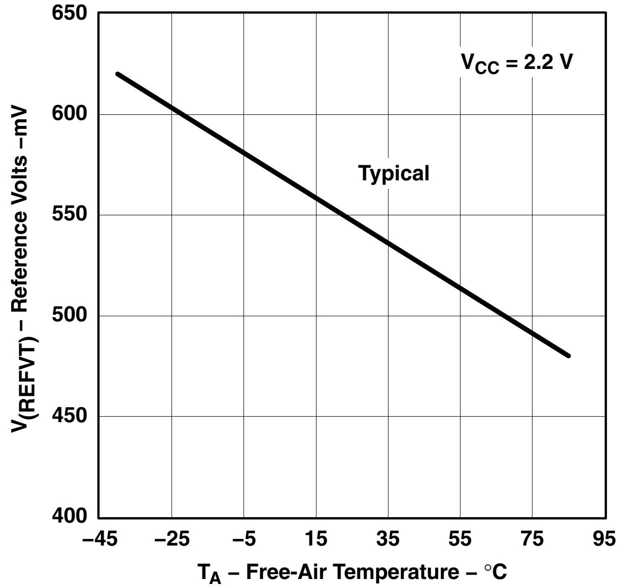


Figure 7. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

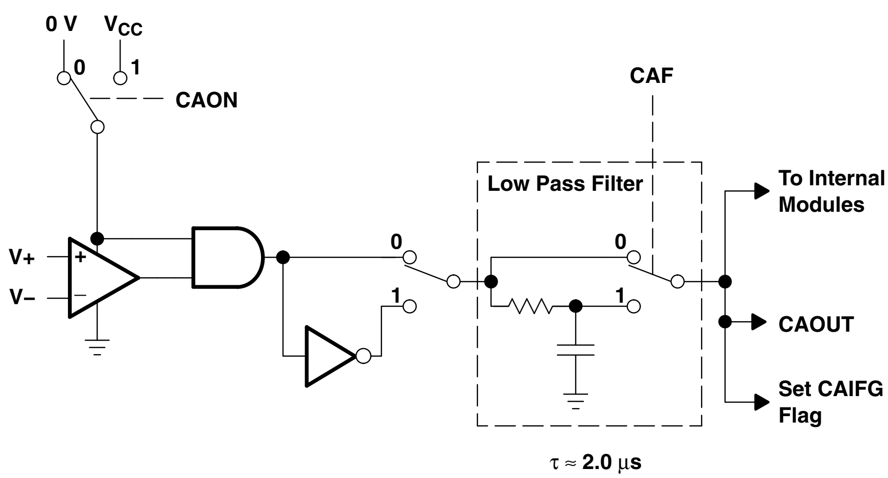


Figure 8. Block Diagram of Comparator_A Module

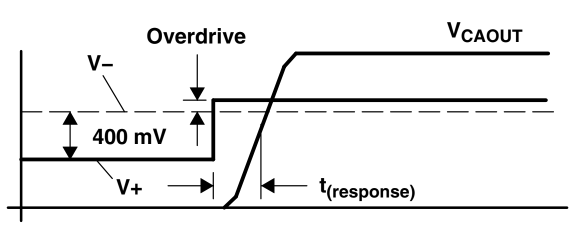


Figure 9. Overdrive Definition

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

POR/brownout reset (BOR) (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout				2000	μs
$V_{CC(Start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10 through Figure 12)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 10)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			μs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8 V.

2. During power up, the CPU begins code execution following a period of $t_{BOR(delay)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency. See the *MSP430x1xx Family User's Guide* (SLAU049) for more information on the brownout/SVS circuit.

typical characteristics

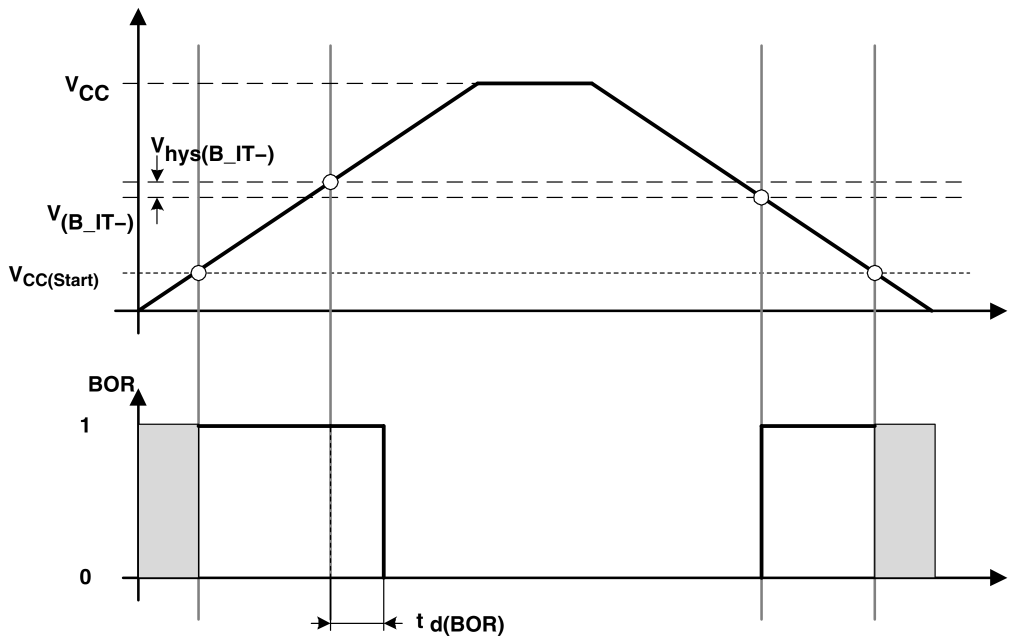


Figure 10. POR/Brownout Reset (BOR) vs Supply Voltage

typical characteristics (continued)

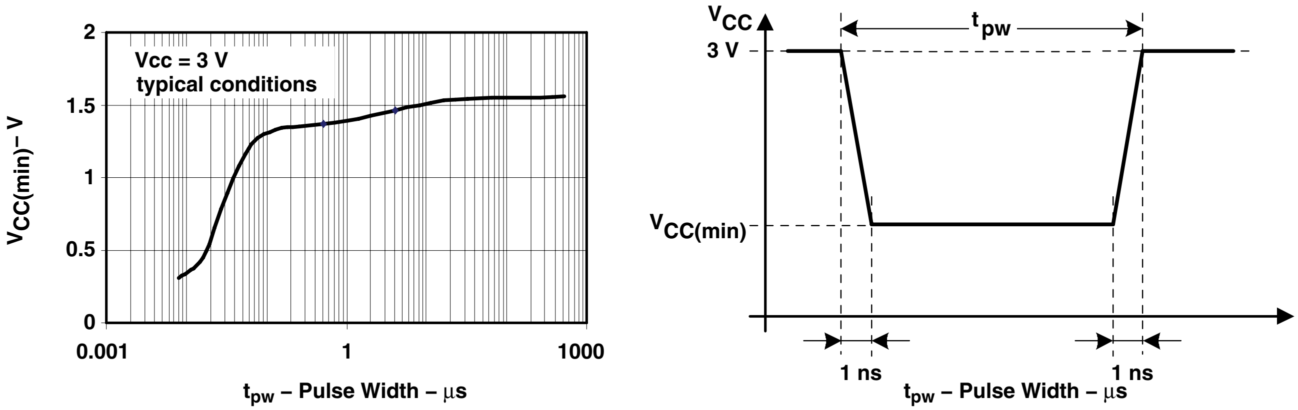


Figure 11. $V_{CC(min)}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

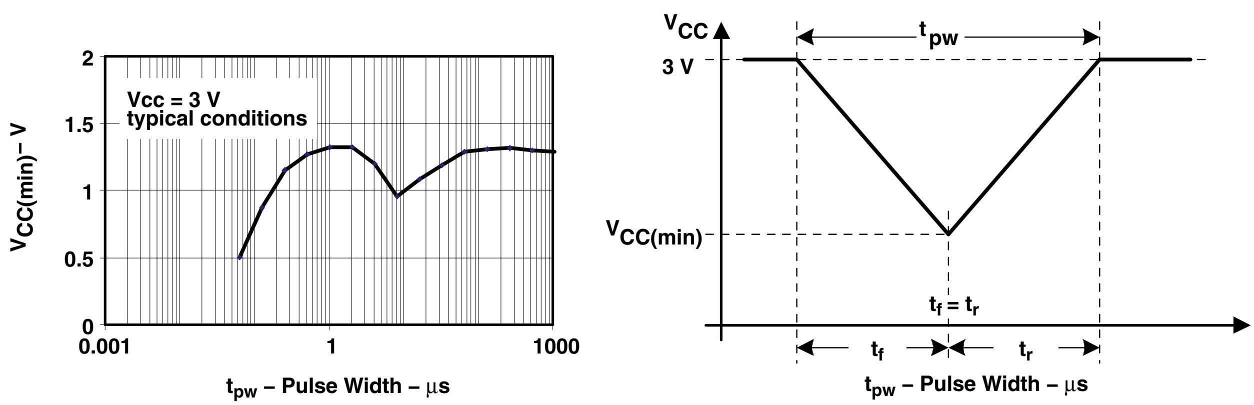


Figure 12. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

SVS (supply voltage supervisor/monitor)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$t_{(SVSR)}$	$dV_{CC}/dt > 30$ V/ms (see Figure 13)		5		150	µs
	$dV_{CC}/dt \leq 30$ V/ms				2000	µs
$t_{d(SVSon)}$	SVSON, switch from VLD = 0 to VLD ≠ 0, V_{CC} = 3 V		20		150	µs
t_{settle}	VLD ≠ 0‡				12	µs
$V_{(SVSstart)}$	VLD ≠ 0, $V_{CC}/dt \leq 3$ V/s (see Figure 13)			1.55	1.7	V
$V_{hys(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 13)	VLD = 1	70	120	155	mV
		VLD = 2 .. 14	$V_{(SVS\_IT-)}$ x 0.004		$V_{(SVS\_IT-)}$ x 0.008	
	$V_{CC}/dt \leq 3$ V/s (see Figure 13), External voltage applied on A7	VLD = 15	4.4		10.4	mV
$V_{(SVS\_IT-)}$	$V_{CC}/dt \leq 3$ V/s (see Figure 13 and Figure 14)	VLD = 1	1.8	1.9	2.05	V
		VLD = 2	1.94	2.1	2.25	
		VLD = 3	2.05	2.2	2.37	
		VLD = 4	2.14	2.3	2.48	
		VLD = 5	2.24	2.4	2.6	
		VLD = 6	2.33	2.5	2.71	
		VLD = 7	2.46	2.65	2.86	
		VLD = 8	2.58	2.8	3	
		VLD = 9	2.69	2.9	3.13	
		VLD = 10	2.83	3.05	3.29	
		VLD = 11	2.94	3.2	3.42	
		VLD = 12	3.11	3.35	3.61†	
		VLD = 13	3.24	3.5	3.76†	
		VLD = 14	3.43	3.7†	3.99†	
	$V_{CC}/dt \leq 3$ V/s (see Figure 13 and Figure 14), External voltage applied on A7	VLD = 15	1.1	1.2	1.3	
$I_{CC(SVS)}$ (see Note 1)	VLD ≠ 0, V_{CC} = 2.2 V/3 V			10	15	µA

† The recommended operating voltage range is limited to 3.6 V.

‡ t_{settle} is the settling time that the comparator o/p needs to have a stable level after VLD is switched VLD ≠ 0 to a different VLD value somewhere between 2 and 15. The overdrive is assumed to be > 50 mV.

NOTE 1: The current consumption of the SVS module is not included in the I_{CC} current consumption data.

typical characteristics

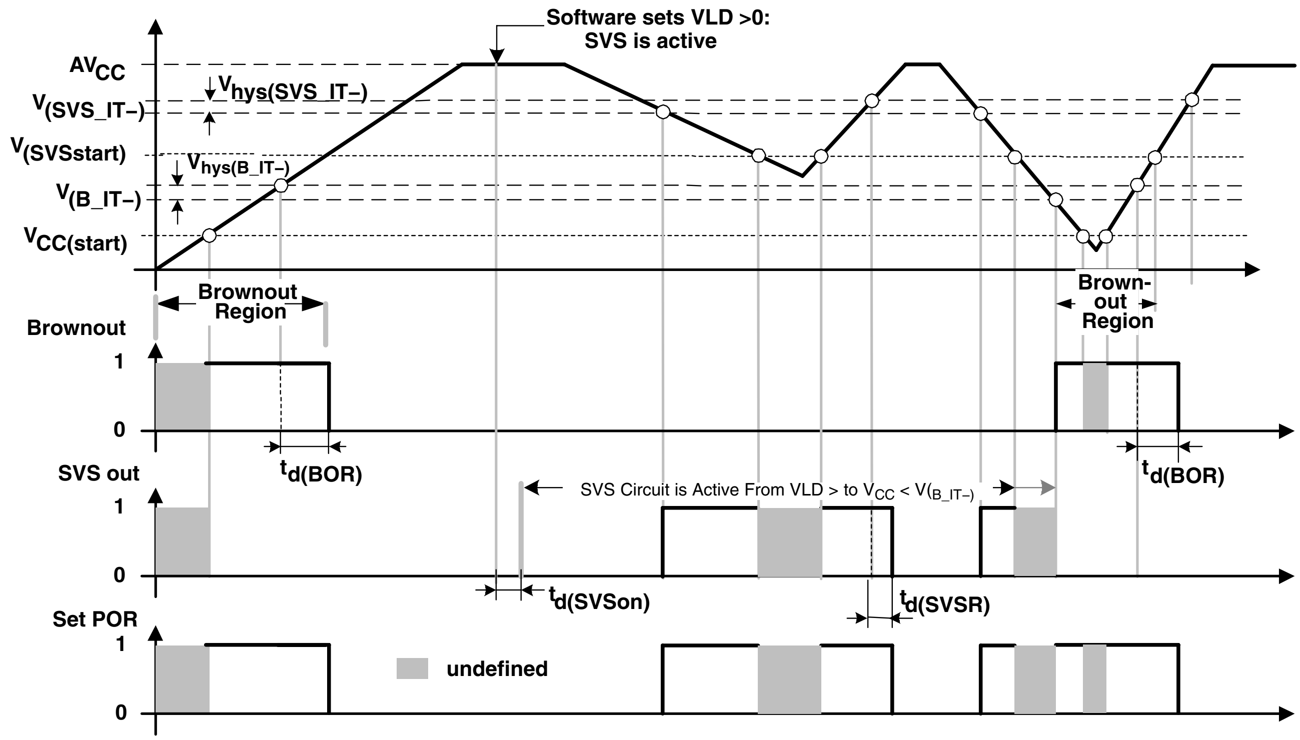
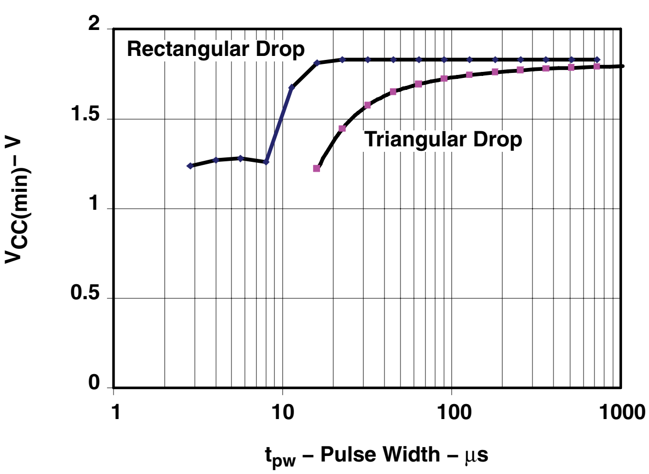


Figure 13. SVS Reset (SVSR) vs Supply Voltage



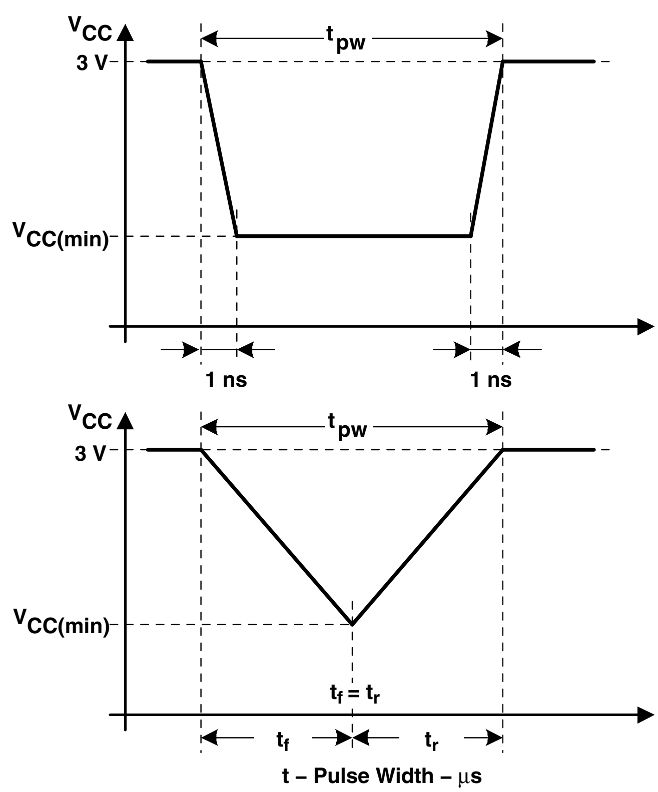


Figure 14. $V_{CC(min)}$: Square Voltage Drop and Triangle Voltage Drop to Generate an SVS Signal (VLD = 1)

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

DCO (see Note 1)

PARAMETER	TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{(DCO03)}$	R_{sel} = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.08	0.12	0.15	MHz
		V_{CC} = 3 V	0.08	0.13	0.16	
$f_{(DCO13)}$	R_{sel} = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.14	0.19	0.23	MHz
		V_{CC} = 3 V	0.14	0.18	0.22	
$f_{(DCO23)}$	R_{sel} = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.22	0.30	0.36	MHz
		V_{CC} = 3 V	0.22	0.28	0.34	
$f_{(DCO33)}$	R_{sel} = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.37	0.49	0.59	MHz
		V_{CC} = 3 V	0.37	0.47	0.56	
$f_{(DCO43)}$	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	0.61	0.77	0.93	MHz
		V_{CC} = 3 V	0.61	0.75	0.90	
$f_{(DCO53)}$	R_{sel} = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1	1.2	1.5	MHz
		V_{CC} = 3 V	1	1.3	1.5	
$f_{(DCO63)}$	R_{sel} = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	1.6	1.9	2.2	MHz
		V_{CC} = 3 V	1.69	2.0	2.29	
$f_{(DCO73)}$	R_{sel} = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	2.4	2.9	3.4	MHz
		V_{CC} = 3 V	2.7	3.2	3.65	
$f_{(DCO47)}$	R_{sel} = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V/3 V	f_{DCO40} × 1.7	f_{DCO40} × 2.1	f_{DCO40} × 2.5	MHz
$f_{(DCO77)}$	R_{sel} = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	V_{CC} = 2.2 V	4	4.5	4.9	MHz
		V_{CC} = 3 V	4.4	4.9	5.4	
S_{Rsel}	$S_R = f_{Rsel+1} / f_{Rsel}$	V_{CC} = 2.2 V/3 V	1.35	1.65	2	
S_{DCO}	$S_{DCO} = f_{(DCO+1)} / f_{(DCO)}$	V_{CC} = 2.2 V/3 V	1.07	1.12	1.16	
D_t	Temperature drift, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V_{CC} = 2.2 V	–0.31	–0.36	–0.40	%/°C
		V_{CC} = 3 V	–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation, R_{sel} = 4, DCO = 3, MOD = 0 (see Note 2)	V_{CC} = 2.2 V/3 V	0	5	10	%/V

NOTES: 1. The DCO frequency may not exceed the maximum system frequency defined by parameter processor frequency, $f_{(System)}$.
2. This parameter is not production tested.

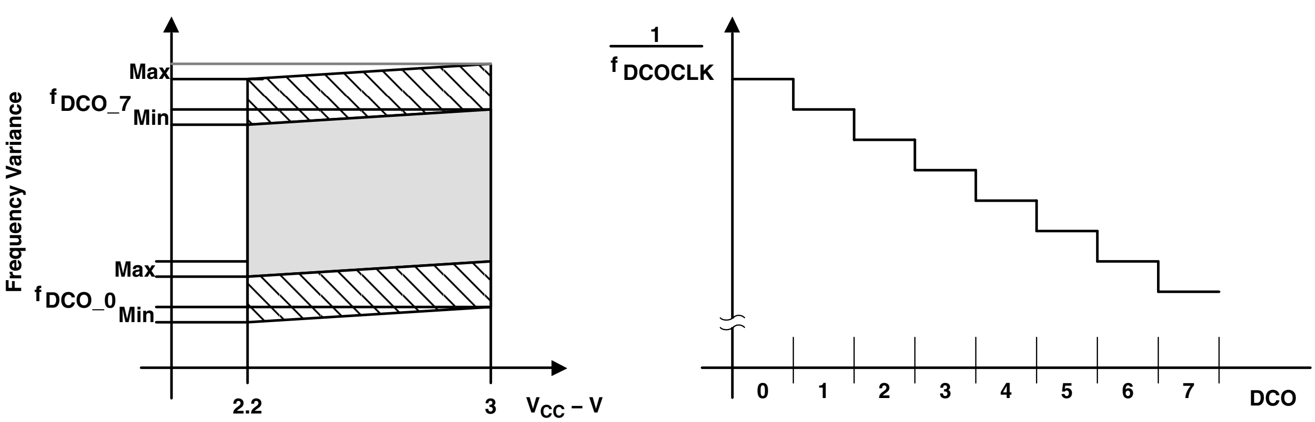


Figure 15. DCO Characteristics

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- Individual devices have a minimum and maximum operation frequency. The specified parameters for $f_{(DCOx0)}$ to $f_{(DCOx7)}$ are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1): Rsel0 overlaps Rsel1, ... Rsel6 overlaps Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often $f_{(DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{(DCO)} \times f_{(DCO+1)}}{MOD \times f_{(DCO)} + (32 - MOD) \times f_{(DCO+1)}}$$

DCO when using R_{OSC} (see Note 1)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{DCO}, DCO output frequency	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 1, T_A = 25°C	2.2 V		1.8±15%		MHz
		3 V		1.95±15%		MHz
D_t, Temperature drift	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V/3 V		±0.1		%/°C
D_V, Drift with V_{CC} variation	R_{sel} = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V/3 V		10		%/V

NOTES: 1. R_{OSC} = 100kΩ. Metal film resistor, type 0257. 0.6 watt with 1% tolerance and T_K = ±50ppm/°C.

crystal oscillator, LFXT1 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
C_{XIN}	Integrated input capacitance	XTS=0; LF oscillator selected, V_{CC} = 2.2 V/3 V			12		pF
		XTS=1; XT1 oscillator selected, V_{CC} = 2.2 V/3 V			2		
C_{XOUT}	Integrated output capacitance	XTS=0; LF oscillator selected, V_{CC} = 2.2 V/3 V			12		pF
		XTS=1; XT1 oscillator selected, V_{CC} = 2.2 V/3 V			2		
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 2)	XTS = 0 or 1 XT1 or LF modes	V_{SS}		0.2 × V_{CC}	V
V_{IH}			XTS = 0, LF mode	0.9 × V_{CC}		V_{CC}	
			XTS = 1, XT1 mode	0.8 × V_{CC}		V_{CC}	

NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

crystal oscillator, XT2 oscillator (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
C_{XIN}	Integrated input capacitance	V_{CC} = 2.2 V/3 V		2		pF
C_{XOUT}	Integrated output capacitance	V_{CC} = 2.2 V/3 V		2		pF
V_{IL}	Input levels at XIN	V_{CC} = 2.2 V/3 V (see Note 2)	V_{SS}		0.2 × V_{CC}	V
V_{IH}			0.8 × V_{CC}		V_{CC}	V

NOTES: 1. The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
2. Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

USART0, USART1 (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{(\tau)}$	USART0/USART1: deglitch time	V_{CC} = 2.2 V	200	430	800	ns
		V_{CC} = 3 V	150	280	500	

NOTE 1: The signal applied to the USART0/USART1 receive signal/terminal (URXD0/1) should meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum-timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0/1 line.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, power supply and input range conditions (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together AV_{SS} and DV_{SS} are connected together $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage range (see Note 2)	All P6.0/A0 to P6.7/A7 terminals. Analog inputs selected in ADC12MCTLx register and P6Sel.x=1 $0 \le x \le 7$; $V_{(AVSS)} \le V_{P6.x/Ax} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	Operating supply current into AV_{CC} terminal (see Note 3)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 1, REFON = 0 SHT0=0, SHT1=0, ADC12DIV=0	2.2 V		0.65	1.3	mA
			3 V		0.8	1.6	
I_{REF+}	Operating supply current into AV_{CC} terminal (see Note 4)	$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.8	mA
			3 V		0.5	0.8	
C_I †	Input capacitance	Only one terminal can be selected at one time, P6.x/Ax	2.2 V			40	pF
R_I†	Input MUX ON resistance	$0V \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω

† Not production tested, limits verified by design

NOTES: 1. The leakage current is defined in the leakage current table with P6.x/Ax parameter.
2. The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
3. The internal reference supply current is not included in current consumption parameter I_{ADC12}.
4. The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.

12-bit ADC, external reference (see Note 1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 2)		1.4		V_{AVCC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 3)		0		1.2	V
$(V_{eREF+} - V_{REF-}/V_{eREF-})$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (see Note 4)		1.4		V_{AVCC}	V
I_{VeREF+}	Static input current	$0V \le V_{eREF+} \le V_{AVCC}$	2.2 V/3 V			±1	µA
$I_{VREF-/VeREF-}$	Static input current	$0V \le V_{eREF-} \le V_{AVCC}$	2.2 V/3 V			±1	µA

NOTES: 1. The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
2. The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
3. The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
4. The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, built-in reference

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	3 V	2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$	2.2 V/3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REF2_5V = 0, $I_{VREF+}max \le I_{VREF+} \le I_{VREF+}min$		2.2			V
		REF2_5V = 1, –0.5mA $\le I_{VREF+} \le I_{VREF+}min$		2.8			
		REF2_5V = 1, –1mA $\le I_{VREF+} \le I_{VREF+}min$		2.9			
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V	0.01		–0.5	mA
			3 V	0.01		–1	
$I_{L(VREF)+}$ †	Load-current regulation V_{REF+} terminal	I_{VREF+} = 500 µA +/– 100 µA Analog input voltage ~0.75 V; REF2_5V = 0	2.2 V			±2	LSB
			3 V			±2	
		I_{VREF+} = 500 µA ± 100 µA Analog input voltage ~1.25 V; REF2_5V = 1	3 V			±2	LSB
$I_{DL(VREF)+}$ ‡	Load current regulation V_{REF+} terminal	I_{VREF+} =100 µA → 900 µA, C_{VREF+}=5 µF, ax ~0.5 x V_{REF+} Error of conversion result ≤ 1 LSB	3 V			20	ns
C_{VREF+}	Capacitance at pin V_{REF+} (see Note 1)	REFON =1, 0 mA $\le I_{VREF+} \le I_{VREF+}max$	2.2 V/3 V	5	10		µF
T_{REF+} †	Temperature coefficient of built-in reference	I_{VREF+} is a constant in the range of 0 mA $\le I_{VREF+} \le$ 1 mA	2.2 V/3 V			±100	ppm/°C
t_{REFON} †	Settle time of internal reference voltage (see Figure 16 and Note 2)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{REF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins V_{REF+} and AV_{SS} and V_{REF-}/V_{eREF-} and AV_{SS}: 10 µF tantalum and 100 nF ceramic.
2. The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

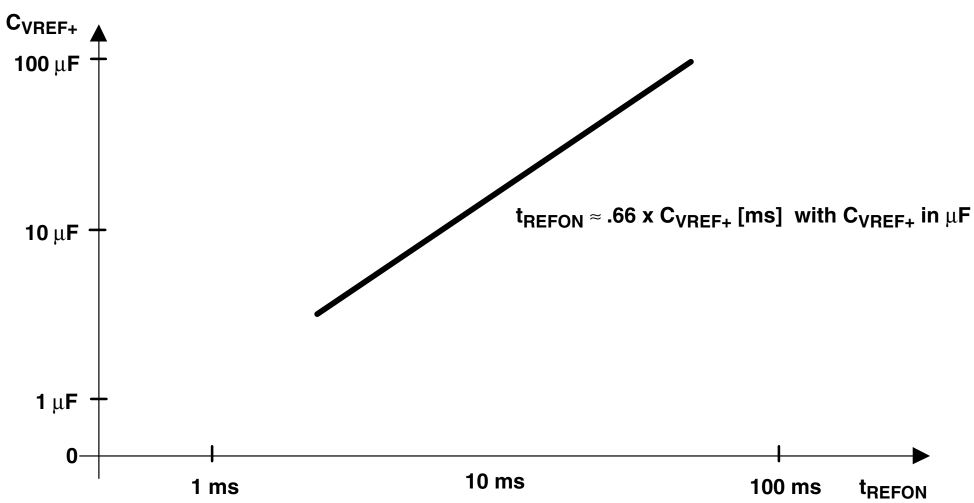


Figure 16. Typical Settling Time of Internal Reference t_{REFON} vs External Capacitor on V_{REF+}

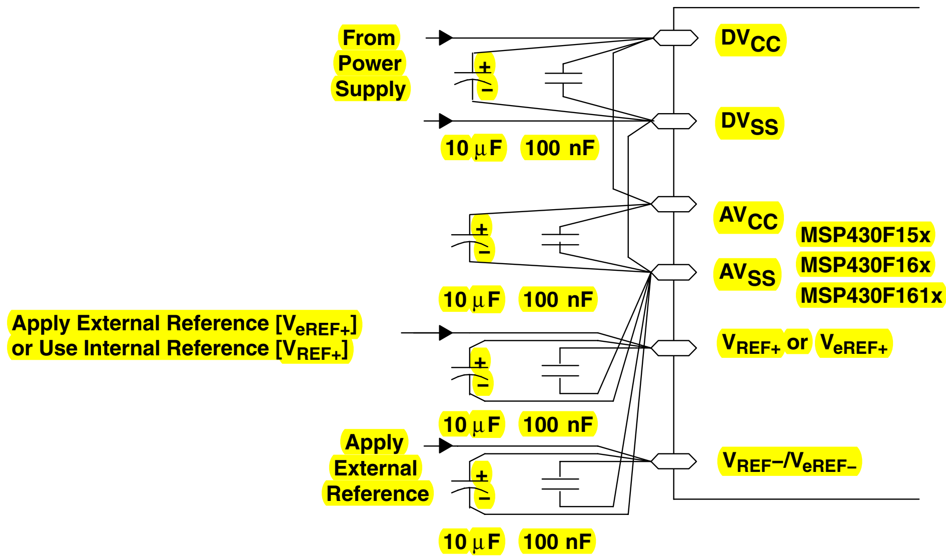


Figure 17. Supply Voltage and Reference Voltage Design V$_{REF-}$/V$_{eREF-}$ External Supply

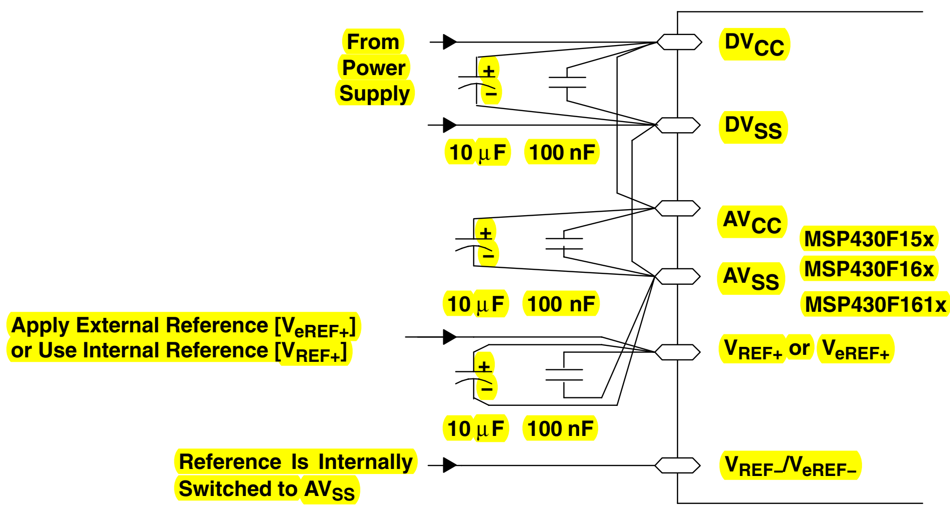


Figure 18. Supply Voltage and Reference Voltage Design V$_{REF-}$/V$_{eREF-}$ = AV$_{SS}$, Internally Connected

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, timing parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
$f_{ADC12CLK}$		For specified performance of ADC12 linearity parameters	2.2V/ 3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV=0, $f_{ADC12CLK}=f_{ADC12OSC}$	2.2 V/ 3 V	3.7	5	6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5\ \mu F$, Internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V/ 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK: ADC12SSEL ≠ 0			13×ADC12DIV× 1/$f_{ADC12CLK}$		µs
$t_{ADC12ON}$‡	Turn on settling time of the ADC	(see Note 1)				100	ns
t_{Sample}‡	Sampling time	$R_S = 400\ \Omega$, $R_I = 1000\ \Omega$, $C_I = 30$ pF, $\tau = [R_S + R_I] \times C_I$;(see Note 2)	3 V	1220			ns
			2.2 V	1400			

† Not production tested, limits characterized
‡ Not production tested, limits verified by design

NOTES: 1. The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
2. Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns where n = ADC resolution = 12, R_S = external source resistance.

12-bit ADC, linearity parameters

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ ($V_{eREF+} - V_{REF-}/V_{eREF-}$) min ≤ 1.6 V	2.2 V/3 V			±2	LSB
		1.6 V < ($V_{eREF+} - V_{REF-}/V_{eREF-}$) min ≤ [$V_{AVCC}$]				±1.7	
E_D	Differential linearity error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, $C_{VREF+} = 10\ \mu F$ (tantalum) and 100 nF (ceramic)	2.2 V/3 V			±1	LSB
E_O	Offset error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, Internal impedance of source $R_S < 100\ \Omega$, $C_{VREF+} = 10\ \mu F$ (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±4	LSB
E_G	Gain error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, $C_{VREF+} = 10\ \mu F$ (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±1.1	±2	LSB
E_T	Total unadjusted error	$(V_{eREF+} - V_{REF-}/V_{eREF-})_{min} \leq (V_{eREF+} - V_{REF-}/V_{eREF-})$, $C_{VREF+} = 10\ \mu F$ (tantalum) and 100 nF (ceramic)	2.2 V/3 V		±2	±5	LSB

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit ADC, temperature sensor and built-in V_{MID}

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal (see Note 1)	REFON = 0, INCH = 0Ah, ADC12ON=NA, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}†	(see Note 2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986		mV
			3 V		986		
TC_{SENSOR}†		ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55±3%	mV/°C
			3 V		3.55	3.55±3%	
$t_{SENSOR(sample)}$†	Sample time required if channel 10 is selected (see Note 3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11 (see Note 4)	ADC12ON = 1, INCH = 0Bh,	2.2 V			NA	µA
			3 V			NA	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is ~0.5 x V_{AVCC}	2.2 V		1.1	1.1±0.04	V
			3 V		1.5	1.50±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (see Note 5)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

† Not production tested, limits characterized

NOTES:
1. The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON=1), or (ADC12ON=1 AND INCH=0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is already included in I_{REF+}.
2. The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended in order to minimize the offset error of the built-in temperature sensor.
3. The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$
4. No additional current is needed. The V_{MID} is used during sampling.
5. The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

12-bit DAC, supply specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS}$ =0 V		2.20		3.60	V
I_{DD}	Supply Current: Single DAC Channel (see Notes 1 and 2)	DAC12AMPx=2, DAC12IR=0, DAC12_xDAT=0800h	2.2V/3V		50	110	µA
		DAC12AMPx=2, DAC12IR=1, DAC12_xDAT=0800h , V_{eREF+}=V_{REF+}= AV_{CC}	2.2V/3V		50	110	
		DAC12AMPx=5, DAC12IR=1, DAC12_xDAT=0800h, V_{eREF+}=V_{REF+}= AV_{CC}	2.2V/3V		200	440	
		DAC12AMPx=7, DAC12IR=1, DAC12_xDAT=0800h, V_{eREF+}=V_{REF+}= AV_{CC}	2.2V/3V		700	1500	
PSRR	Power supply rejection ratio (see Notes 3 and 4)	DAC12_xDAT = 800h, V_{REF} = 1.5 V ΔAV_{CC} = 100mV	2.2V		70		dB
		DAC12_xDAT = 800h, V_{REF} = 1.5 V or 2.5 V ΔAV_{CC} = 100mV	3V				

NOTES:
1. No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
2. Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
3. PSRR = 20*log{$\Delta AV_{CC}/\Delta V_{DAC12\_xOUT}$}.
4. V_{REF} is applied externally. The internal reference is not used.

electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (see Figure 19)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	(12-bit Monotonic)		12			bits
INL	Integral nonlinearity (see Note 1)	V_{ref} = 1.5 V DAC12AMPx = 7, DAC12IR = 1	2.2V		±2.0	±8.0	LSB
		V_{ref} = 2.5 V DAC12AMPx = 7, DAC12IR = 1	3V				
DNL	Differential nonlinearity (see Note 1)	V_{ref} = 1.5 V DAC12AMPx = 7, DAC12IR = 1	2.2V		±0.4	±1.0	LSB
		V_{ref} = 2.5 V DAC12AMPx = 7, DAC12IR = 1	3V				
E_O	Offset voltage w/o calibration (see Notes 1, 2)	V_{ref} = 1.5 V DAC12AMPx = 7, DAC12IR = 1	2.2V			±21	mV
		V_{ref} = 2.5 V DAC12AMPx = 7, DAC12IR = 1	3V				
	Offset voltage with calibration (see Notes 1, 2)	V_{ref} = 1.5 V DAC12AMPx = 7, DAC12IR = 1	2.2V			±2.5	
		V_{ref} = 2.5 V DAC12AMPx = 7, DAC12IR = 1	3V				
$d_{E(O)}/d_T$	Offset error temperature coefficient (see Note 1)		2.2V/3V		30		uV/C
E_G	Gain error (see Note 1)	V_{REF} = 1.5 V	2.2V			±3.50	% FSR
		V_{REF} = 2.5 V	3V				
$d_{E(G)}/d_T$	Gain temperature coefficient (see Note 1)		2.2V/3V		10		ppm of FSR/°C
t_{Offset_Cal}	Time for offset calibration (see Note 3)	DAC12AMPx=2	2.2V/3V			100	ms
		DAC12AMPx=3,5	2.2V/3V			32	
		DAC12AMPx=4,6,7	2.2V/3V			6	

NOTES: 1. Parameters calculated from the best-fit curve from 0x0A to 0xFFF. The best-fit curve method is used to deliver coefficients “a” and “b” of the first order equation: y = a + b*x. $V_{DAC12\_xOUT} = E_O + (1 + E_G) * (V_{eREF+}/4095) *$ DAC12_xDAT, DAC12IR = 1.
2. The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
3. The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx ={0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

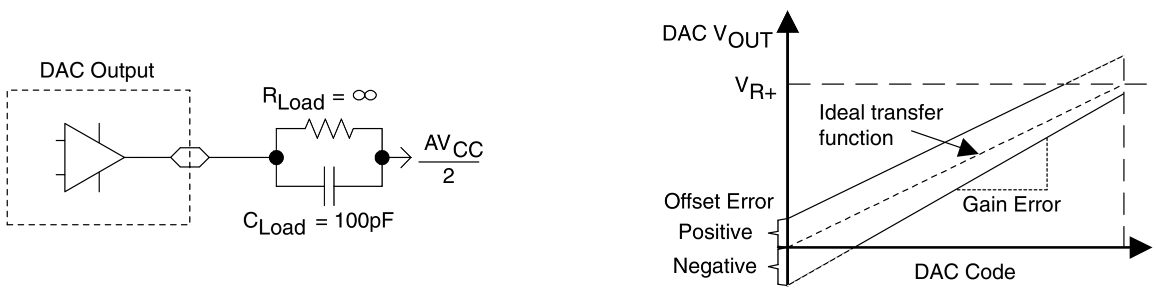
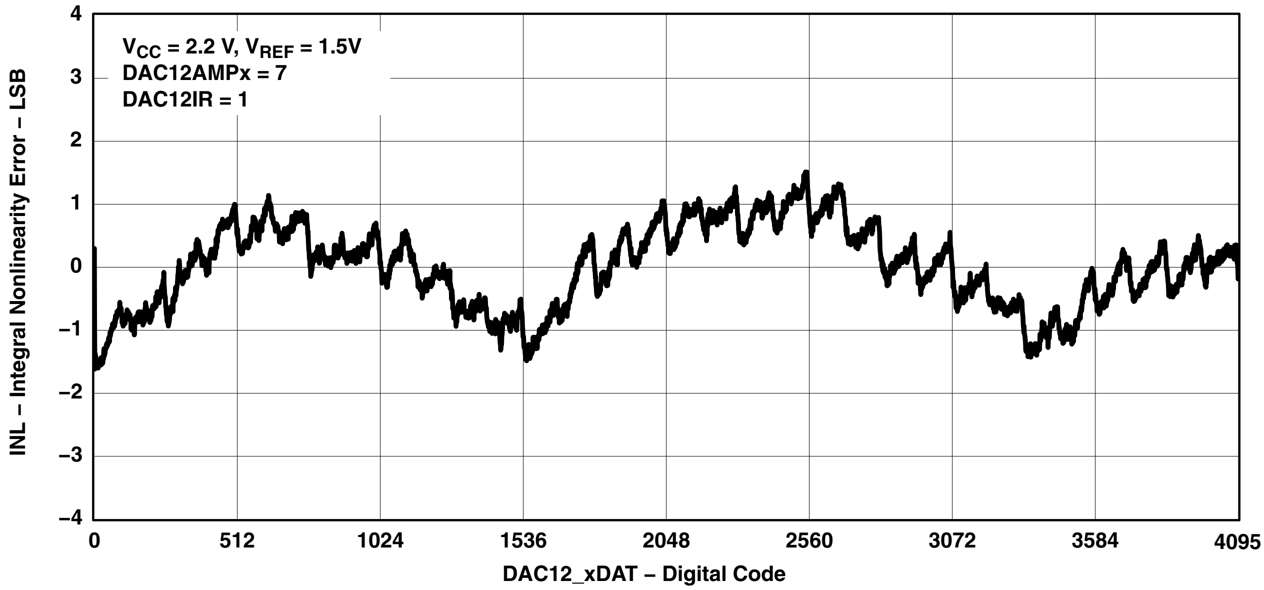


Figure 19. Linearity Test Load Conditions and Gain/Offset Definition

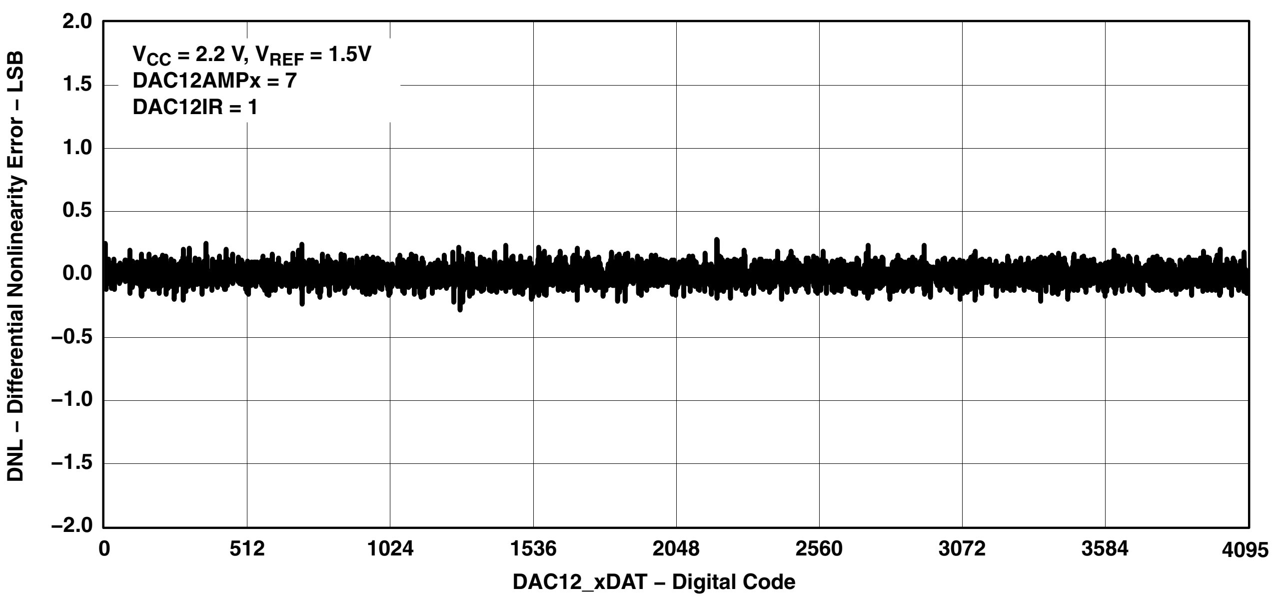
electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, linearity specifications (continued)

TYPICAL INL ERROR
vs
DIGITAL INPUT DATA



TYPICAL DNL ERROR
vs
DIGITAL INPUT DATA



electrical characteristics over recommended operating free-air temperature (unless otherwise noted) (continued)

12-bit DAC, output specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range (see Note 1, Figure 22)	No Load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.005	V
		No Load, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV_{CC}−0.05		AV_{CC}	
		R_{Load}= 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	0		0.1	V
		R_{Load}= 3 kΩ, $Ve_{REF+} = AV_{CC}$, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7	2.2V/3V	AV_{CC}−0.13		AV_{CC}	V
$C_{L(DAC12)}$	Max DAC12 load capacitance		2.2V/3V			100	pF
$I_{L(DAC12)}$	Max DAC12 load current		2.2V	−0.5		+0.5	mA
			3V	−1.0		+1.0	mA
$R_{O/P(DAC12)}$	Output Resistance (see Figure 22)	R_{Load}= 3 kΩ, $V_{O/P(DAC12)}$ = 0 V, DAC12AMPx = 7, DAC12_xDAT = 0h	2.2V/3V		150	250	Ω
		R_{Load}= 3 kΩ, $V_{O/P(DAC12)} = AV_{CC}$, DAC12AMPx = 7, DAC12_xDAT = 0FFFh	2.2V/3V		150	250	
		R_{Load}= 3 kΩ, $0.3\ V \le V_{O/P(DAC12)} \le AV_{CC} - 0.3\ V$, DAC12AMPx = 7	2.2V/3V		1	4	

NOTES: 1. Data is valid after the offset calibration of the output amplifier.

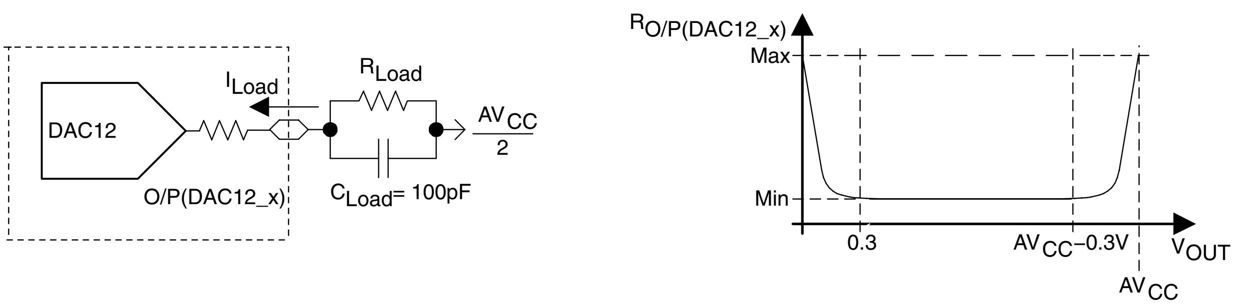


Figure 22. DAC12_x Output Resistance Tests

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

12-bit DAC, reference input specifications

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Ve_{REF+}	Reference input voltage range	DAC12IR=0, (see Notes 1 and 2)	2.2V/3V		$AV_{CC}/3$	$AV_{CC}+0.2$	V
		DAC12IR=1, (see Notes 3 and 4)	2.2V/3V		AVcc	AVcc+0.2	
$Ri_{(VREF+)}$, $Ri_{(VeREF+)}$	Reference input resistance	DAC12_0 IR=DAC12_1 IR =0	2.2V/3V	20			MΩ
		DAC12_0 IR=1, DAC12_1 IR = 0	2.2V/3V	40	48	56	kΩ
		DAC12_0 IR=0, DAC12_1 IR = 1	2.2V/3V				
		DAC12_0 IR=DAC12_1 IR =1 DAC12_0 SREFx = DAC12_1 SREFx (see Note 5)	2.2V/3V	20	24	28	kΩ

NOTES: 1. For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AV_{CC}).
2. The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} - V_{E(O)}] / [3^*(1 + E_G)]$.
3. For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AV_{CC}).
4. The maximum voltage applied at reference input voltage terminal $Ve_{REF+} = [AV_{CC} - V_{E(O)}] / (1 + E_G)$.
5. When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-bit DAC, dynamic specifications; $V_{ref} = V_{CC}$, DAC12IR = 1 (see Figure 23 and Figure 24)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on-time	DAC12_xDAT = 800h, $Error_{V(O)} < \pm 0.5$ LSB (see Note 1,Figure 23)	DAC12AMPx=0 → {2, 3, 4}	2.2V/3V		60	120	µs
			DAC12AMPx=0 → {5, 6}	2.2V/3V		15	30	
			DAC12AMPx=0 → 7	2.2V/3V		6	12	
$t_{S(FS)}$	Settling time,full-scale	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V		100	200	µs
			DAC12AMPx=3,5	2.2V/3V		40	80	
			DAC12AMPx=4,6,7	2.2V/3V		15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h→ 408h→ 3F8h BF8h→ C08h→ BF8h	DAC12AMPx=2	2.2V/3V		5		µs
			DAC12AMPx=3,5	2.2V/3V		2		
			DAC12AMPx=4,6,7	2.2V/3V		1		
SR	Slew Rate	DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V	0.05	0.12		V/µs
			DAC12AMPx=3,5	2.2V/3V	0.35	0.7		
			DAC12AMPx=4,6,7	2.2V/3V	1.5	2.7		
Glitch energy: full-scale		DAC12_xDAT = 80h→ F7Fh→ 80h	DAC12AMPx=2	2.2V/3V		10		nV-s
			DAC12AMPx=3,5	2.2V/3V		10		
			DAC12AMPx=4,6,7	2.2V/3V		10		

NOTES: 1. R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 23.
2. Slew rate applies to output voltage steps >= 200mV.

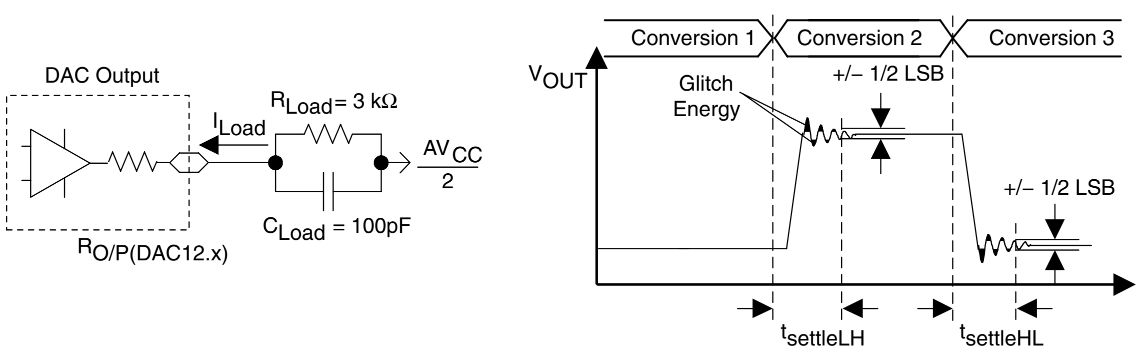


Figure 23. Settling Time and Glitch Energy Testing

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

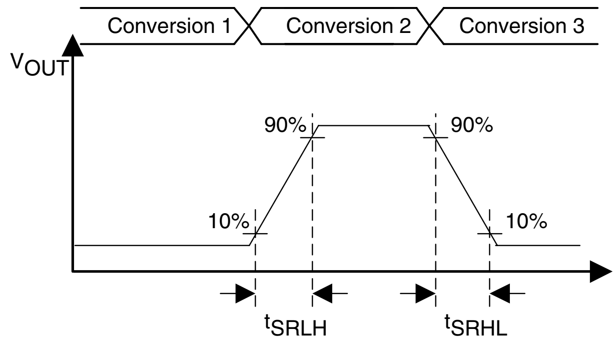


Figure 24. Slew Rate Testing

12-bit DAC, dynamic specifications continued (T_A = 25°C unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC}=1.5V, V_{AC}=0.1V_{PP} (see Figure 25)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2V/3V	550			
Channel to channel crosstalk (see Note 1 and Figure 26)		DAC12_0DAT = 800h, No Load, DAC12_1DAT = 80h<–>F7Fh, R_{Load} = 3kΩ f_{DAC12_1OUT} = 10kHz @ 50/50 duty cycle	2.2V/3V		–80		dB
		DAC12_0DAT = 80h<–>F7Fh, R_{Load} = 3kΩ, DAC12_1DAT = 800h, No Load f_{DAC12_0OUT} = 10kHz @ 50/50 duty cycle	2.2V/3V		–80		

NOTES: 1. R_{LOAD} = 3 kΩ, C_{LOAD} = 100 pF

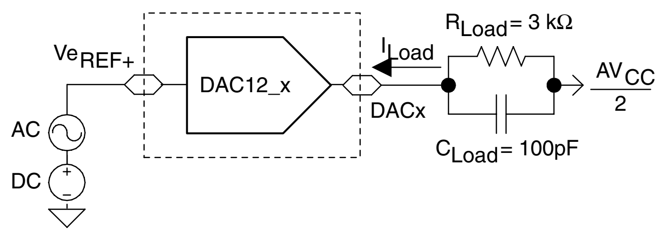


Figure 25. Test Conditions for 3-dB Bandwidth Specification

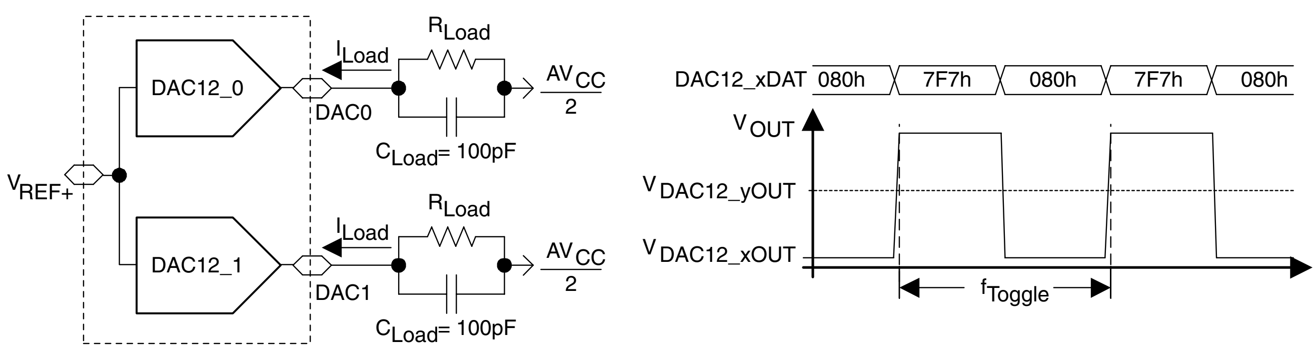


Figure 26. Crosstalk Test Conditions

electrical characteristics over recommended operating free-air temperature (unless otherwise noted)

Flash Memory

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.7		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.7 V/ 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time	see Note 2	2.7 V/ 3.6 V	200			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 3			35		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				30		
$t_{Block, 1-63}$	Block program time for each additional byte or word				21		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				5297		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. The mass erase duration generated by the flash timing generator is at least 11.1ms (= 5297x1/f_{FTG},max = 5297x1/476kHz). To achieve the required cumulative mass erase time the Flash Controller's mass erase operation can be repeated until this time is met. (A worst case minimum of 19 cycles are required).
3. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

JTAG Interface

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-up resistance on TMS, TCK, TDI/TCLK	see Note 2	2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.
2. TMS, TDI/TCLK, and TCK pull-up resistors are implemented in all versions.

JTAG Fuse (see Note 1)

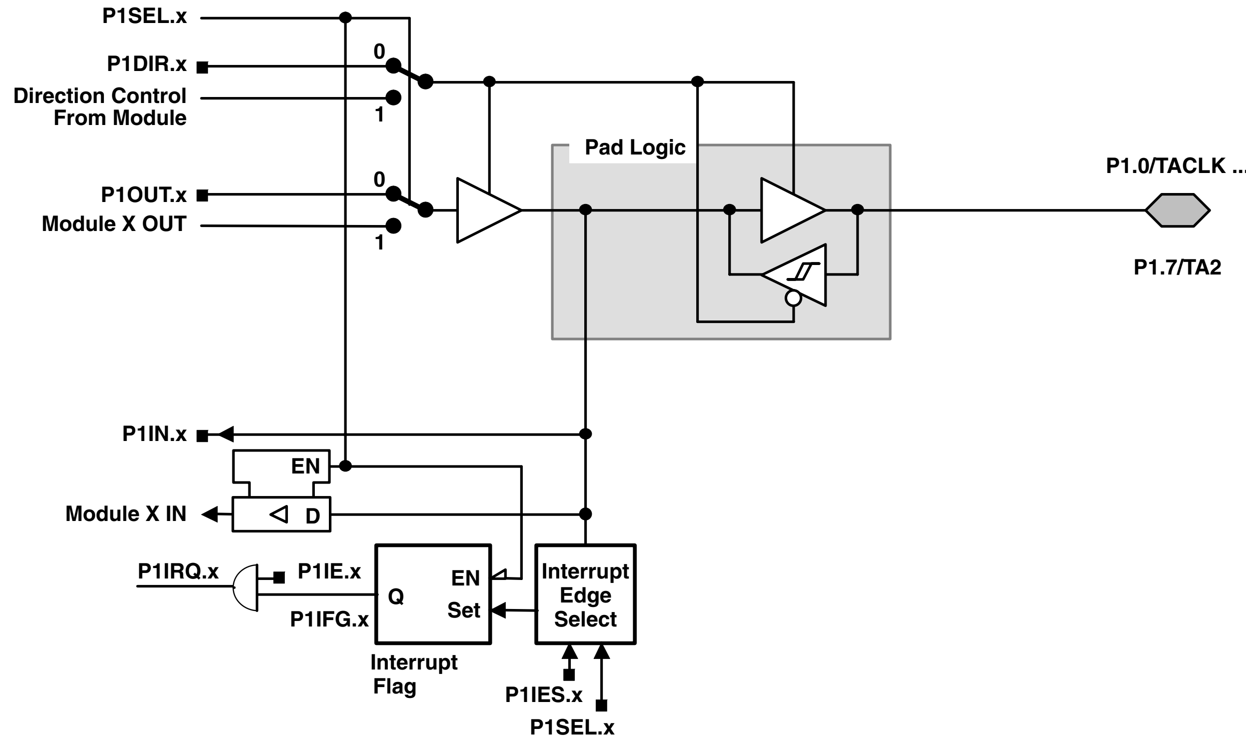
PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TDI/TCLK for fuse-blow: F versions			6		7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

APPLICATION INFORMATION

input/output schematic

port P1, P1.0 to P1.7, input/output with Schmitt-trigger



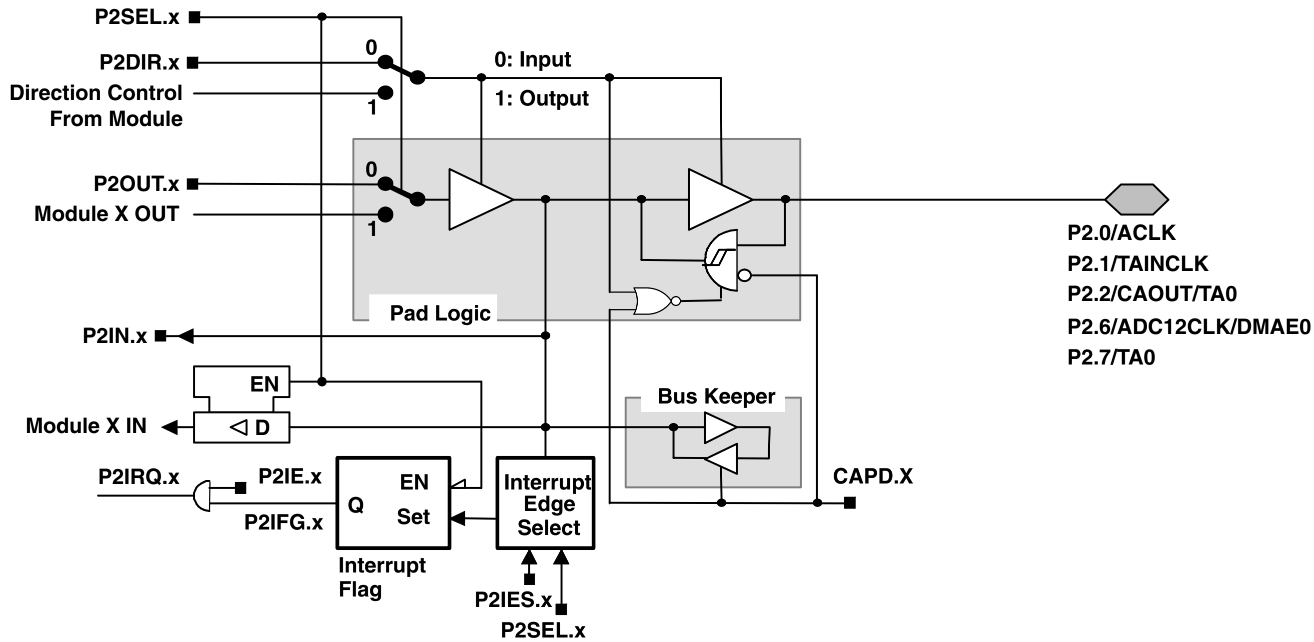
PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	DV_{SS}	P1IN.0	TACLK†	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal†	P1IN.1	CCI0A†	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal†	P1IN.2	CCI1A†	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal†	P1IN.3	CCI2A†	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal†	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal†	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal†	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

† Signal from or to Timer_A

APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.0 to P2.2, P2.6, and P2.7 input/output with Schmitt-trigger



x: Bit Identifier 0 to 2, 6, and 7 for Port P2

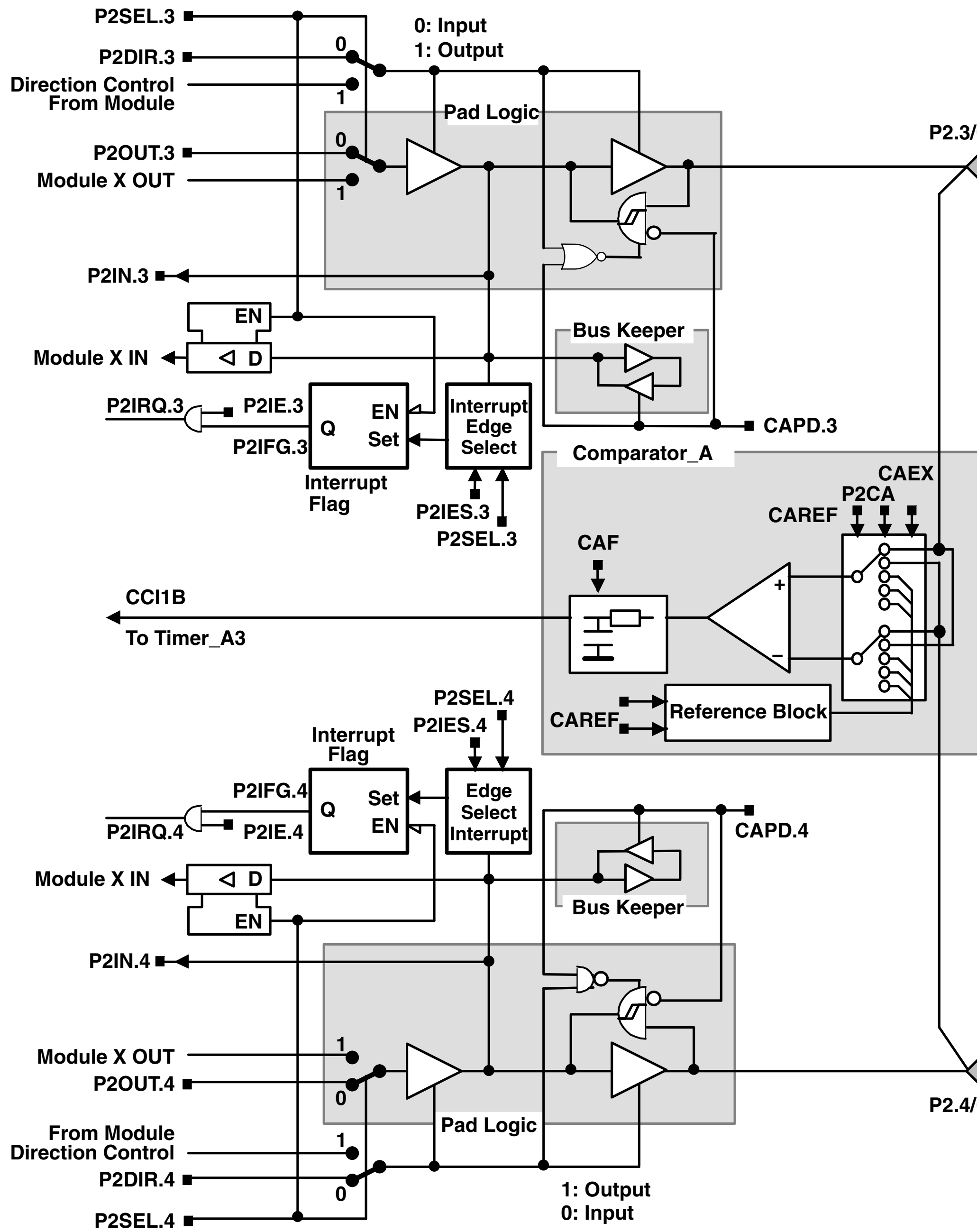
PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DV_{SS}	P2IN.1	INCLK‡	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT†	P2IN.2	CCI0B‡	P2IE.2	P2IFG.2	P2IES.2
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	ADC12CLK¶	P2IN.6	DMAE0#	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	Out0 signal§	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

† Signal from Comparator_A
‡ Signal to Timer_A
§ Signal from Timer_A
¶ ADC12CLK signal is output of the 12-bit ADC module
# Signal to DMA, channel 0, 1 and 2

APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.3 to P2.4, input/output with Schmitt-trigger



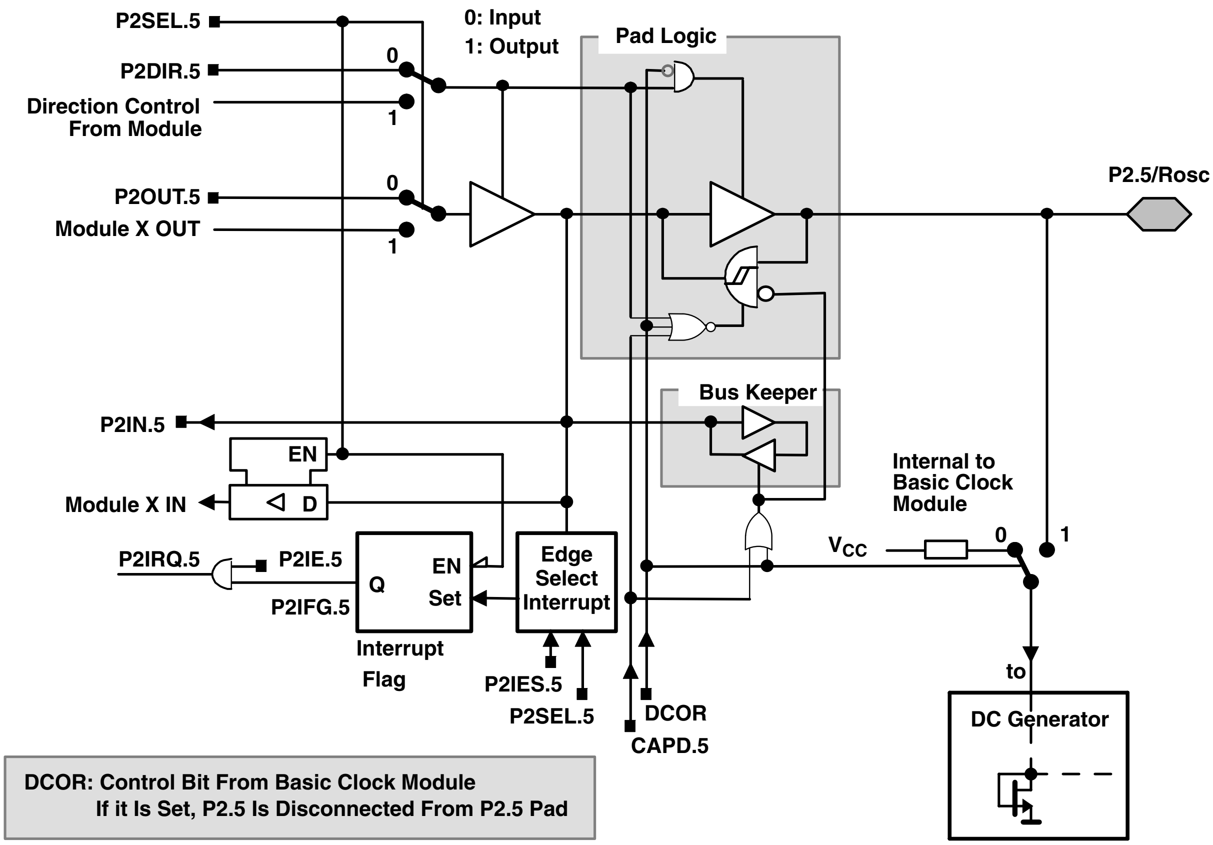
PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal†	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal†	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4

† Signal from Timer_A

APPLICATION INFORMATION

input/output schematic (continued)

port P2, P2.5, input/output with Schmitt-trigger and R_{osc} function for the basic clock module

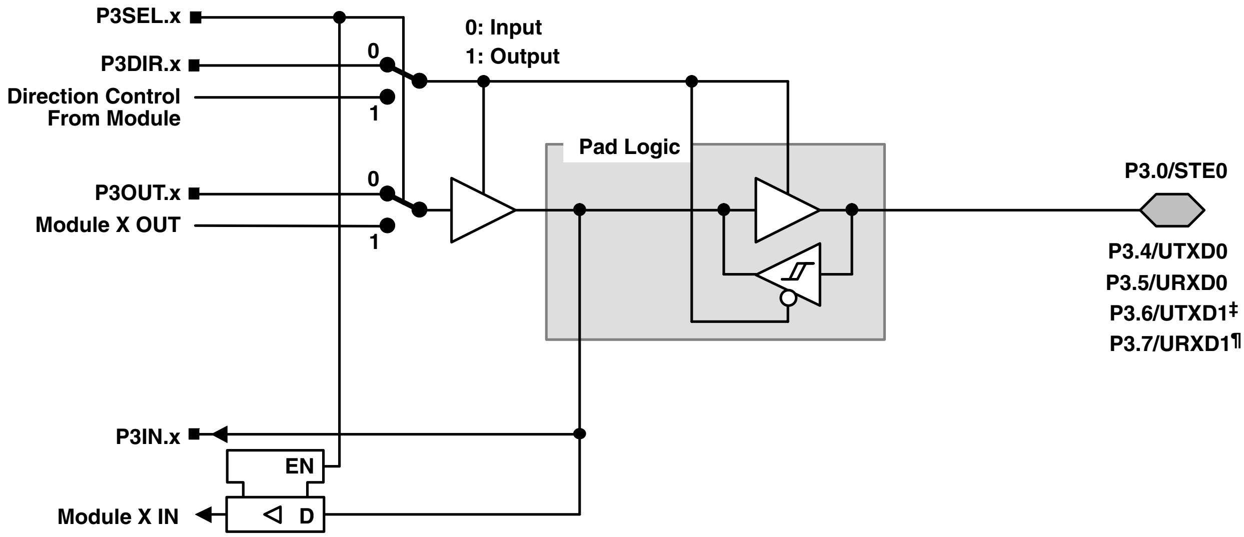


PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DV_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

APPLICATION INFORMATION

input/output schematic (continued)

port P3, P3.0 and P3.4 to P3.7, input/output with Schmitt-trigger



x: Bit Identifier, 0 and 4 to 7 for Port P3

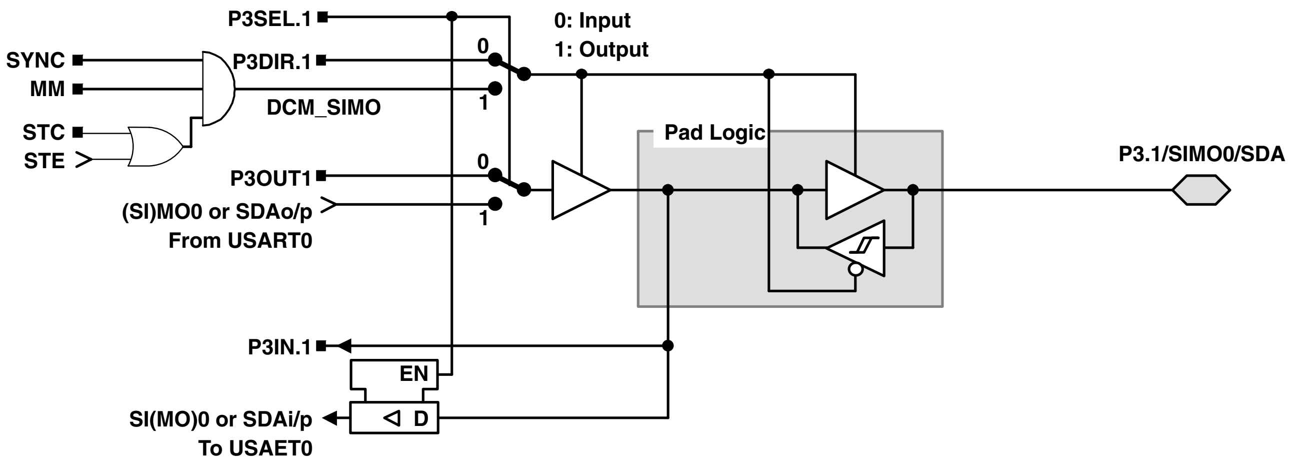
PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	DV_{CC}	P3OUT.4	UTXD0†	P3IN.4	Unused
P3Sel.5	P3DIR.5	DV_{SS}	P3OUT.5	DV_{SS}	P3IN.5	URXD0§
P3Sel.6	P3DIR.6	DV_{CC}	P3OUT.6	UTXD1‡	P3IN.6	Unused
P3Sel.7	P3DIR.7	DV_{SS}	P3OUT.7	DV_{SS}	P3IN.7	URXD1¶

† Output from USART0 module
‡ Output from USART1 module
‡ Input to USART0 module
¶ Input to USART1 module

APPLICATION INFORMATION

input/output schematic (continued)

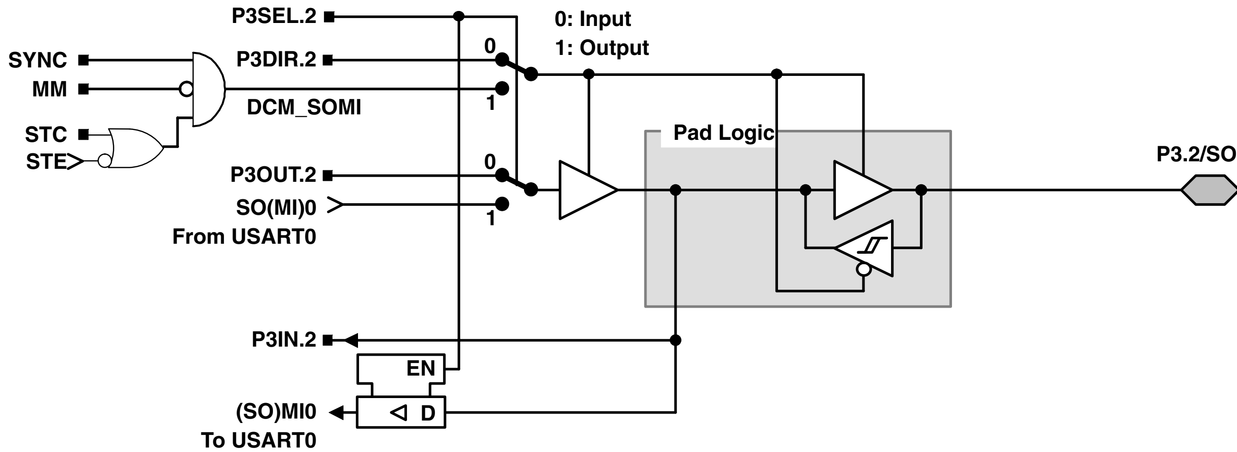
port P3, P3.1, input/output with Schmitt-trigger



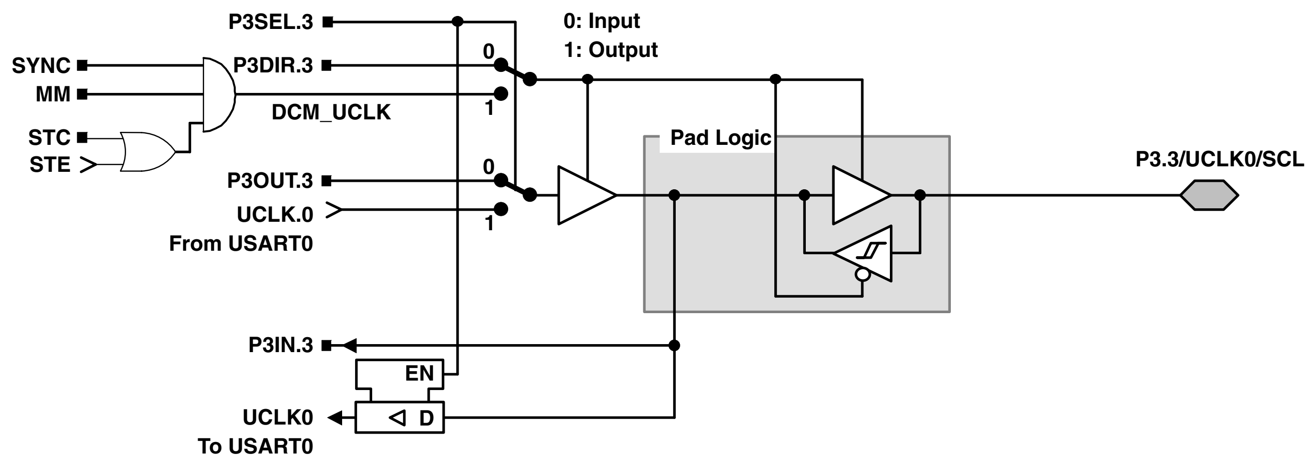
APPLICATION INFORMATION

input/output schematic (continued)

port P3, P3.2, input/output with Schmitt-trigger



port P3, P3.3, input/output with Schmitt-trigger

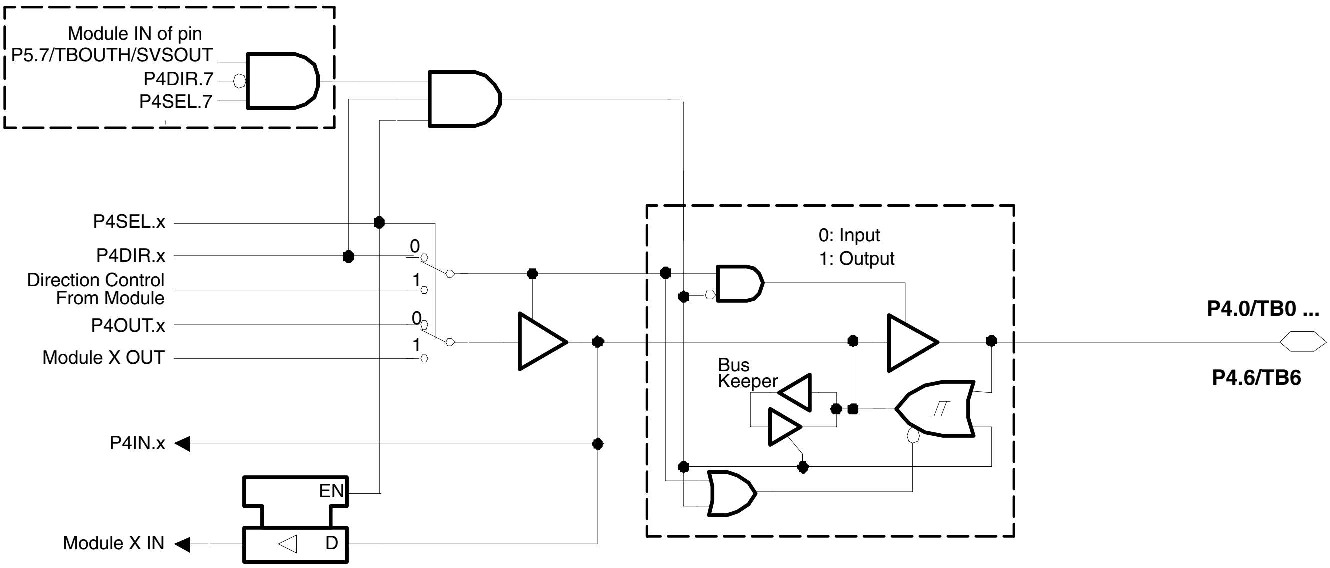


NOTE: UART mode:		The UART clock can only be an input. If UART mode and UART function are selected, the P3.3/UCLK0 is always an input.
	SPI, slave mode:	The clock applied to UCLK0 is used to shift data in and out.
	SPI, master mode:	The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).
	I^2C, slave mode:	The clock applied to SCL is used to shift data in and out. The frequency of the clock source of the module must be ≥ 10 times the frequency of the SCL clock.
	I^2C, master mode:	To shift data in and out, the clock is supplied via the SCL terminal to all I^2C slaves. The frequency of the clock source of the module must be ≥ 10 times the frequency of the SCL clock.

APPLICATION INFORMATION

input/output schematic (continued)

port P4, P4.0 to P4.6, input/output with Schmitt-trigger



x: Bit Identifier, 0 to 6 for Port P4

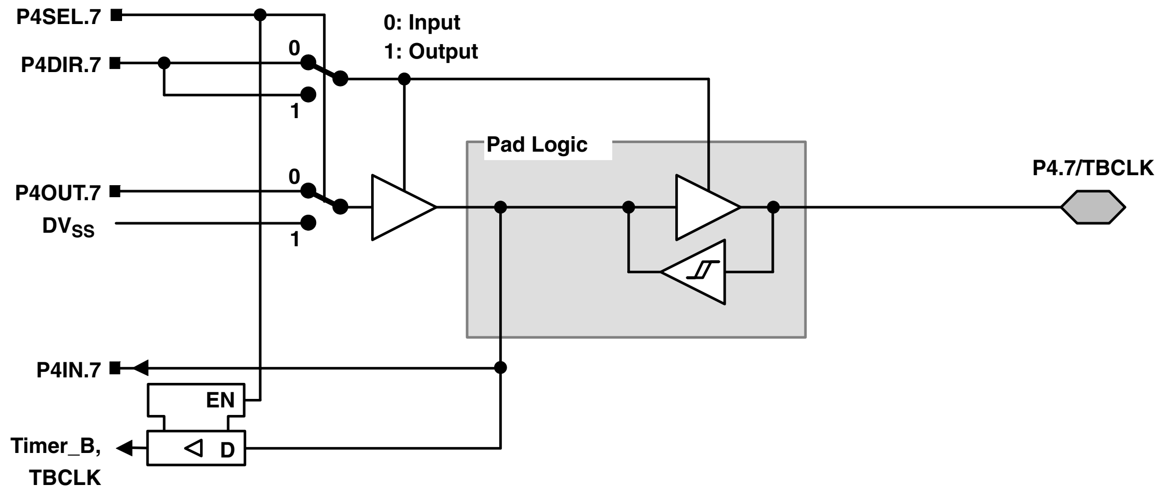
PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	Out0 signal†	P4IN.0	CCI0A / CCI0B‡
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	Out1 signal†	P4IN.1	CCI1A / CCI1B‡
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	Out2 signal†	P4IN.2	CCI2A / CCI2B‡
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	Out3 signal†	P4IN.3	CCI3A / CCI3B‡
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	Out4 signal†	P4IN.4	CCI4A / CCI4B‡
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	Out5 signal†	P4IN.5	CCI5A / CCI5B‡
P4Sel.6	P4DIR.6	P4DIR.6	P4OUT.6	Out6 signal†	P4IN.6	CCI6A

† Signal from Timer_B
‡ Signal to Timer_B

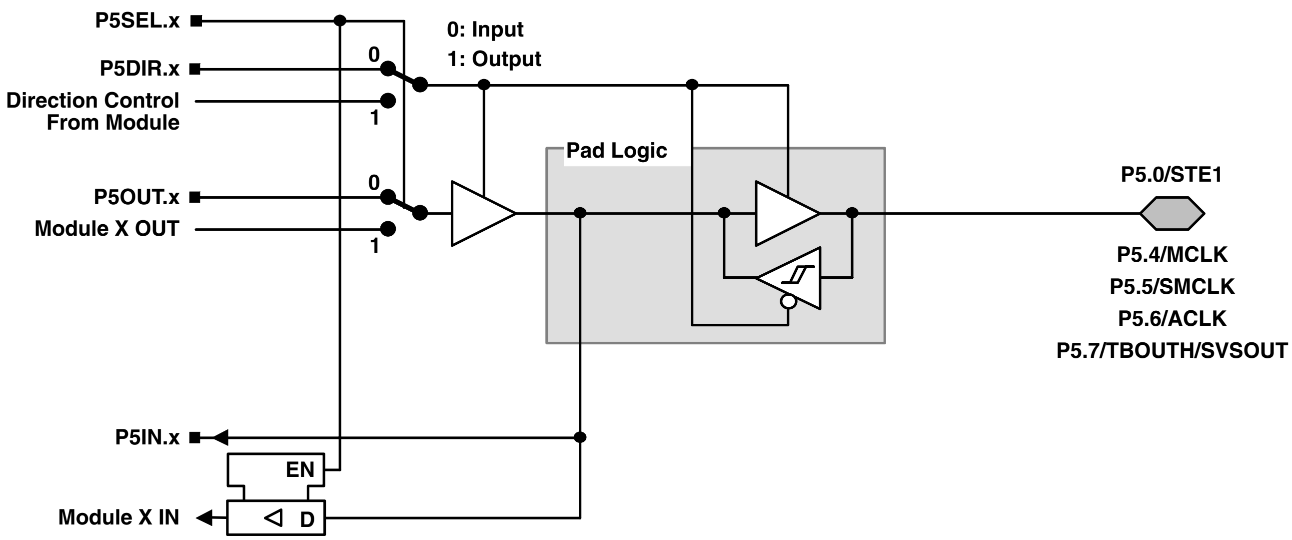
APPLICATION INFORMATION

input/output schematic (continued)

port P4, P4.7, input/output with Schmitt-trigger



port P5, P5.0 and P5.4 to P5.7, input/output with Schmitt-trigger



x: Bit Identifier, 0 and 4 to 7 for Port P5

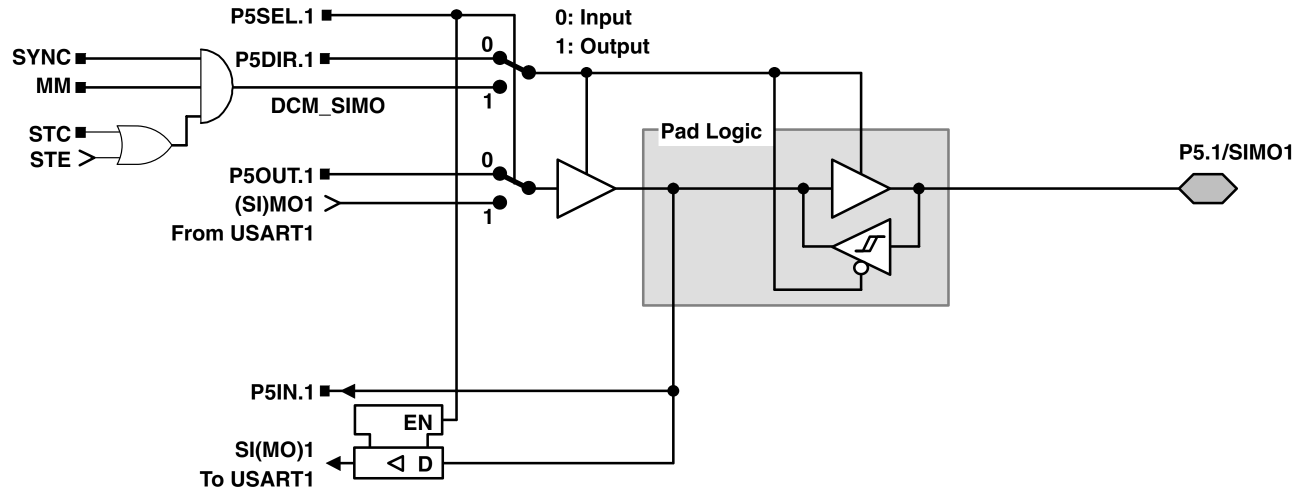
PnSel.x	PnDIR.x	Dir. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P5Sel.0	P5DIR.0	DV_{SS}	P5OUT.0	DV_{SS}	P5IN.0	STE.1
P5Sel.4	P5DIR.4	DV_{CC}	P5OUT.4	MCLK	P5IN.4	unused
P5Sel.5	P5DIR.5	DV_{CC}	P5OUT.5	SMCLK	P5IN.5	unused
P5Sel.6	P5DIR.6	DV_{CC}	P5OUT.6	ACLK	P5IN.6	unused
P5Sel.7	P5DIR.7	DV_{SS}	P5OUT.7	SVSOUT	P5IN.7	TBOUTHiZ

NOTE: TBOUTHiZ signal is used by port module P4, pins P4.0 to P4.6. The function of TBOUTHiZ is mainly useful when used with Timer_B7.

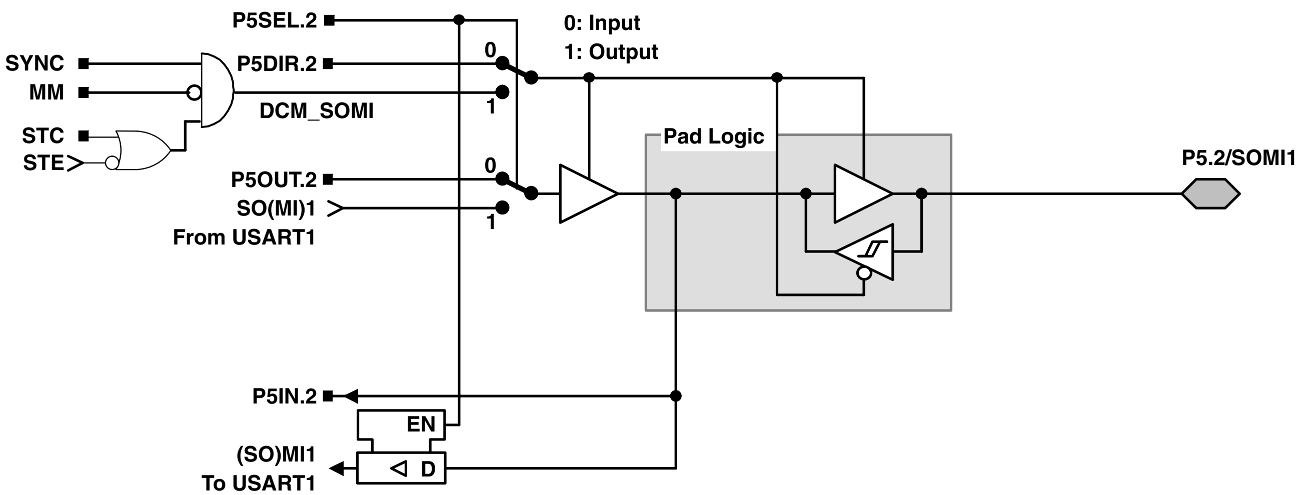
APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.1, input/output with Schmitt-trigger



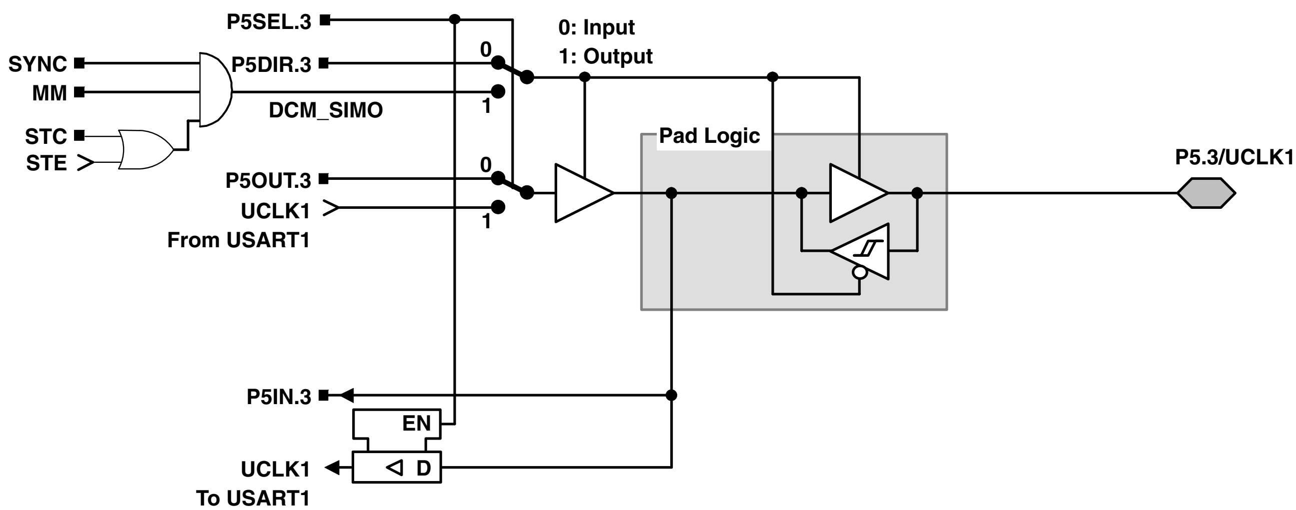
port P5, P5.2, input/output with Schmitt-trigger



APPLICATION INFORMATION

input/output schematic (continued)

port P5, P5.3, input/output with Schmitt-trigger

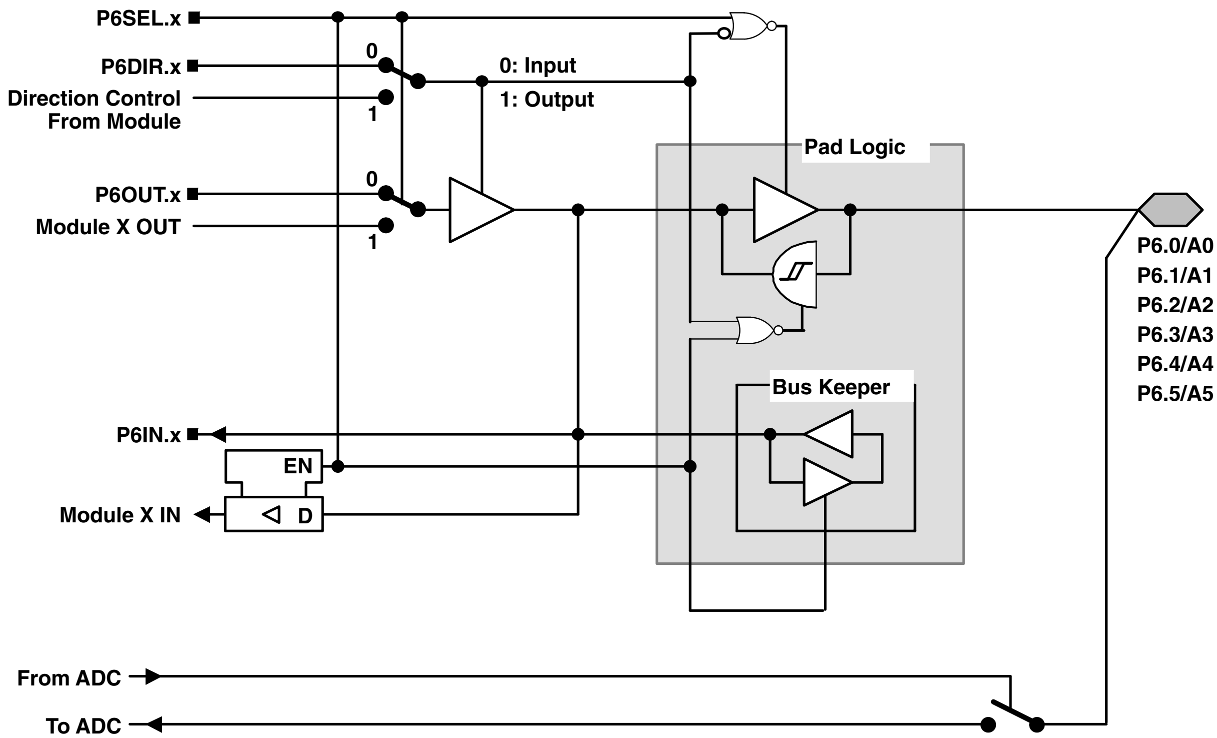


NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, the P5.3/UCLK1 direction is always input.
SPI, slave mode: The clock applied to UCLK1 is used to shift data in and out.
SPI, master mode: The clock to shift data in and out is supplied to connected devices on pin P5.3/UCLK1 (in slave mode).

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.0 to P6.5, input/output with Schmitt-trigger



x: Bit Identifier, 0 to 5 for Port P6

NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1←0. The value of the throughput current depends on the driving capability of the gate. For MSP430, it is approximately 100 µA.
Use P6SEL.x=1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

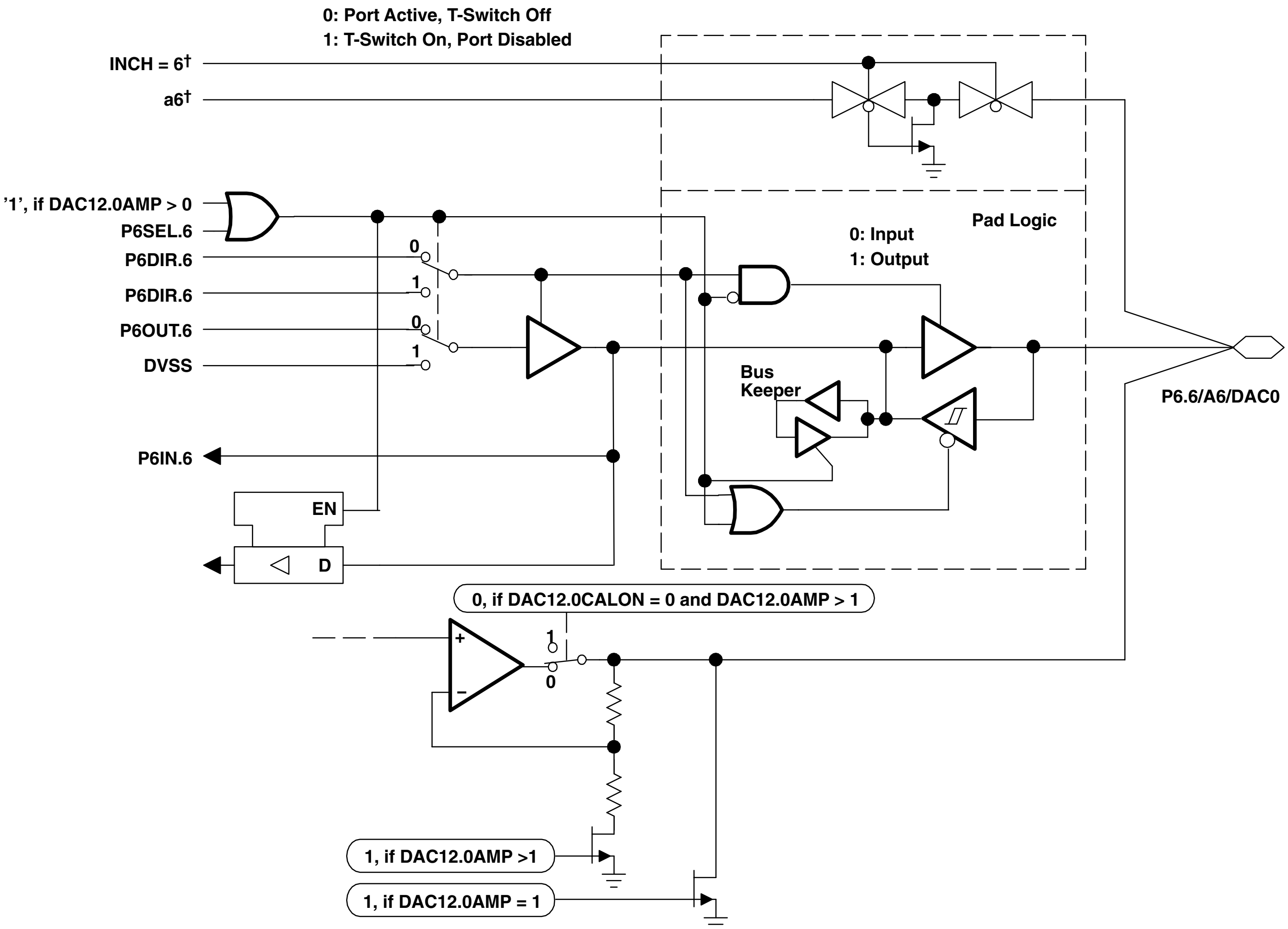
PnSel.x	PnDIR.x	DIR. CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused

NOTE: The signal at pins P6.x/Ax is used by the 12-bit ADC module.

APPLICATION INFORMATION

input/output schematic (continued)

port P6, P6.6, input/output with Schmitt-trigger

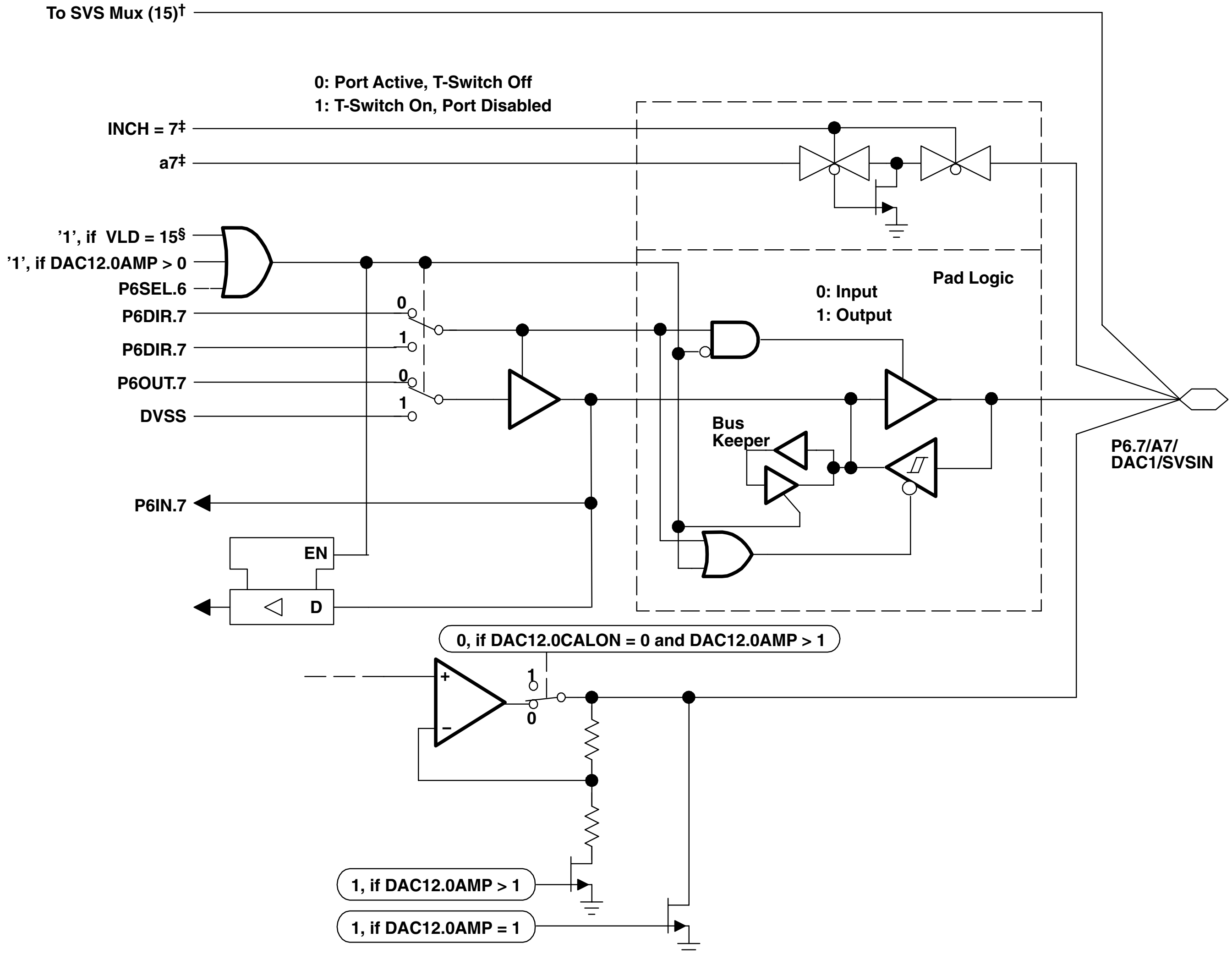


†Signal from or to ADC12

APPLICATION INFORMATION

input/output schematic (continued)

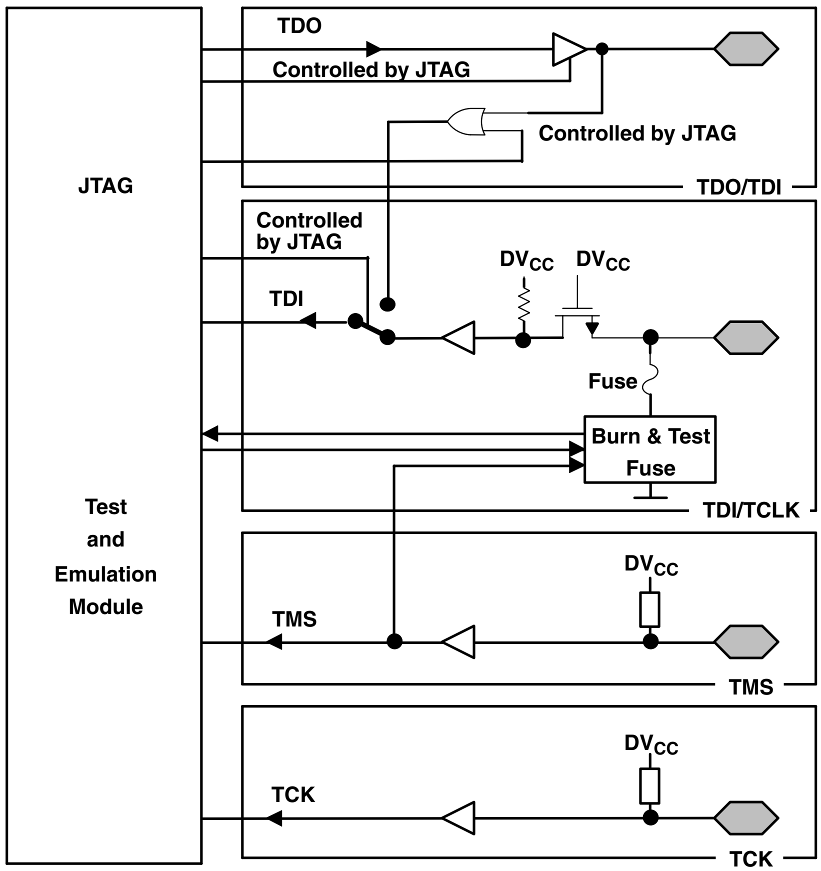
port P6, P6.7, input/output with Schmitt-trigger



†Signal to SVS Block, Selected if VLD = 15
‡Signal From or To ADC12
§VLD Control Bits are Located in SVS

APPLICATION INFORMATION

JTAG pins TMS, TCK, TDI/TCLK, TDO/TDI, input/output with Schmitt-trigger



During Programming Activity and During Blowing of the Fuse, Pin TDO/TDI Is Used to Apply the Test Input Data for JTAG Circuitry

APPLICATION INFORMATION

JTAG fuse check mode

MSP430 devices that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 27). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

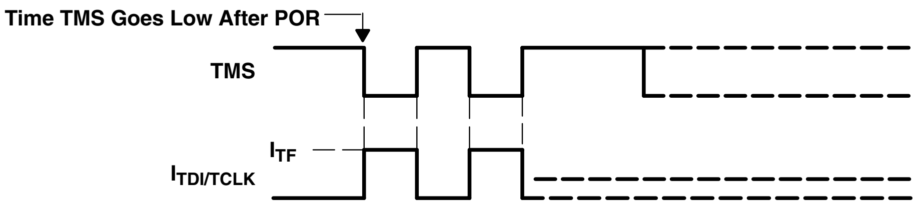


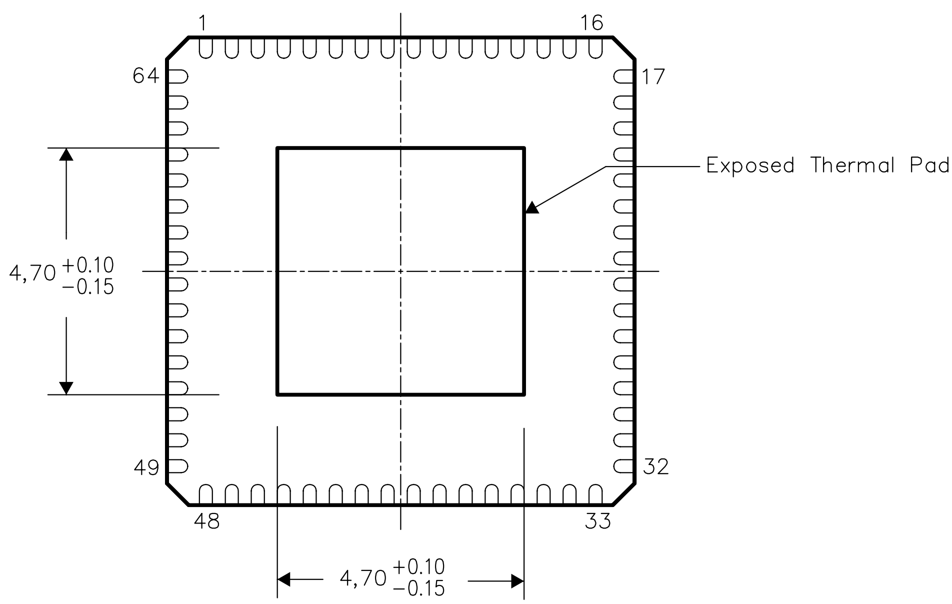
Figure 27. Fuse Check Mode Current, MSP430x15x/16x/161x

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MSP430F155IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F155IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F155IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F155IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F156IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F156IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F156IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F156IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F157IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F157IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F157IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F157IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1610IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1610IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1610IRTD	ACTIVE	QFN	RTD	64		TBD	Call TI	Call TI
MSP430F1610IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1610IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1611IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1611IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1611IRTD	ACTIVE	QFN	RTD	64		TBD	Call TI	Call TI
MSP430F1611IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1611IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F1612IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1612IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F1612IRTD	ACTIVE	QFN	RTD	64		TBD	Call TI	Call TI
MSP430F1612IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
MSP430F1612IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F167IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F167IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F167IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F167IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F168IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F168IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F168IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F168IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F169IPM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F169IPMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
MSP430F169IRTDR	ACTIVE	QFN	RTD	64	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR
MSP430F169IRTDT	ACTIVE	QFN	RTD	64	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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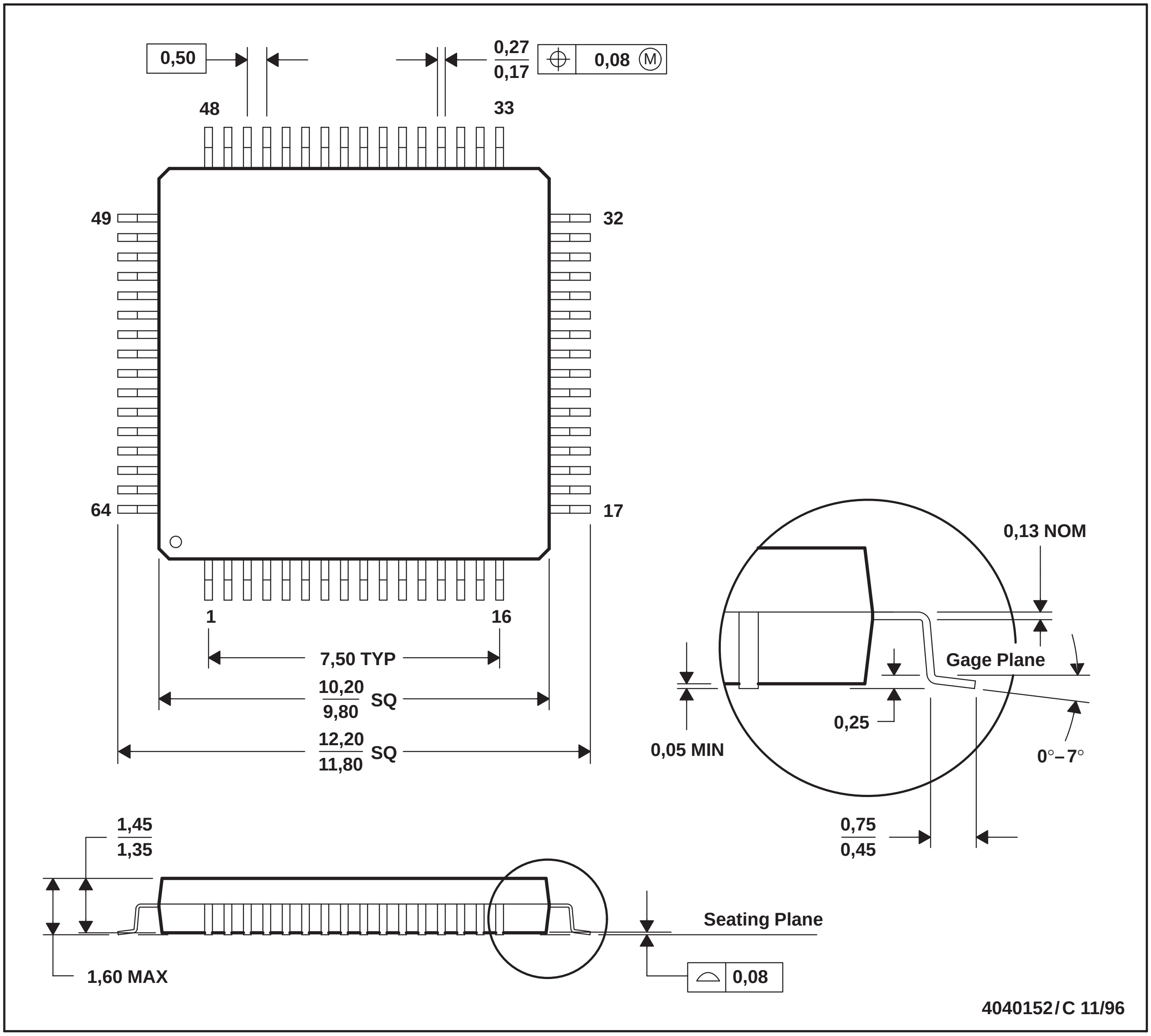
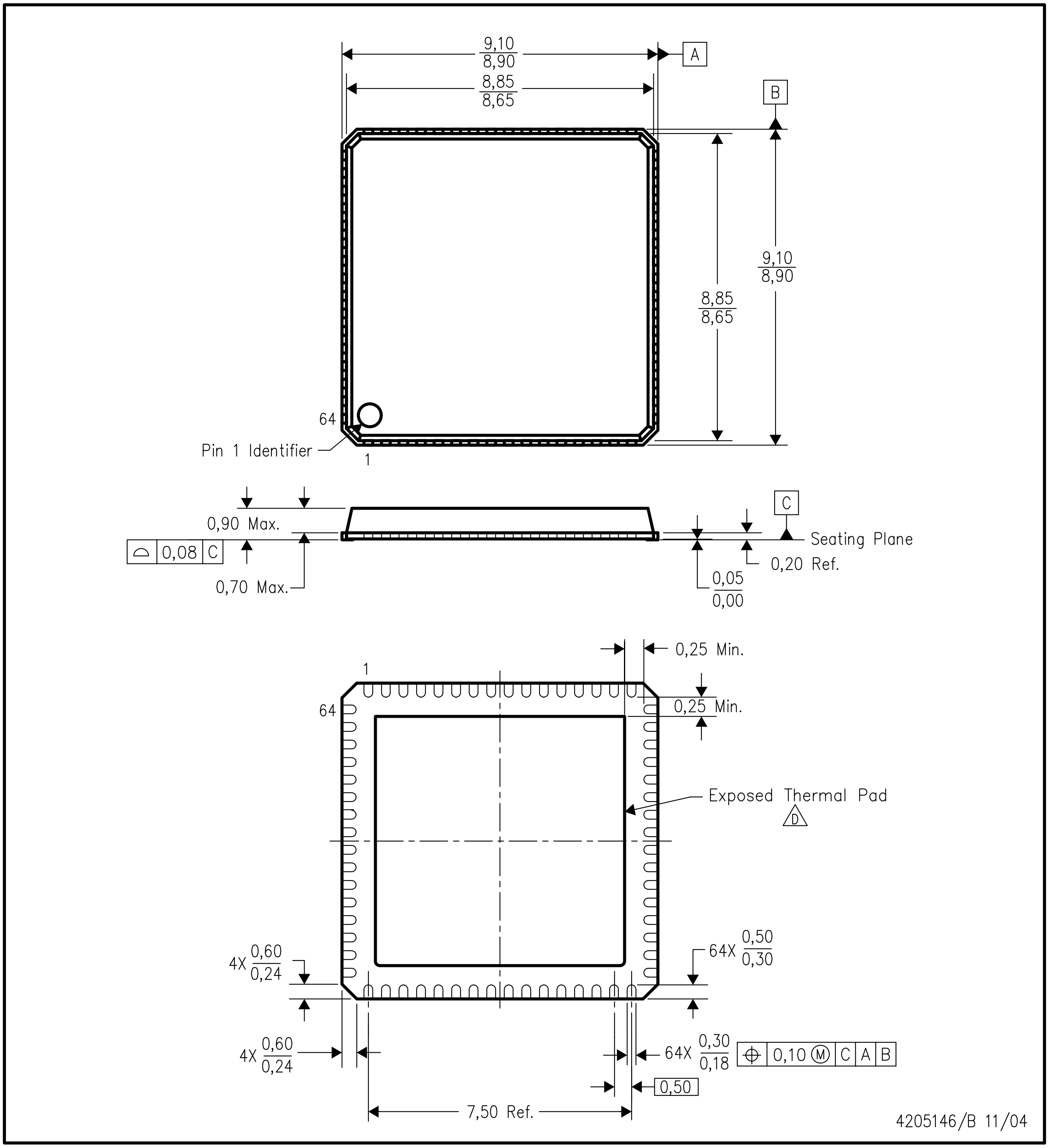
PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

RTD (S–PQFP–N64) PLASTIC QUAD FLATPACK



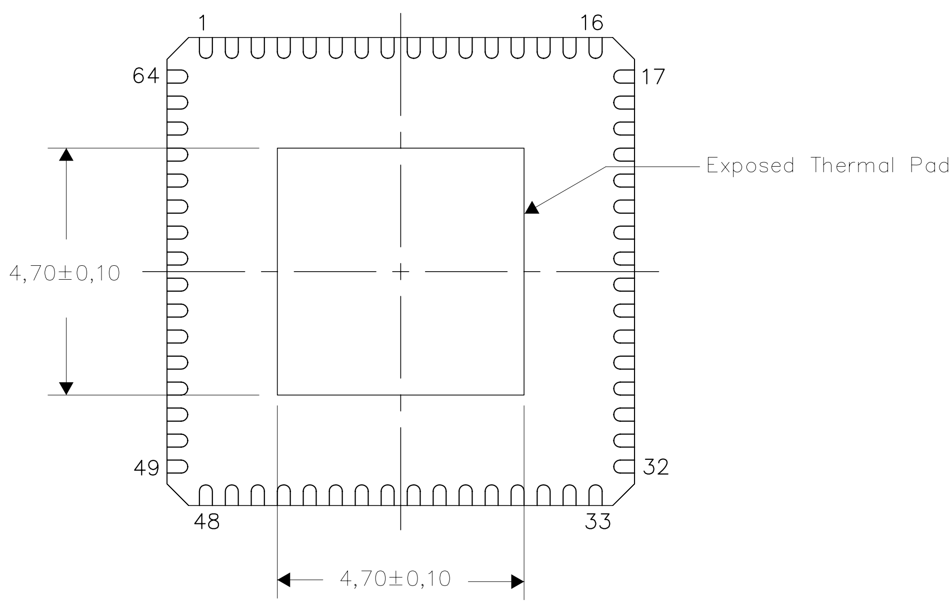
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

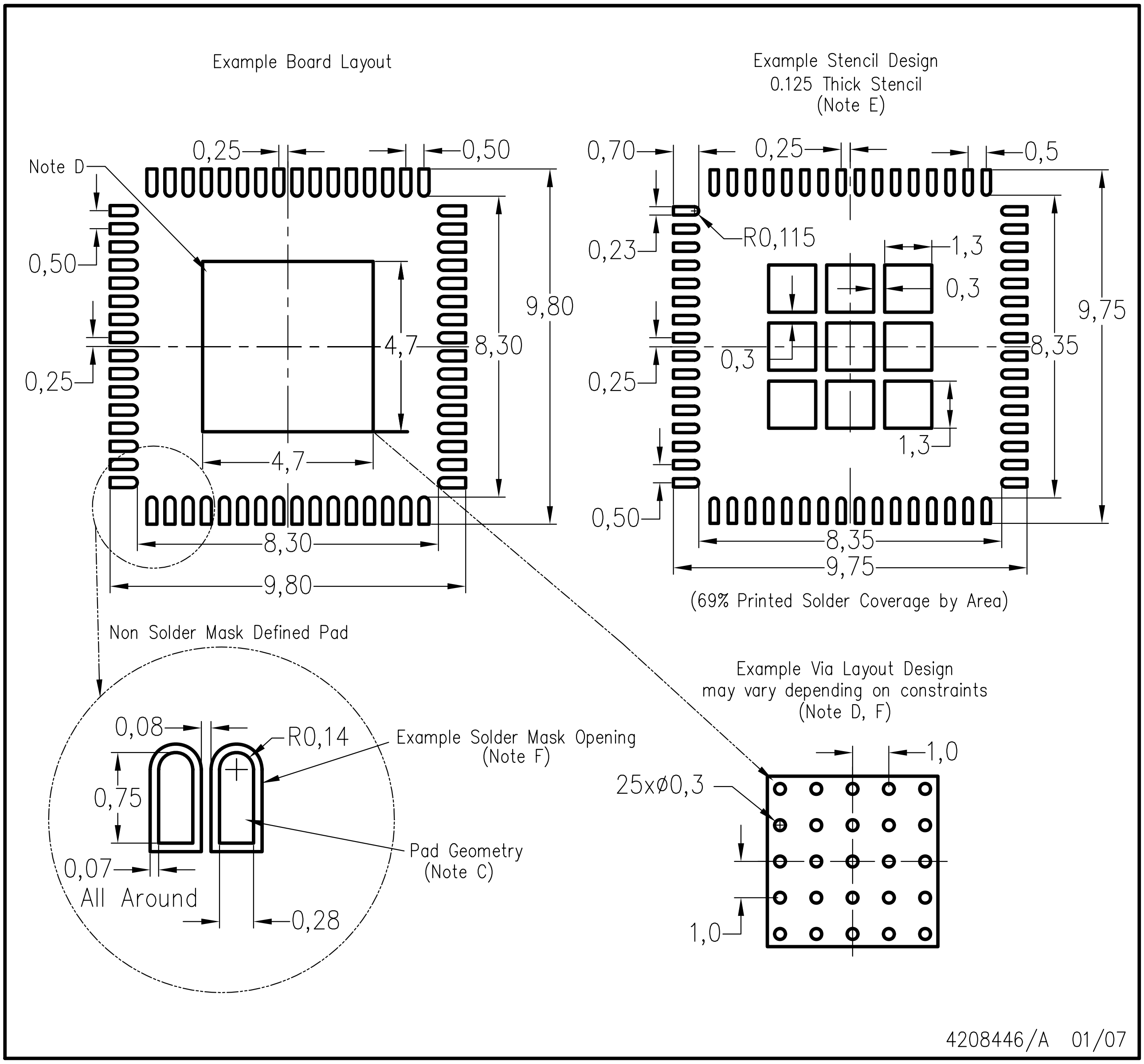


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RTD (S–PQFP–N64)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Package, Texas Instruments Literature No. SCBA017 and SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customer should contact their board fabrication site for recommended solder mask tolerances and vias tenting recommendations for vias placed int the thermal pad.