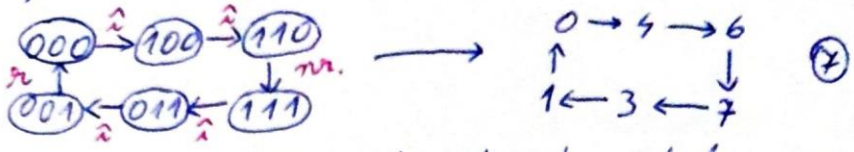
Cireș Estera- proiect CID

CIREȘ ESTERA - 7-G-III

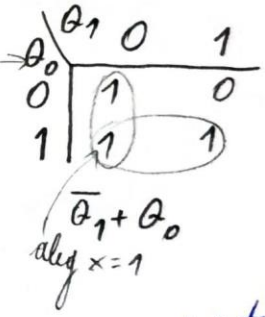


Tabelul de adevăr aferent automatului secvențial, care surprinde informația despre starea actuală și cea viitoare (6)

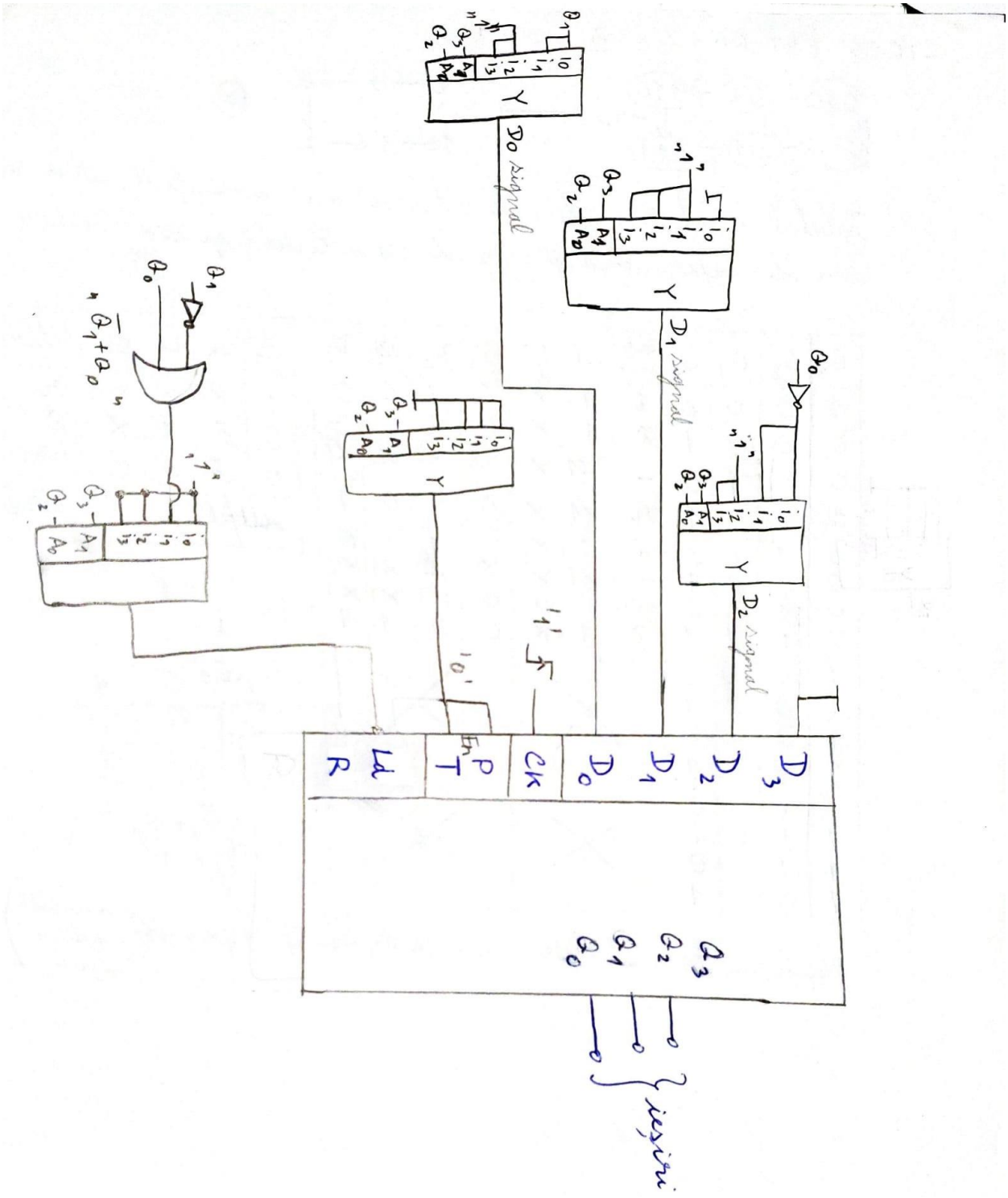
Q_3	Q_2	Q_1	Q_0	acțiune	Ld	PT	D_3	D_2	D_1	D_0
0	0	0	0	$\hat{\imath}$	1	×	0	1	0	0
0	0	0	1	$\hat{\imath}$	1	×	0	0	0	0
0	0	1	0	–	×1	×	×0	×1	×0	×1
0	0	1	1	r	×1	×	0	0	0	1
0	1	0	0	$\hat{\imath}$	1	×	0	1	1	0
0	1	0	1	–	×1	×	×0	×0	×1	×0
0	1	1	0	nr.	0	0	0	×1	×1	×1
0	1	1	1	$\hat{\imath}$	1	×	0	0	1	1
1	0	0	0		1					
1	0	0	1		1					
1	0	1	0		×					
1	0	1	1		1					
1	1	0	0		1					
1	1	0	1		1					
1	1	1	0		×					
1	1	1	1		1					

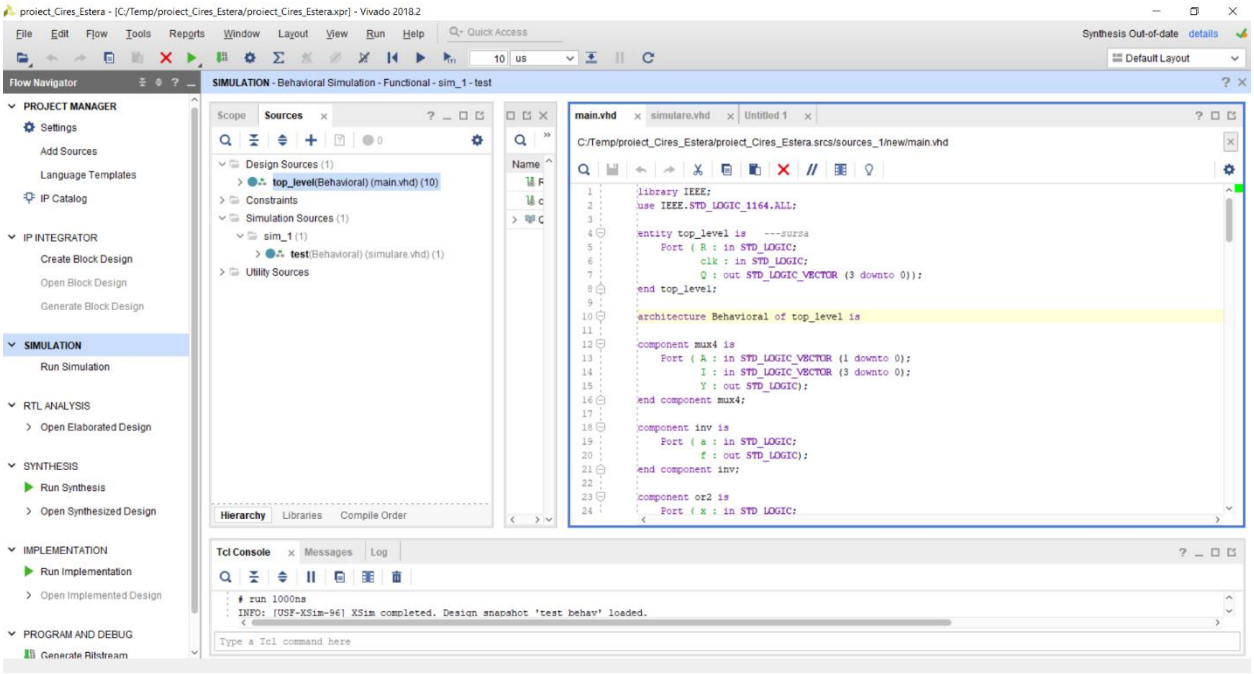
En

r	Clk	Ld	En	Acțiune
1	×	×	×	r
0	↓	1	×	$\hat{\imath}$
0	↓	0	0	nr.
altfel				așteaptă



Implementare cu MUX 4:1 și porți logice / MUX 4:1 ← 4 intrări, 2 adrese, 1 ieșire


D0 signal
D1 signal
D2 signal
'1'
'0'
R
Ld
T
P
Ck
D0
D1
D2
D3
Q3
Q2
Q1
Q0
ieșiri


proiect_Cires_Estera - [C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.xpr] - Vivado 2018.2
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main.vhd
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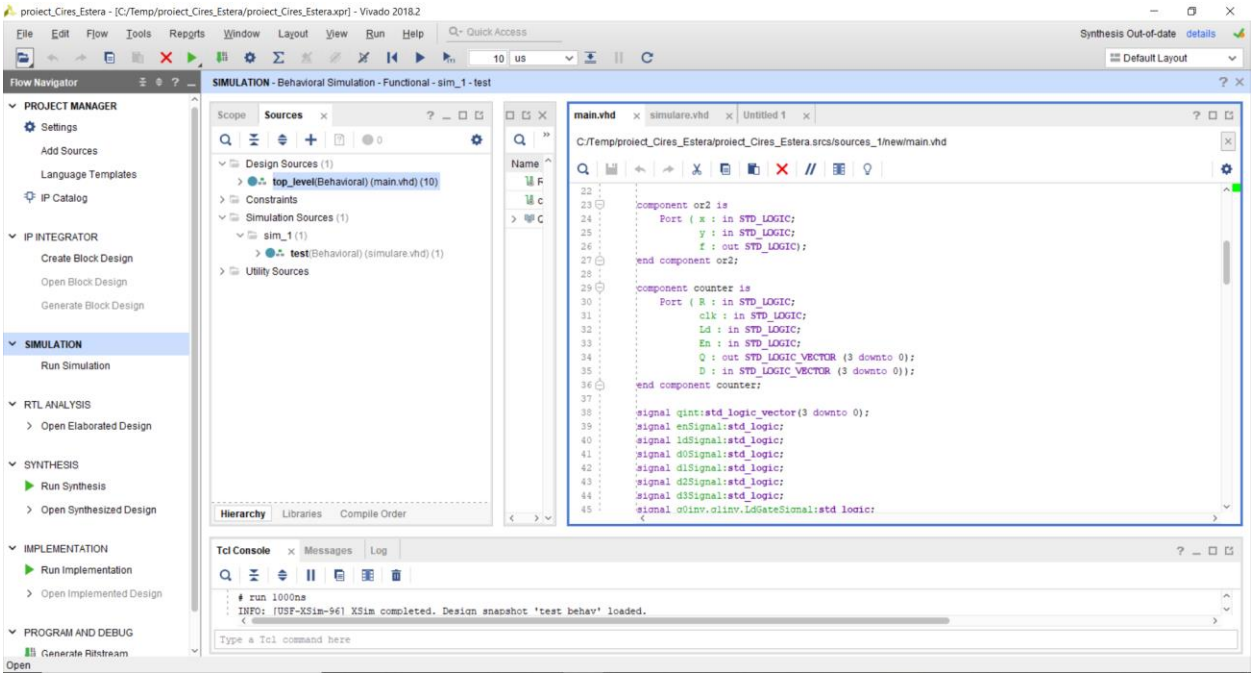
Untitled 1
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/main.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity top_level is ---surse
Port (R : in STD_LOGIC;
clk : in STD_LOGIC;
Q : out STD_LOGIC_VECTOR (3 downto 0));
end top_level;
architecture Behavioral of top_level is
component mux4 is
Port (A : in STD_LOGIC_VECTOR (1 downto 0);
I : in STD_LOGIC_VECTOR (3 downto 0);
Y : out STD_LOGIC);
end component mux4;
component inv is
Port (a : in STD_LOGIC;
f : out STD_LOGIC);
end component inv;
component or2 is
Port (x : in STD_LOGIC;
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here


proiect_Cires_Estera - [C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.xpr] - Vivado 2018.2
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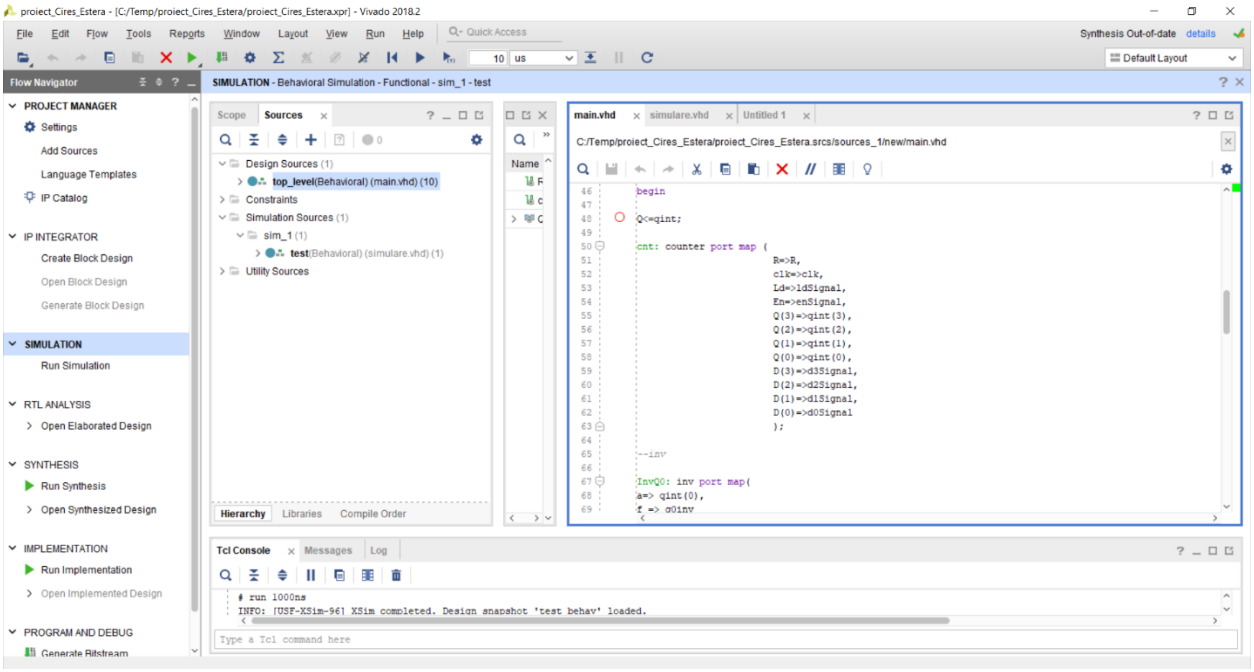
Untitled 1
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/main.vhd
component or2 is
Port (x : in STD_LOGIC;
y : in STD_LOGIC;
f : out STD_LOGIC);
end component or2;
component counter is
Port (R : in STD_LOGIC;
clk : in STD_LOGIC;
Ld : in STD_LOGIC;
En : in STD_LOGIC;
Q : out STD_LOGIC_VECTOR (3 downto 0);
D : in STD_LOGIC_VECTOR (3 downto 0));
end component counter;
signal qint:std_logic_vector(3 downto 0);
signal enSignal:std_logic;
signal ldSignal:std_logic;
signal d0Signal:std_logic;
signal d1Signal:std_logic;
signal d2Signal:std_logic;
signal d3Signal:std_logic;
signal g0inv,g1inv,LdGateSignal:std_logic;
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here
Open


proiect_Cires_Estera - [C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.xpr] - Vivado 2018.2
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Untitled 1
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/main.vhd
begin
Q<=qint;
cnt: counter port map (
R=>R,
clk=>clk,
Ld=>ldSignal,
En=>enSignal,
Q(3)=>qint(3),
Q(2)=>qint(2),
Q(1)=>qint(1),
Q(0)=>qint(0),
D(3)=>d3Signal,
D(2)=>d2Signal,
D(1)=>d1Signal,
D(0)=>d0Signal
);
--inv
InvQ0: inv port map(
a=> qint(0),
f => q0inv
Tcl Console
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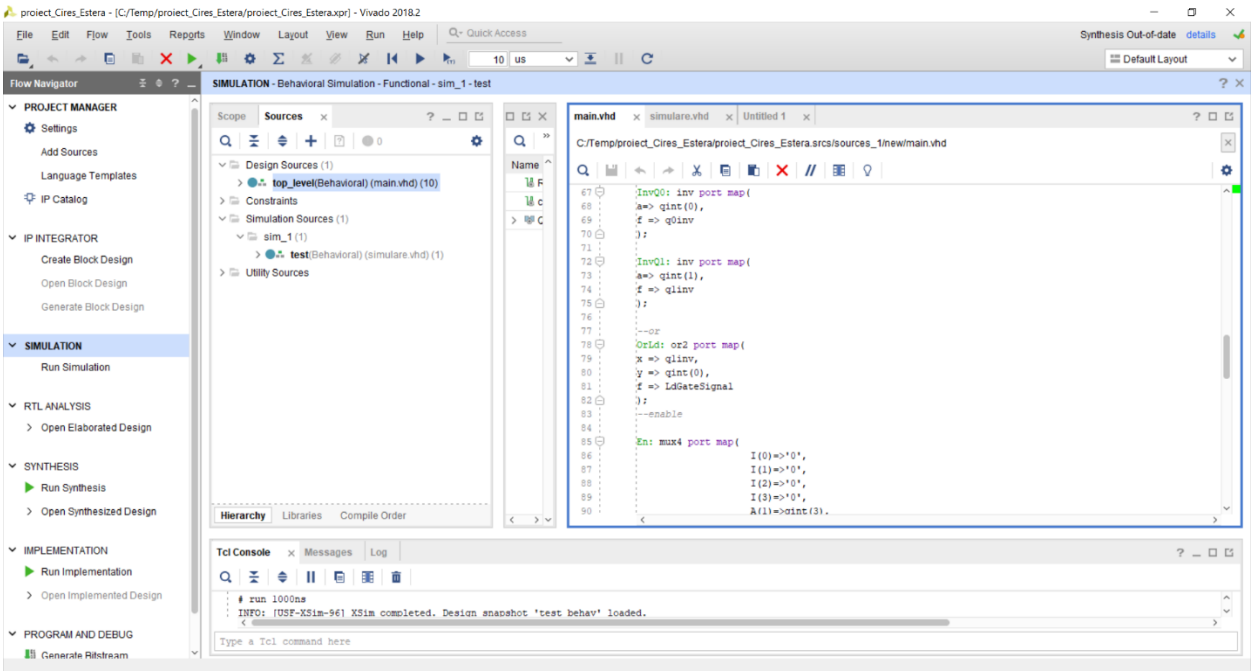
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here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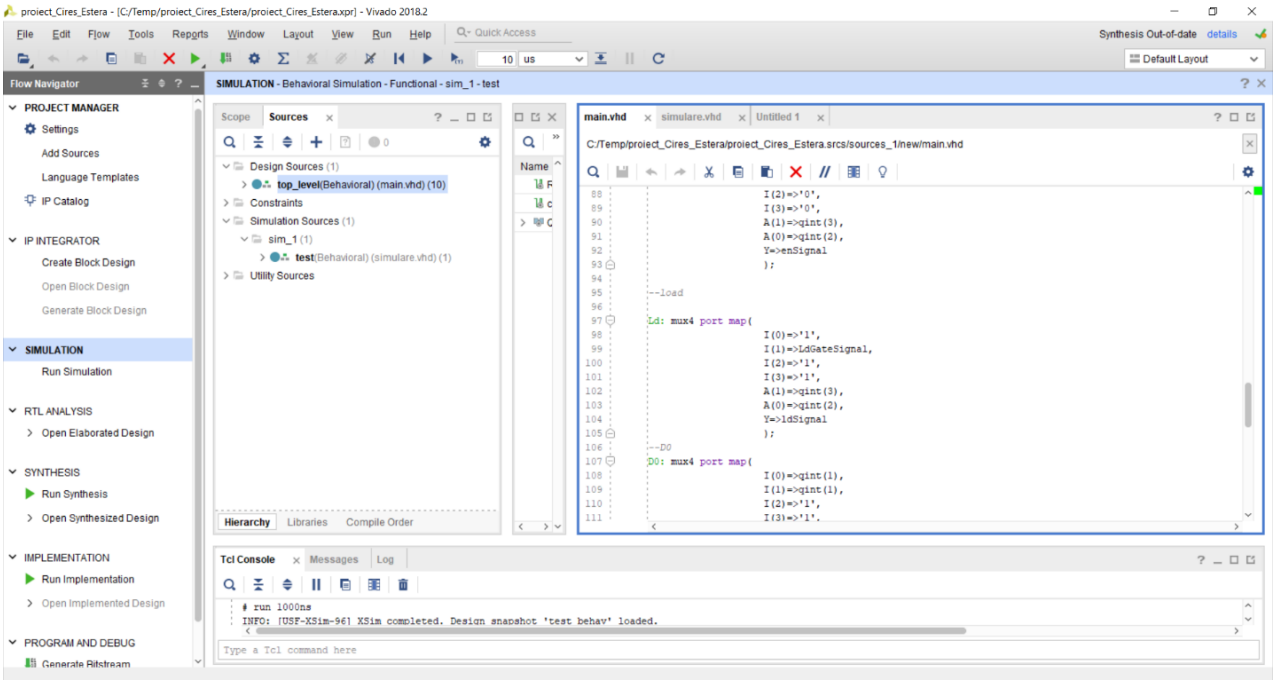
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/main.vhd
InvQ0: inv port map(
a=> qint(0),
f => q0inv
);
InvQ1: inv port map(
a=> qint(1),
f => q1inv
);
--or
OrLd: or2 port map(
x => q1inv,
y => qint(0),
f => LdGateSignal
);
--enable
En: mux4 port map(
I(0)=>'0',
I(1)=>'0',
I(2)=>'0',
I(3)=>'0',
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here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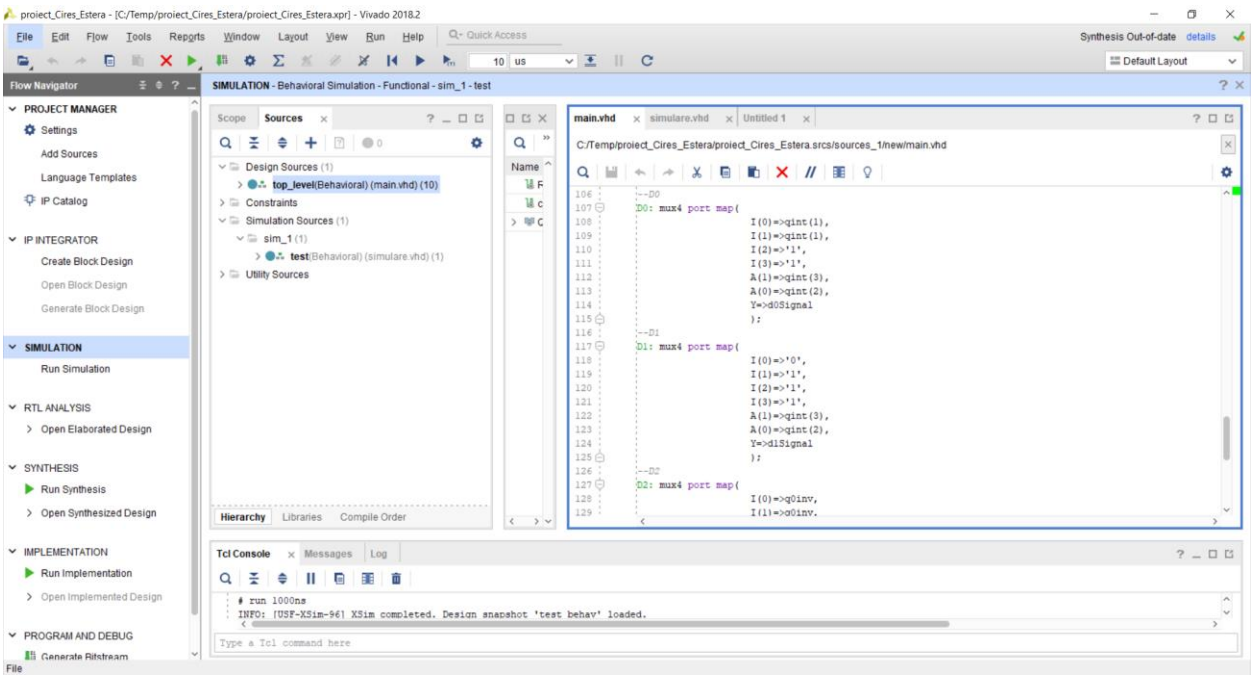
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/main.vhd
I(2)=>'0',
I(3)=>'0',
A(1)=>qint(3),
A(0)=>qint(2),
Y=>enSignal
);
--load
Ld: mux4 port map(
I(0)=>'1',
I(1)=>LdGateSignal,
I(2)=>'1',
I(3)=>'1',
A(1)=>qint(3),
A(0)=>qint(2),
Y=>ldSignal
);
--D0
D0: mux4 port map(
I(0)=>qint(1),
I(1)=>qint(1),
I(2)=>'1',
I(3)=>'1'.
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here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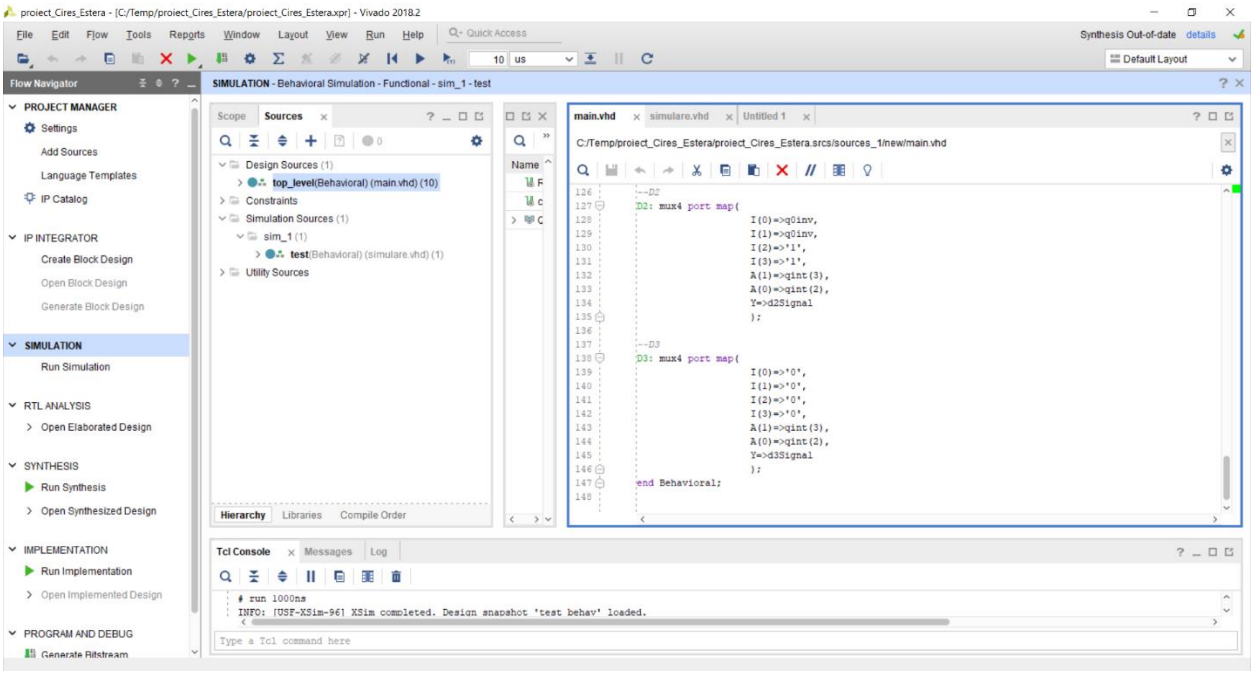
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/main.vhd
--D0
D0: mux4 port map(
I(0)=>qint(1),
I(1)=>qint(1),
I(2)=>'1',
I(3)=>'1',
A(1)=>qint(3),
A(0)=>qint(2),
Y=>d0Signal
);
--D1
D1: mux4 port map(
I(0)=>'0',
I(1)=>'1',
I(2)=>'1',
I(3)=>'1',
A(1)=>qint(3),
A(0)=>qint(2),
Y=>d1Signal
);
--D2
D2: mux4 port map(
I(0)=>q0inv,
I(1)=>q0inv.
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here
File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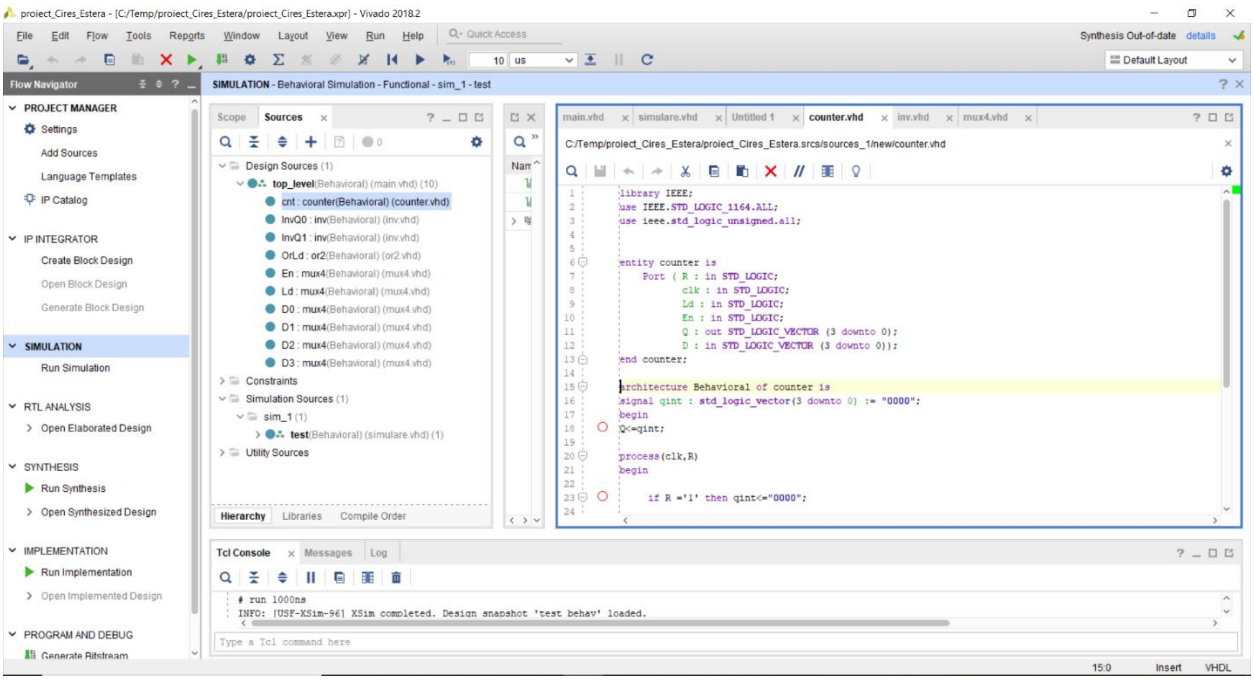
Untitled 1
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/main.vhd
--D2
D2: mux4 port map(
I(0)=>q0inv,
I(1)=>q0inv,
I(2)=>'1',
I(3)=>'1',
A(1)=>qint(3),
A(0)=>qint(2),
Y=>d2Signal
);
--D3
D3: mux4 port map(
I(0)=>'0',
I(1)=>'0',
I(2)=>'0',
I(3)=>'0',
A(1)=>qint(3),
A(0)=>qint(2),
Y=>d3Signal
);
end Behavioral;
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here


proiect_Cires_Estera - [C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.xpr] - Vivado 2018.2
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top_level(Behavioral) (main.vhd) (10)
cnt : counter(Behavioral) (counter.vhd)
InvQ0 : inv(Behavioral) (inv.vhd)
InvQ1 : inv(Behavioral) (inv.vhd)
OrLd : or2(Behavioral) (or2.vhd)
En : mux4(Behavioral) (mux4.vhd)
Ld : mux4(Behavioral) (mux4.vhd)
D0 : mux4(Behavioral) (mux4.vhd)
D1 : mux4(Behavioral) (mux4.vhd)
D2 : mux4(Behavioral) (mux4.vhd)
D3 : mux4(Behavioral) (mux4.vhd)
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sim_1 (1)
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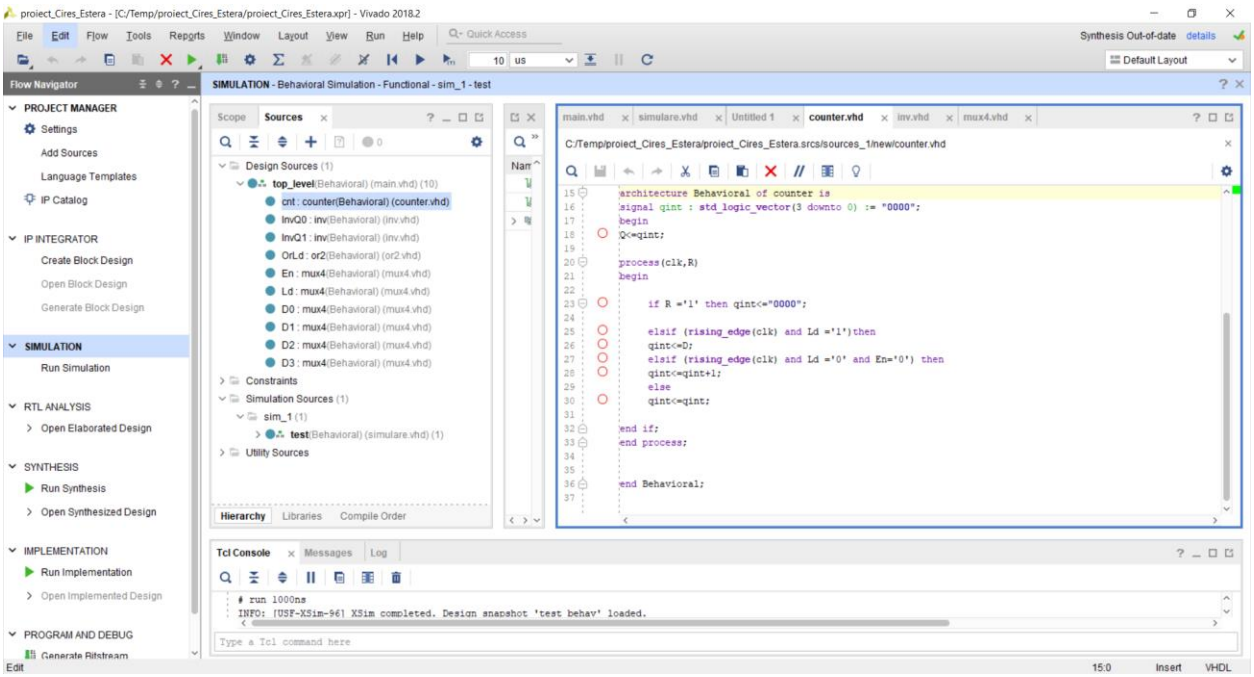
Untitled 1
counter.vhd
inv.vhd
mux4.vhd
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/counter.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.std_logic_unsigned.all;
entity counter is
Port (R : in STD_LOGIC;
clk : in STD_LOGIC;
Ld : in STD_LOGIC;
En : in STD_LOGIC;
Q : out STD_LOGIC_VECTOR (3 downto 0);
D : in STD_LOGIC_VECTOR (3 downto 0));
end counter;
architecture Behavioral of counter is
signal qint : std_logic_vector(3 downto 0) := "0000";
begin
Q<=qint;
process(clk,R)
begin
if R ='1' then qint<="0000";
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here
15:0
Insert
VHDL


proiect_Cires_Estera - [C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.xpr] - Vivado 2018.2
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cnt : counter(Behavioral) (counter.vhd)
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InvQ1 : inv(Behavioral) (inv.vhd)
OrLd : or2(Behavioral) (or2.vhd)
En : mux4(Behavioral) (mux4.vhd)
Ld : mux4(Behavioral) (mux4.vhd)
D0 : mux4(Behavioral) (mux4.vhd)
D1 : mux4(Behavioral) (mux4.vhd)
D2 : mux4(Behavioral) (mux4.vhd)
D3 : mux4(Behavioral) (mux4.vhd)
Constraints
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sim_1 (1)
test(Behavioral) (simulare.vhd) (1)
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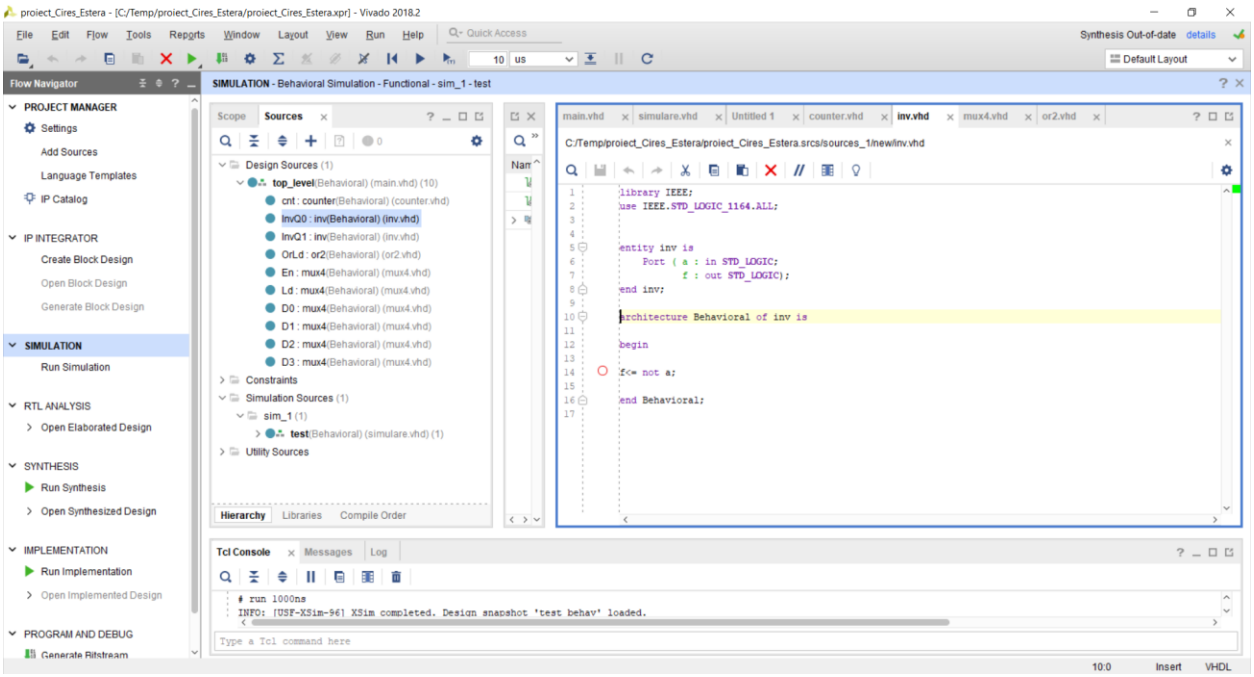
main.vhd simulare.vhd Untitled 1 counter.vhd inv.vhd mux4.vhd
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/counter.vhd
architecture Behavioral of counter is
signal qint : std_logic_vector(3 downto 0) := "0000";
begin
Q<=qint;
process(clk,R)
begin
if R ='1' then qint<="0000";
elsif (rising_edge(clk) and Ld ='1')then
qint<=D;
elsif (rising_edge(clk) and Ld ='0' and En='0') then
qint<=qint+1;
else
qint<=qint;
end if;
end process;
end Behavioral;
Tcl Console Messages Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here
Edit
15:0
Insert
VHDL


proiect_Cires_Estera - [C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.xpr] - Vivado 2018.2
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InvQ0 : inv(Behavioral) (inv.vhd)
InvQ1 : inv(Behavioral) (inv.vhd)
OrLd : or2(Behavioral) (or2.vhd)
En : mux4(Behavioral) (mux4.vhd)
Ld : mux4(Behavioral) (mux4.vhd)
D0 : mux4(Behavioral) (mux4.vhd)
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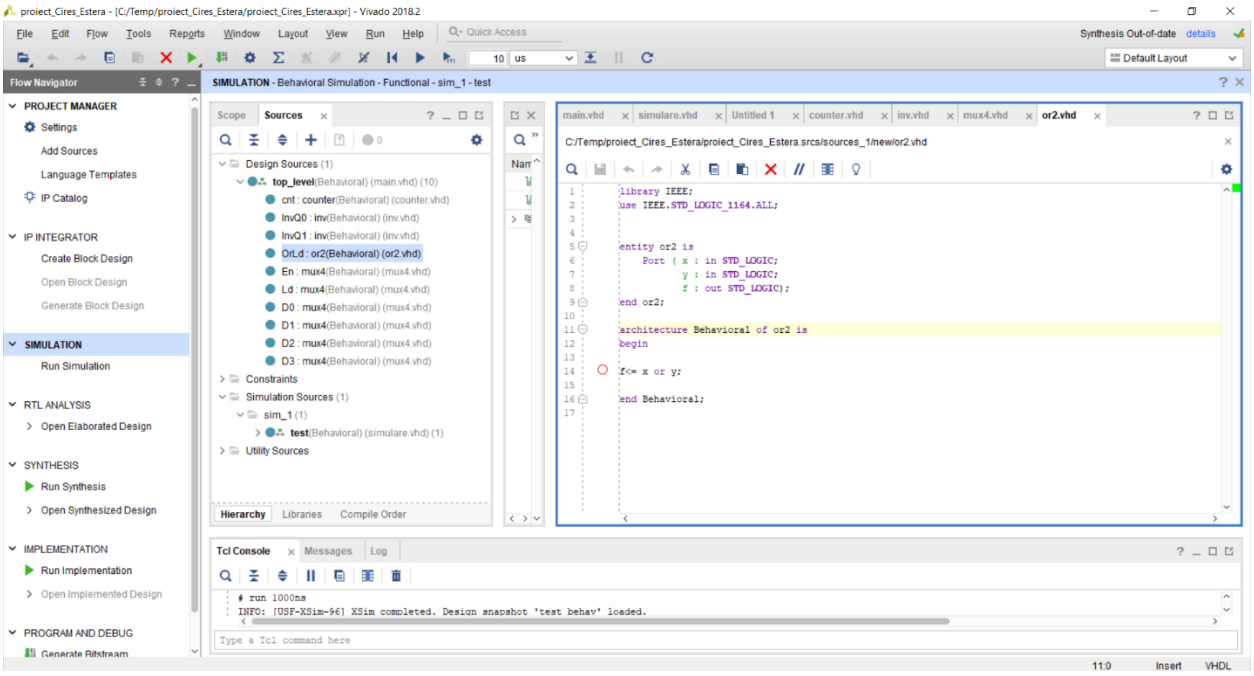
test(Behavioral) (simulare.vhd) (1)
Utility Sources
Hierarchy Libraries Compile Order
main.vhd simulare.vhd Untitled 1 counter.vhd inv.vhd mux4.vhd or2.vhd
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/inv.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity inv is
Port (a : in STD_LOGIC;
f : out STD_LOGIC);
end inv;
architecture Behavioral of inv is
begin
f<= not a;
end Behavioral;
Tcl Console Messages Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here
10:0
Insert
VHDL


proiect_Cires_Estera - [C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.xpr] - Vivado 2018.2
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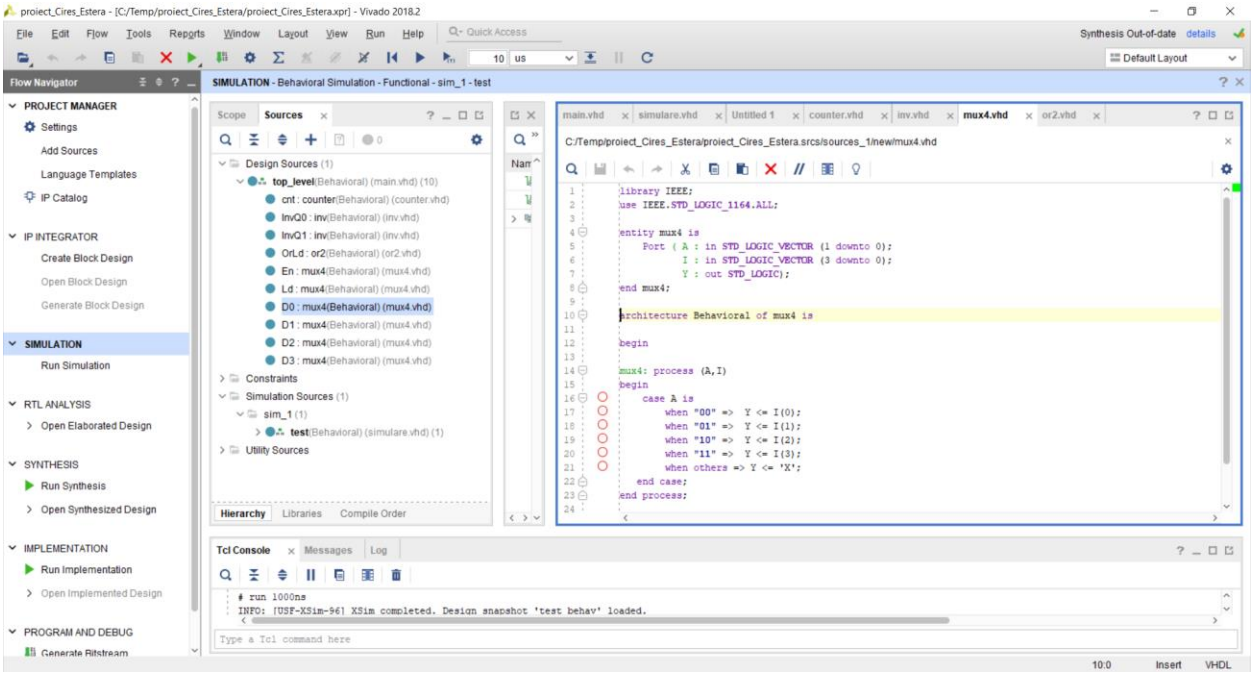
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/or2.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity or2 is
Port (x : in STD_LOGIC;
y : in STD_LOGIC;
f : out STD_LOGIC);
end or2;
architecture Behavioral of or2 is
begin
f<= x or y;
end Behavioral;
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.


proiect_Cires_Estera - [C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.xpr] - Vivado 2018.2
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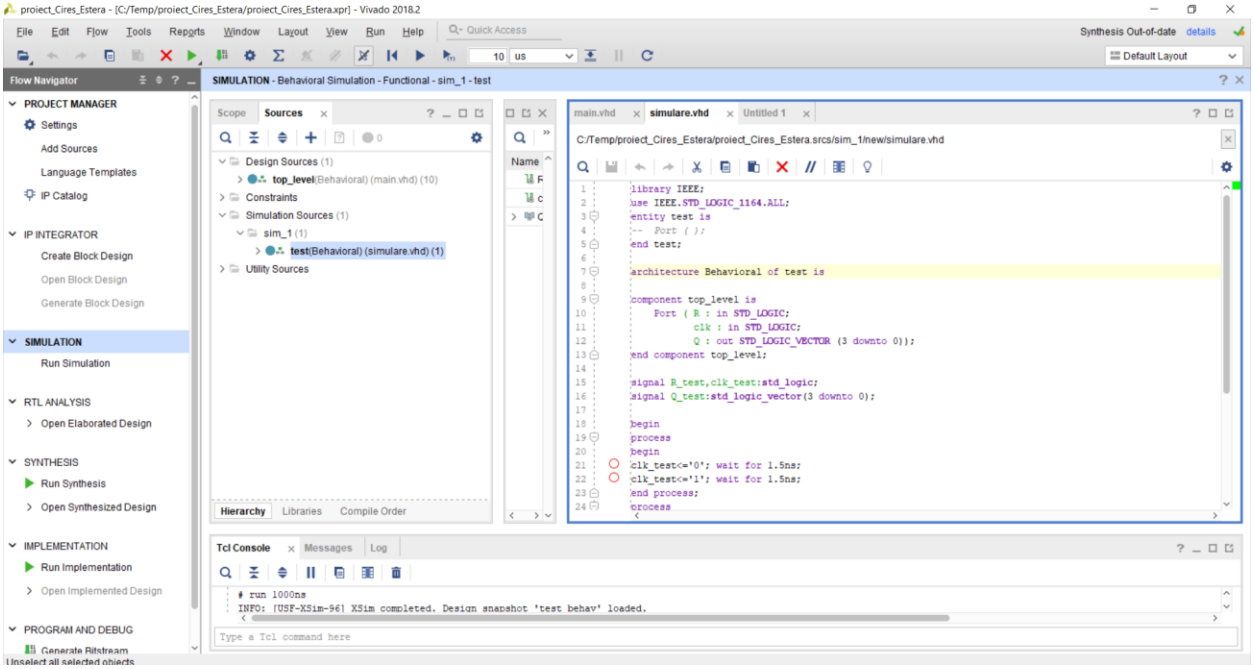
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sources_1/new/mux4.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity mux4 is
Port (A : in STD_LOGIC_VECTOR (1 downto 0);
I : in STD_LOGIC_VECTOR (3 downto 0);
Y : out STD_LOGIC);
end mux4;
architecture Behavioral of mux4 is
begin
mux4: process (A,I)
begin
case A is
when "00" => Y <= I(0);
when "01" => Y <= I(1);
when "10" => Y <= I(2);
when "11" => Y <= I(3);
when others => Y <= 'X';
end case;
end process;
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.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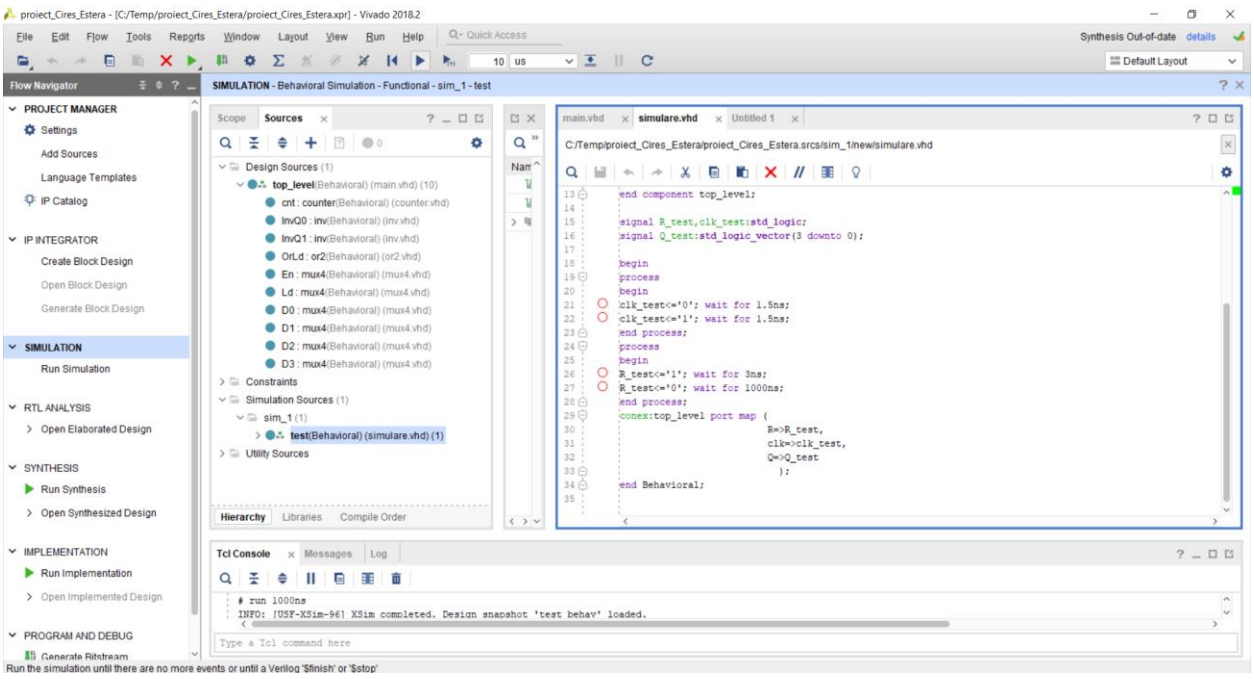
Utility Sources
Hierarchy Libraries Compile Order
main.vhd
simulare.vhd
Untitled 1
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sim_1/new/simulare.vhd
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity test is
-- Port ( );
end test;
architecture Behavioral of test is
component top_level is
Port (R : in STD_LOGIC;
clk : in STD_LOGIC;
Q : out STD_LOGIC_VECTOR (3 downto 0));
end component top_level;
signal R_test,clk_test:std_logic;
signal Q_test:std_logic_vector(3 downto 0);
begin
process
begin
clk_test<='0'; wait for 1.5ns;
clk_test<='1'; wait for 1.5ns;
end process;
process
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here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simulare.vhd
Untitled 1
C:/Temp/proiect_Cires_Estera/proiect_Cires_Estera.srcs/sim_1/new/simulare.vhd
end component top_level;
signal R_test,clk_test:std_logic;
signal Q_test:std_logic_vector(3 downto 0);
begin
process
begin
clk_test<='0'; wait for 1.5ns;
clk_test<='1'; wait for 1.5ns;
end process;
process
begin
R_test<='1'; wait for 3ns;
R_test<='0'; wait for 1000ns;
end process;
comex:top_level port map (
R=>R_test,
clk=>clk_test,
Q=>Q_test
);
end Behavioral;
Tcl Console
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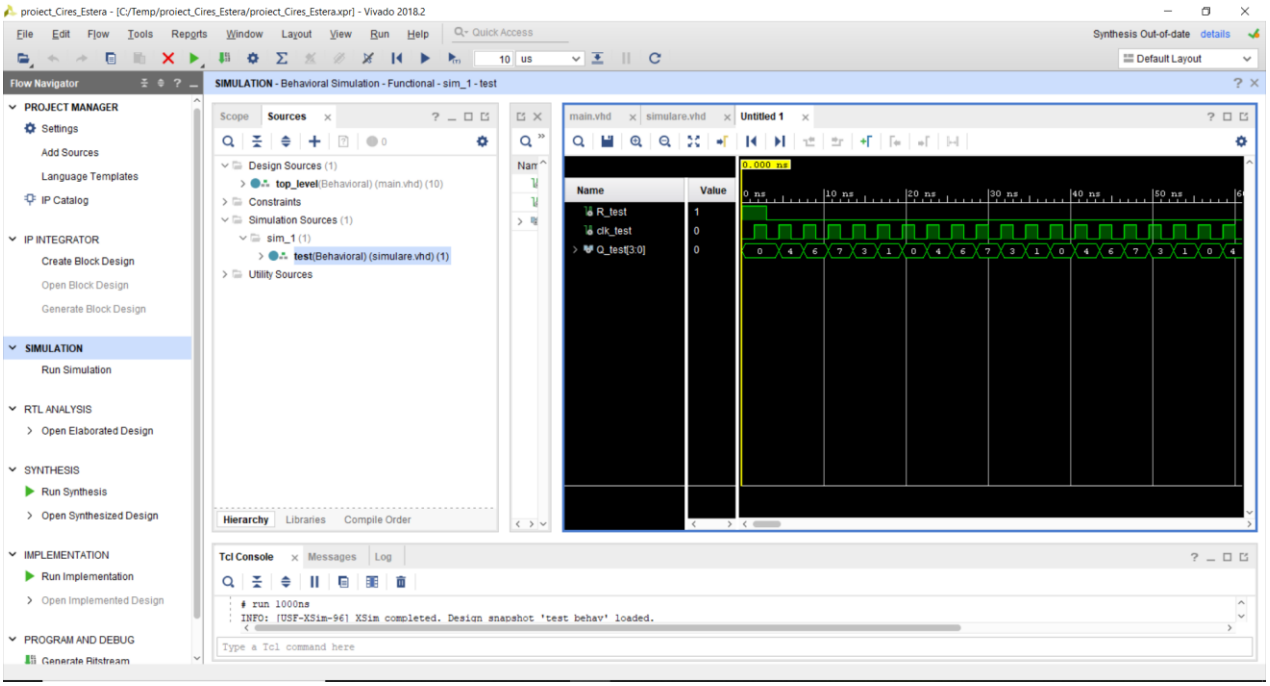
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test_behav' loaded.
Type a Tcl command here
Run the simulation until there are no more events or until a Verilog '$finish' or '$stop'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simulare.vhd
Untitled 1
Name
Value
R_test
clk_test
Q_test[3:0]
0.000 ns
Tcl Console
Messages
Log
run 1000ns
INFO: [USF-XSim-96] XSim completed. Design snapshot 'test behav' loaded.
Type a Tcl command here