# Error Minimization in Layered Manufacturing Parts by Stereolithography File Modification Using a Vertex Translation Algorithm

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*Layered manufacturing (LM) machines use stereolithography (STL) files to build parts by creating continuous slices on top of each other. An STL file approximates the surface of a part with planar triangles. This results in geometric errors being introduced in the part surface during the conversion from the CAD model to the STL file format, which in turn leads to errors in the LM manufactured part. CAD packages have built-in export options to reduce this CAD to STL conversion error. However, this is applied to the entire part geometry which leads to an increase in the file size and preprocessing time in LM machines. This paper presents a new approach to locally reduce this CAD to STL translation error. This approach, referred to as vertex translation algorithm (VTA), compares an STL facet to its corresponding CAD surface, computes the chordal error at multiple points on the STL surface, and translates the point with the maximum chordal error until it lies on the design surface. This translation results in the reduction of the chordal error locally without unnecessarily increasing the size of the STL file. In addition, a facet isolation algorithm (FIA) has also been developed and presented in this paper. This isolation algorithm extracts the STL facets corresponding to the surfaces and features of the part that have to be modified by the translation algorithm. The VTA is applied in conjunction with the FIA on a sample service part to reduce the form and profile error of critical features of the part in order to satisfy the tolerance callouts on the part.*
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## 1 Introduction

Layered manufacturing (LM) is an emerging technology for manufacturing highly complex precision parts by creating contiguous slices on top of one another. The inputs that are required for manufacturing a part by the LM process are STL file, part orientation, slicing, support structures, tool path planning and materials [1]. The stereolithography (STL) file format is the standard input for all LM machines and approximates the skin of the part using planar triangles. This approximation leads to geometric errors in the STL file when the part consists of curved surfaces. These geometric errors are propagated downstream in the manufacturing process and lead to surface inaccuracies and errors in LM parts. Although, alternate file formats and methodologies have been proposed to improve LM part accuracy [2–5], LM machines still use the standard STL file format as their input. Therefore, there is a definite need to improve the quality of the existing STL file format in order to minimize the loss of part information during CAD to STL conversion. This paper presents a new algorithm to selectively and locally modify the STL file to reduce the CAD-STL conversion errors with a view to achieving profile and form tolerances specified in the part design.

The CAD-STL translation error has been generally defined by LM researchers as a chordal error [3,4,6] which is the Euclidean distance between the STL facet and the CAD surface as shown in Fig. 1. Mathematically, the chordal error can be written as

$$\varepsilon_{ch} = \|P_{STL} - P_{CAD}\| \tag{1}$$

where $P_{STL}$ is a point on the STL facet and $P_{CAD}$ is the corresponding point on the CAD surface. In the algorithm presented in this paper, the chordal errors for multiple points on the STL facets are calculated and the point on an STL facet with the maximum chordal error is translated to coincide with the CAD surface. This algorithm, termed as vertex translation algorithm (VTA) [7,8], reduces the chordal error associated with the STL file and is applied iteratively on the STL facets until the chordal error becomes less than the specified error threshold. The VTA has been applied on a test surface and the results show that there is 91.6% reduction in the chordal error of the surface.

Actual service parts, however, have geometric dimensioning and tolerancing (GD&T) callouts on their critical features. Consequently, the STL files of the LM parts should be suitably modified such that the critical features and surfaces adhere to their respective design callouts. Therefore, in this paper, the effect of VTA in minimizing the form and profile errors in LM parts has also been investigated. When the STL file of a part is modified by the translation algorithm, each STL facet is replaced with three new triangles, thereby leading to an increase in the size of the STL file. To avoid this increase in the file size, the translation algorithm is applied only on select features and surfaces that need to be modified based on their respective tolerance callouts. In order to facilitate selective application of the VTA on only the necessary

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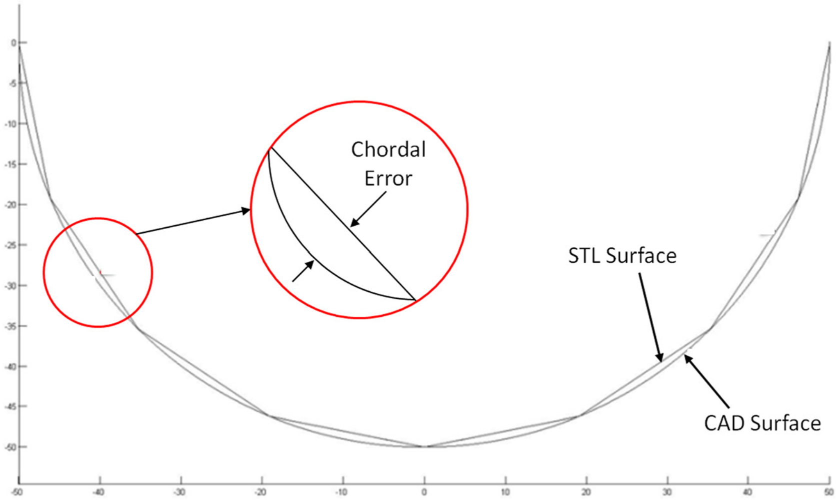


**Fig. 1 Chordal error in an STL file**

surfaces and features, a facet isolation algorithm (FIA) has been developed. This isolation algorithm extracts and separates the surfaces and features in a part with different tolerance callouts and isolates the STL facets which correspond to the extracted surfaces and features. The extracted STL facet files are then used as an input to the translation algorithm which then modifies the files individually.

For analyzing the effect of VTA in reducing the form and profile tolerances in service parts, the LM part is virtually manufactured. Points are then sampled from the simulated manufactured surface and the errors are calculated from these sampled points. If these errors on the critical features and surfaces exceed the respective tolerance callouts, their corresponding STL facets are isolated. These isolated STL facets are then modified by the VTA and this process is repeated until all the specified tolerances are satisfied. This methodology has been tested with an example service part and the results are provided. The translation algorithm was able to reduce the cylindricity form error by 73.43% and the surface profile errors by 14.36% and 48.98%, respectively.

The rest of the paper is divided into four sections. Section 2 presents a detailed technical literature review pertaining to STL file format and LM errors. Section 3 provides a thorough explanation of the VTA methodology and the results of two test cases. Section 4 explains the FIA in detail while Sec. 5 discusses the effect of VTA in reducing the form and profile errors in LM parts. Section 6 presents the conclusions based on this research and the scope for future research within this domain.

## 2 Literature Review

The STL file format is the standard input to all LM machines. However, the STL file is prone to several drawbacks, such as missing geometry, redundant information, and lack of manufacturing data [9–12]. Several researchers have studied ways to eliminate the STL file errors and this section presents some of the relevant research carried out in this area. The errors in the STL file together with the staircase effect lead to profile and form errors in LM manufactured parts. The calculations of profile and form errors have also been researched before and some of the published research has been presented here.

**2.1 STL File Format Errors and Modification.** The STL format approximates the design surface by a series of triangular facets. It lacks any topological information and can exist in both binary and ASCII formats. Although the STL file format is an accepted industry standard, it may suffer from certain shortcomings, such as gaps, missing and overlapping facets and nonmanifold topology conditions. Leong et al. [10] studied these problems and provided a geometric solution to correct the missing facets. van Niekerk and Ehlers [11] divided STL errors into structural and geometrical errors and developed a mathematical approach to check the problems in an STL file and corrected them. They considered the errors in file structure, overlapping triangles, violation of vertex to vertex rule, incorrect direction of surface normal and violation of Euler's rule. Stroud and Xirouchakis [12] presented approaches towards improving the free form fabrication process by using approximation control parameters and use of STL extensions. According to their study, STL format redundancy, incomplete description of geometry, coarse approximation method and inability to include manufacturing information were the main shortcomings of the STL file format. Fadel and Kirschman [9] explained the issues involved in tessellation and convex boundary error. Errors, such as missing lines, truncation errors, and reversal of normal direction due to incorrect order of vertices were explained. Lee et al. [13] proposed a methodology for generating an STL file from measured data points using a Delaunay triangulation approach. Lee and Kim [14] presented a methodology to obtain a deformed model from an STL model based on a user defined error criteria. They introduced a new STL data structure that involves searching and splitting the facets using Euler operators. The STL file was deformed on the basis of a certain user defined error criteria evaluated from the given constraints of the shape. To date, researchers have not looked into selectively modifying the existing STL format to minimize the CAD-STL translation errors associated with the different surfaces of the part. The current paper is an extension of the study on STL file modification by Navangul et al. [7,8] and presents a new algorithm which will seek to improve the STL file quality by locally modifying the STL facets in order to satisfy and minimize the chordal errors specified on the part.

**2.2 Form and Profile Errors in LM Parts.** Several researchers have investigated the impact of LM process parameters on the different errors on the manufactured part. Paul and Anand [15] analyzed the effect between part orientation and cylindricity error in single and multiple cylindrical features using mathematical and geometric analyses. Ollison and Berisso [16] performed a statistical study on cylindrical parts manufactured by the 3D printing process and correlated part orientation, part diameter and printhead life to the cylindricity error. Lynn-Charney and Rosen [17] used response surface methodology (RSM) and compromise decision support problem (CDSP) techniques to calculate the optimal LM process parameters for reducing six types of tolerances: positional, flatness, parallelism, perpendicularity, concentricity, and circularity. Arni and Gupta [18] studied the flatness errors in planar features on LM manufactured parts and calculated feasible orientations for satisfying the flatness tolerances using Gaussian spheres. Masood et al. [19,20] studied the volumetric error of LM manufactured parts and correlated the volumetric error to the part build orientation. Chang and Huang [21] analyzed the profile error induced in fused deposition modeling (FDM) parts and correlated the error to the extruding aperture. Singh and Dutta [22] presented a novel method of multidimensional slicing algorithm which leads to reduction in supports and also can be used to generate freeform slices. Kulkarni and Dutta [23] developed a CAD slicing algorithm using curvature information to reduce the cusp height of LM parts. Koc [24] studied the profile error in free form surfaces in LM and developed a marching point algorithm to calculate the error. They also presented an adaptive slicing algorithm to minimize this profile error. Tsopanos et al. [25] studied the effect of process parameters in the selective laser sintering (SLS) process on density and strength of the manufactured part. Although, several researchers have studied the profile and form errors induced in LM parts, the correlation of the STL file quality and the modification of STL file with the profile and form errors on an LM part have not been researched before. This paper analyzes the effect of the VTA based STL file modification on minimizing form and profile errors of LM parts.

## 3 Vertex Translation Algorithm

The conversion of the CAD model to an STL file leads to surface errors due to the approximation of nonplanar surfaces by planar triangles [3,4,6]. This approximation, defined as chordal error, leads to the development of form, profile and volumetric errors in LM parts built from the STL file. This section introduces a new vertex translation algorithm (VTA) for reducing the chordal error of an STL file.

**3.1 VTA Methodology.** For developing the VTA, the surface is first modeled using any standard CAD package (in this case NX 7.5 from Siemens PLM [26]) and then exported into two file formats, initial graphics exchange specification (IGES) and STL. IGES is a neutral file format that is widely used in the industry and can be used for extracting information about part surfaces stored within the native CAD file. In the IGES file, all surfaces whether they are planar or curved are stored as a NURBS surface. A NURBS surface can be written mathematically as [27]

$$S(u,v) = \frac{\sum_{i=0}^{m}\sum_{j=0}^{n} N_{i,p}(u)N_{j,q}(v)\omega_{i,j}CP_{i,j}}{\sum_{i=0}^{m}\sum_{j=0}^{n} N_{i,p}(u)N_{j,q}(v)\omega_{i,j}} \tag{2}$$

where $(u, v)$ are the parameters of the NURBS surface, $(m, n)$ is the order of the NURBS surface, $N_{i,p}$ and $N_{j,q}$ are the basis functions, $CP_{i,j}$ are the control points, and $\omega_{i,j}$ are the weights. This NURBS surface is considered as the design surface in this paper and the STL file is compared with this NURBS surface for calculating the chordal error. The chordal error is calculated for an STL file and if the error is more than a certain user specified threshold, the VTA is applied on the STL file. The algorithm is applied iteratively on the STL surface until the chordal error threshold is satisfied. The algorithm is explained in detail in the following sections.

*3.1.1 Overall Methodology.* The first step in the algorithm is to calculate the chordal errors at multiple points within an STL facet and then compute the maximum chordal error within the STL facet. The calculation of chordal errors at multiple points can be carried out as follows:

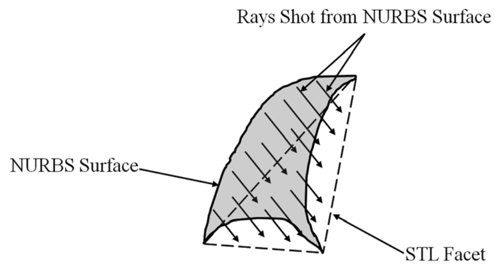


**Fig. 2 Rays shot from NURBS surface to STL facet**

(1) Divide the STL triangle into multiple points, $P_{STL}$.
(2) From each point on the STL facet, shoot rays along the direction of the normal of the facet.
(3) Find the point of intersection of these rays with the NURBS design surface. This provides the points on the design surface, $P_{CAD}$ in 3D Euclidean space.
(4) Calculate the Euclidean distance between $P_{STL}$ and $P_{CAD}$ from Eq. (1) which provides the chordal error at the points $P_{STL}$ on the STL facet.

However, the calculation of the point of intersection between a line and an NURBS surface, as required in step 3 above, is not straightforward. Therefore, in this paper, an alternate method has been adopted in which instead of shooting rays from the STL facet to the NURBS surface, the rays are shot from multiple points on the NURBS patch towards their corresponding points on the STL surface. The overall steps involved in this alternate method are

(1) Find the NURBS patch corresponding to an STL facet; this step is explained in detail in the next section.
(2) Divide this NURBS patch into multiple points, $P_{CAD}$.
(3) Shoot rays from these points towards the STL facet parallel to the direction of the normal of the STL surface as shown in Fig. 2.
(4) Calculate the points of intersection of the rays with the STL facet, $P_{STL}$.
(5) Calculate the chordal error at the point $P_{STL}$ from Eq. (1).

*3.1.2 Calculating the Corresponding NURBS Patch.* For calculating the NURBS patch corresponding to an STL facet, the $u, v$ values of the three STL vertices are first calculated. In an STL file, the three vertices of the triangular facets always lie on the design NURBS surface [12], as shown in Fig. 3.

The Euclidean distance between any triangle vertex and its corresponding NURBS design point is ideally zero. Thus the problem of finding the $u, v$ values for the triangular facet vertices that lie on the NURBS surface can be formulated as an unconstrained nonlinear optimization as shown below

$$\begin{aligned} \text{Min } f(u_i, v_i) &= \|S(u_i, v_i) - P_i(x_i, y_i, z_i)\| \\ 0 &\le u_i \le 1 \\ 0 &\le v_i \le 1 \end{aligned} \tag{3}$$

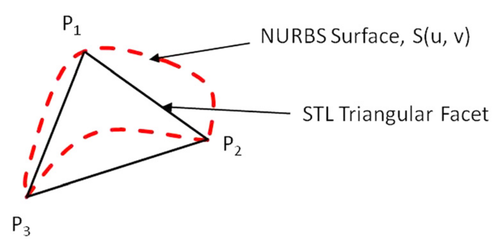


**Fig. 3 STL vertices and CAD surface**

Table 1 Lookup table for coarse optimization

| $x$ | $y$ | $z$ | $u$ | $v$ |
|---|---|---|---|---|
| 50.33 | 10.23 | 41.41 | 0.2 | 0.4 |
| 65.00 | 6.56 | 40.24 | 0.6 | 0.2 |
| 45.78 | 3.00 | 21.63 | 0.8 | 0.6 |
| — | — | — | — | — |
| — | — | — | — | — |

where $P_i(x_i, y_i, z_i)$ $i = 1, 2, 3$, are the vertices of the triangle facet and $S_i(u_i, v_i)$ are the NURBS design points for the vertices. The optimization model in Eq. (3) is a nonlinear optimization and the final optimal solution depends upon the initial starting point for the optimization. Also, the time required for solving the optimization is effected by how close the initial guess is to the final optimal solution. Therefore, for ensuring a correct and fast solution, a coarse optimization is first performed to bring the initial starting point within the neighborhood of the probable optimal solution. In the coarse optimization step, the starting solution for the optimization model in Eq. (3) is calculated by using a lookup table. The lookup table is generated by discretizing the $u, v$ space of the CAD surface into finite number of values to form a grid and calculating the $x, y, z$ Cartesian coordinates for each of these $u, v$ values using Eq. (2). A sample lookup table is shown in Table 1. After the lookup table has been generated, the $x, y, z$ coordinates in the lookup table closest to each STL vertex are chosen and the corresponding $u, v$ values in the lookup table are selected as the starting solution for the fine optimization step. This optimization provides the final $u, v$ parameter values for the three vertices of each STL facet and these $u, v$ values describe the boundary of the NURBS surface patch corresponding to each STL facet.

*3.1.3 Calculating Maximum Chordal Error in an STL Facet.* Once the NURBS patch corresponding to the STL facet has been calculated, chordal errors at multiple points on the STL facet are calculated. The chordal errors are calculated by shooting rays from discrete points on the NURBS surface patch corresponding to an STL facet, as shown in Fig. 2. The discretization of the NURBS surface patch is performed using the following steps:

(1) Calculate the NURBS $u, v$ parameters of the three vertices using the methodology described in Sec. 3.1.2. These $u, v$ values form an analogous triangle in the $u, v$ parameter space as shown in Fig. 4(*a*) with vertices $S_1(u_1, v_1)$, $S_2(u_2, v_2)$, and $S_3(u_3, v_3)$.

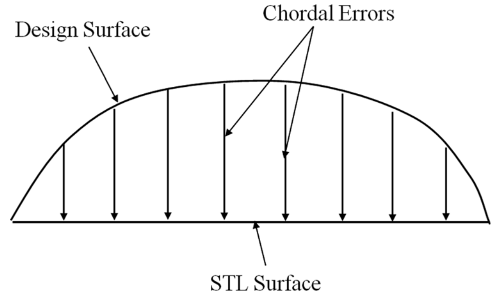


Fig. 5 Chordal errors at different points in an STL facet

(2) Divide any two edges of the triangle into an equal number of points using the following formulas:

$$S_{12}(t) = S_1 + t.(S_2 - S_1)$$
$$S_{23}(t) = S_2 + t.(S_3 - S_2)$$

where $t$ is varied between 0 and 1, i.e., $t = (0, 1)$. The values of the parameter $t$ determine the number of points into which the edges will be divided and can be varied by the user according to his/her preferences.

(3) Connect the corresponding points on both the edges, $S_{12}$ and $S_{23}$, and join these points to form connecting lines, $L$. These lines, $L$ are then further divided into points to obtain the point set $R$ in the $u, v$ parameter space using the formula

$$R(s, t) = S_{12}(t) + s.(S_{23}(t) - S_{12}(t))$$

where $s$ is varied between 0 and 1, i.e., $s = (0, 1)$. The value of the parameter $s$ depends on the length of the line $L$ and is varied such that the distance between any two points in the point set $R$ remains constant.

(4) Calculate the points, $P_{\text{CAD}}$, on the NURBS patch in the Cartesian space corresponding to the discretized points $R$ in the $u, v$ space. The mapping of the points $R$ in the $u, v$ space to points $P_{\text{CAD}}$ in the Cartesian space is shown in Fig. 4(*b*).

Rays are then traced from these discretized NURBS points $P_{\text{CAD}}$ parallel to the direction of the normal of the STL triangle until they intersect the STL facet. The points of intersection are denoted as $P_{\text{STL}}$ and their Euclidean distances from the corresponding design points $P_{\text{CAD}}$ provide the chordal error for the multiple points on the STL facet, as shown in Fig. 5. However,

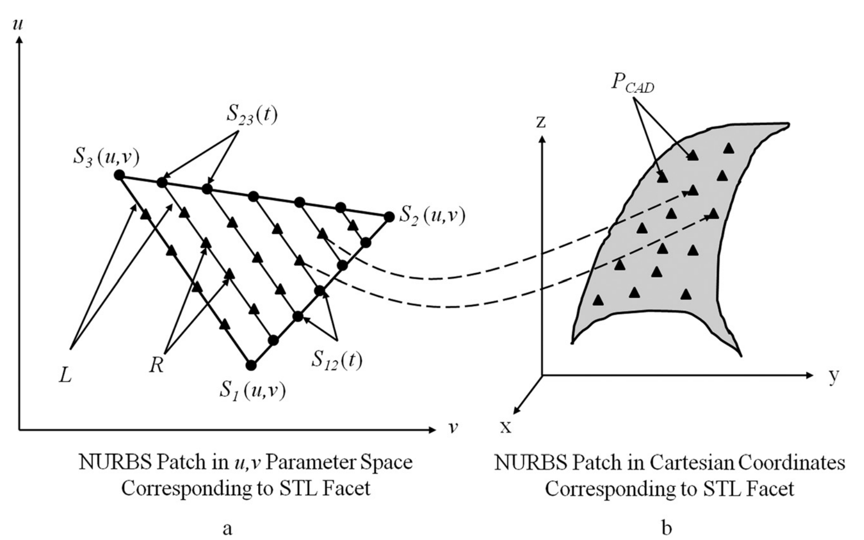


Fig. 4 (*a*) Division of the $u, v$ triangle and (*b*) mapping to Cartesian coordinates

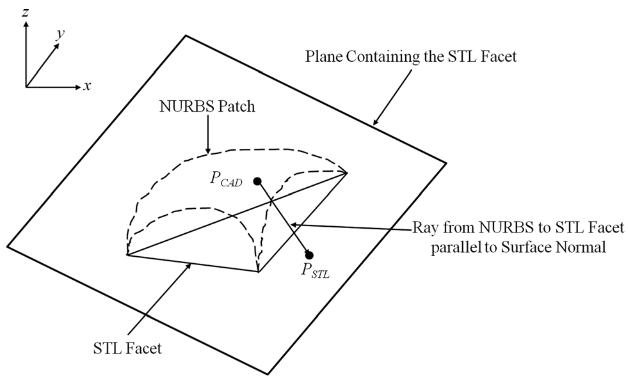


**Fig. 6 Point of intersection outside the STL facet**

there may be cases when the rays from the NURBS surface intersect the plane containing the STL facet outside the boundary of the STL triangle, as shown in Fig. 6. These cases are eliminated by using a simple point in a polygon test [28].

After the chordal errors for different points in an STL triangle are calculated, the maximum chordal error $(\varepsilon_{\mathrm{ch\_max}})$ is chosen for the facet and the point on the STL facet with the maximum chordal error, $P_{\mathrm{STL\_max}}$ is found. The Cartesian point on the NURBS surface corresponding to the maximum chordal error $(P_{\mathrm{CAD\_max}})$ is also calculated.

*3.1.4 Dividing the STL Facet.* The average chordal error $(\varepsilon_{\mathrm{ch\_avg}})$ for the STL file is then calculated. The average chordal error is defined as the mean of the chordal errors of all discrete points on all triangular facets within the STL file. Mathematically, the average chordal error can be written as

$$\varepsilon_{\mathrm{ch\_avg}} = \frac{\sum_{i=1}^{n_t} \sum_{j=1}^{n_i} (\varepsilon_{\mathrm{ch}})_{ij}}{\sum_{i=1}^{n_t} n_i} \tag{4}$$

where, $(\varepsilon_{\mathrm{ch}})_{ij}$ is the chordal error for the $j$th point on the $i$th triangular facet, $n_i$ is the number of points in the $i$th triangular facet, and $n_t$ is the total number of triangular facets in the STL file corresponding to the NURBS surface or feature. If this average error is less than the user specified threshold chordal error specified for the surface $(\varepsilon_{\mathrm{ch\_sp}})$, then the STL file is not modified. Otherwise, for each facet in the STL file, the point within the facet which has the maximum chordal error, $P_{\mathrm{STL\_max}}$, is translated parallel to direction of the normal of the facet until it coincides with its corresponding design point, $P_{\mathrm{CAD\_max}}$, on the NURBS surface. Thus the point $P_{\mathrm{CAD\_max}}$ forms the common vertex for three new STL triangles which are generated due to this translation, as shown in Fig. 7. The original facet is deleted after the translation which results in a bottomless tetrahedral structure, i.e., the original facet $P_1P_2P_3$ is replaced with three new triangles, $P_1P_{\mathrm{CAD\_max}}P_2$, $P_2P_{\mathrm{CAD\_max}}P_3$, and $P_3P_{\mathrm{CAD\_max}}P_1$. This translation results in the reduction in the maximum chordal error for the three new triangular facets as compared to the original triangle, as shown in Fig. 8. The original vertices and edges of the existing triangles are not removed which ensures that the connectivity of the new triangles with the neighboring triangles is not affected.

A special case may arise when the point with the maximum chordal error occurs on the edges of the STL facets. If such an edge point is translated to the CAD surface, the original edge of the triangle will be broken. This may create connectivity problems if this triangle facet is shared by two neighboring surfaces of the part. Since in this research, the edge connectivity between original and modified facets is kept unchanged, such edge points are discarded. Effectively, this means that any point in the set $P_{\mathrm{STL}}$ lying on the STL triangle edges is not used in the chordal error calculations (as shown in Fig. 9) and only those points which lie within the boundary of the triangular facet are considered. This is a limitation of the current algorithm but does not seem to have any significant impact on the final results, as presented in later sections.

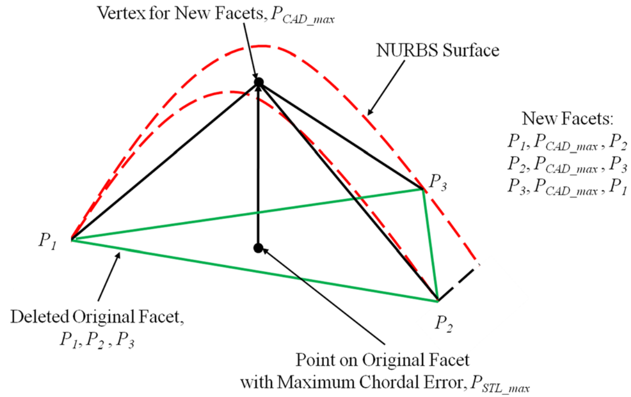


**Fig. 7 Vertex translation to create new facets**

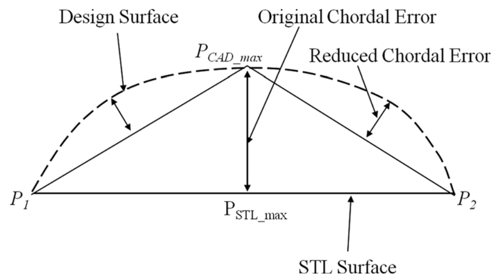


**Fig. 8 Reduction of chordal error due to VTA**

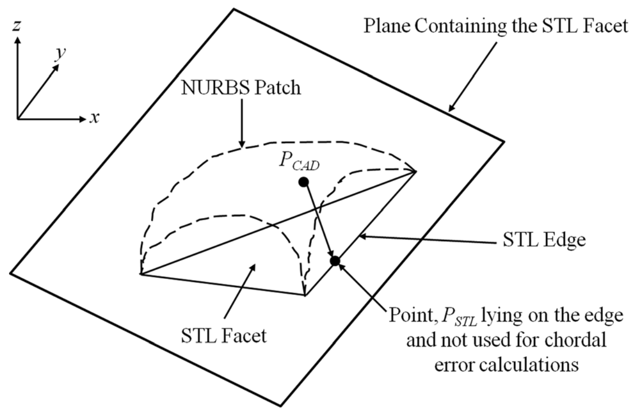


**Fig. 9 Point with maximum chordal error lying on the edge of the STL triangle**

Once the facets are modified by the VTA, they are combined to form a new modified STL file. The algorithm is applied iteratively until the average chordal error for the surface is less than the threshold chordal error. The next section presents two cases where the VTA was successfully applied to minimize the chordal error of two test surfaces.

**3.2 VTA Test Cases.** The VTA is applied on two sample surfaces, test surface 1 and test surface 2, as shown in Figs. 10 and 11. Test surface 1 is a semicircular surface and test surface 2 is a freeform surface with curvature in two directions. Both the surfaces are modeled in NX 7.5 (a Siemens PLM CAD software [26]) and exported to STL and IGES formats. The CAD to STL

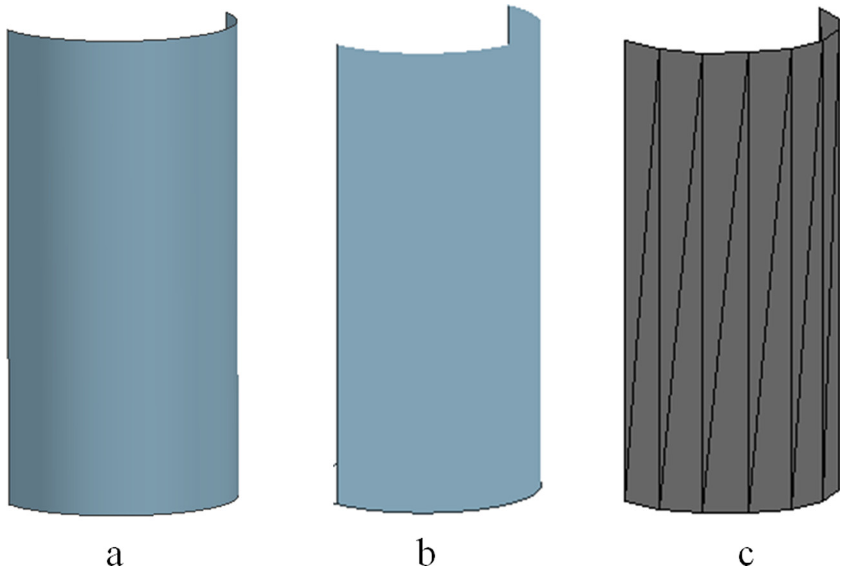


**Fig. 10 (*a*) Test surface 1 in NX, (*b*) test surface 1 in IGES, and (*c*) STL file for test surface 1**

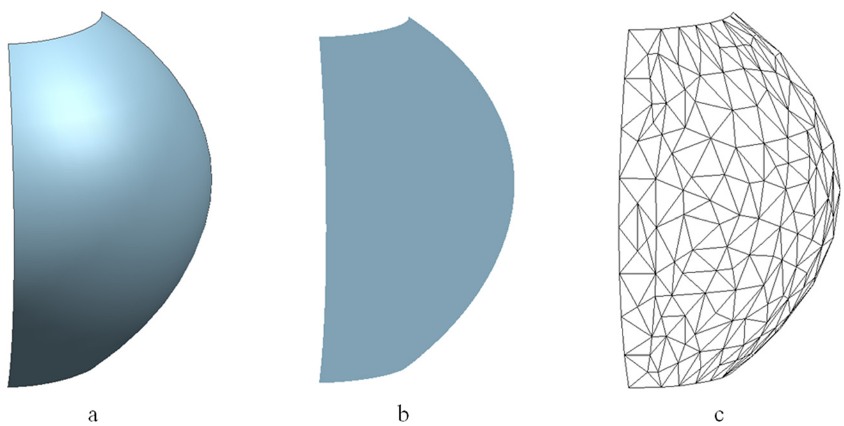


**Fig. 11 (*a*) Test surface 2 in NX, (*b*) test surface 2 in IGES, and (*c*) STL file for test surface 2**

export conversion factor is set to 0.8 mm, while the chordal error threshold is set to 0.1 mm for the test surface 1 and 0.002 mm for test surface 2. The VTA is applied iteratively on the exported STL surfaces until the average chordal error for each surface is less than the threshold error. Figure 12 shows the additional facets added to the original STL facets of test surface 1 after the first iteration, while Fig. 13 shows the evolution of the modified STL surface after each iteration. The reduction in the average chordal error for test surface 1 per iteration is shown in Fig. 14(*a*) and the percent error reduction for each iteration is shown in Fig. 14(*b*). Similar to test surface 1, the VTA is applied iteratively on test surface 2 and the results are shown in Figs. 15 and 16. Tables 2 and 3 show the summary of the results of applying the VTA on the test surfaces. As seen from these tables, the number of facets increases from 16 facets to 1296 facets for test surface 1 and from 213 to 18 747 for test surface 2. Thus, the decrease in the chordal error is offset by an increase in the number of facets, which will increase the file size and may increase the computational time. However, in the manufacturing of precision parts, error minimization and tolerance satisfaction is considered more important than computational and build time costs and therefore, the increase in file size can be justified. In addition, all slicing calculations are typically performed offline prior to the manufacture of the part and do not affect the real-time build of the part.

The above examples demonstrate that the VTA is able to reduce the average chordal error associated with an STL file by modifying the STL facets. The VTA is effective on not only ruled surfaces but also on freeform surfaces with curvature in both directions. The VTA can be applied selectively on different surfaces of a part with different error thresholds in order to locally minimize the average chordal errors associated with the surfaces. The following section presents a methodology to isolate STL facets corresponding to different surfaces and describes how the VTA can be applied on these isolated facets to modify them.

## 4 Facet Isolation Algorithm

The traditional approach for minimizing CAD-STL translation errors is to opt for a lower approximation factor in the native CAD modeling system while exporting the part models to the STL file format. However, this method of refining the STL file is applied globally to the entire part independent of the tolerance requirements on the individual part features and surfaces. Therefore, in cases where a part has one or more features or surfaces with very high tolerances, the CAD-STL translation error has to be very small in order to satisfy the tolerances in all the part features. This in turn increases the size of the STL file considerably. A better way of satisfying the part tolerances without

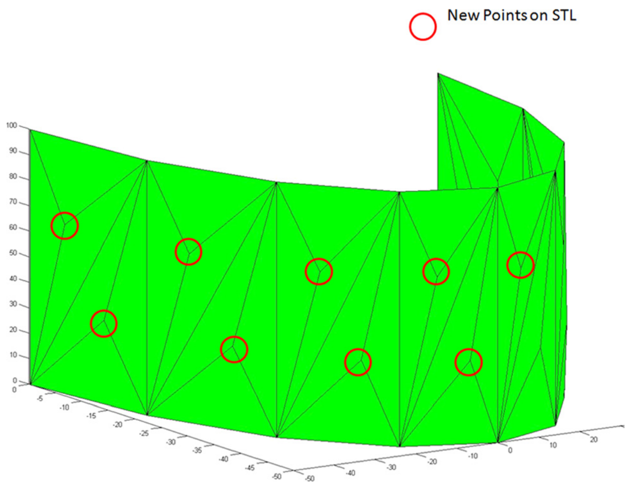


Fig. 12 First VTA iteration for test surface 1

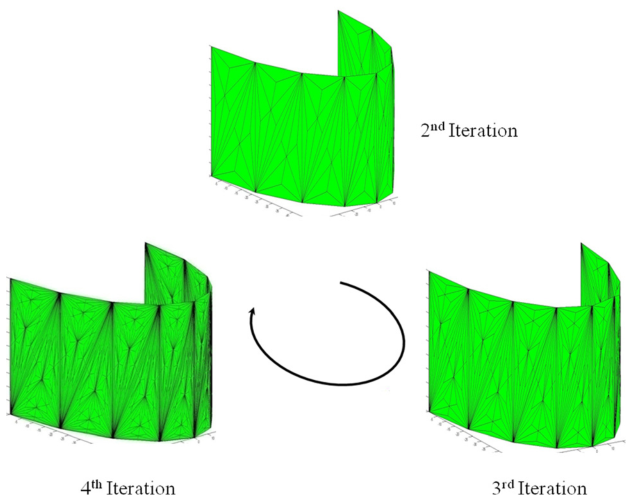


Fig. 13 Multiple VTA iterations for test surface 1

unnecessarily increasing the STL file size would be to selectively apply VTA to reduce the CAD-STL translation error only for those features or surfaces which have tighter tolerances. In order to apply the VTA only on the required surfaces and features, the STL facets representing these surfaces and features have to be first isolated. For this purpose, a FIA has been developed. This algorithm is explained in detail in the following paragraphs.

The first step in the FIA is to identify the NURBS equation of the design surface or feature for which the STL facets have to be found. Next, from the NURBS equation, the axis-aligned bounding box is calculated and the STL facets which lie within this bounding box are extracted. The final step is to identify and eliminate any extraneous facets that do not correspond to the NURBS equation of the surface. The remaining facets are the ones which correspond to the particular design surface. The schematic of the methodology for the FIA is shown in Fig. 17.

**4.1 FIA Methodology.** The different steps in the FIA are explained in detail with the help of a simple test case, test part 1, as shown in Fig. 18. The objective is to isolate the STL facets pertaining to the curved surface highlighted in Fig. 18. To start with, the CAD model is converted to the IGES format and the NURBS surface corresponding to the highlighted surface is filtered from the IGES file. Next, from the NURBS equation of the surface, the points on the surface with the minimum and maximum $x$, $y$, and $z$ coordinates are calculated by varying the NURBS parametric values $(u, v)$ between 0 and 1. These minimum and maximum values are used to calculate the bounding box of the surface as shown in Fig. 19(*a*). The bounding box is then superimposed on the STL file as shown in Fig. 19(*b*) in order to select the facets of the STL file that lie within the bounding box and may correspond to the design surface. If all the three vertices of a triangular facet lie inside the bounding box, the facet is selected. Otherwise if this condition is not satisfied, the facet is rejected since it does not correspond to the design surface. All such facets in the STL file that satisfy this condition are collected together and an intermediate STL file is generated.

This intermediate STL file contains all the facets corresponding to the selected surface in the IGES file. However, it may also consist of additional facets which do not correspond to the design surface being considered, as shown in Fig. 20(*a*). In this figure, the darker color facets are required and the lighter color facets are extra facets belonging to other surfaces which have to be removed from the intermediate STL file. As per the definition of an STL file, if a facet approximates a surface, all three vertices of the facet will lie on the NURBS surface and will satisfy the NURBS equation of the surface [12]. This property is used to remove the extraneous facets from the intermediate STL file. The process for checking whether the Cartesian coordinates of a vertex satisfy the NURBS surface equation has been formulated as a constrained nonlinear optimization problem, as described in Eq. (3). If the minimum value of the objective function in Eq. (3) is less than a specified error value, which in this case is taken as 0.0001 mm,

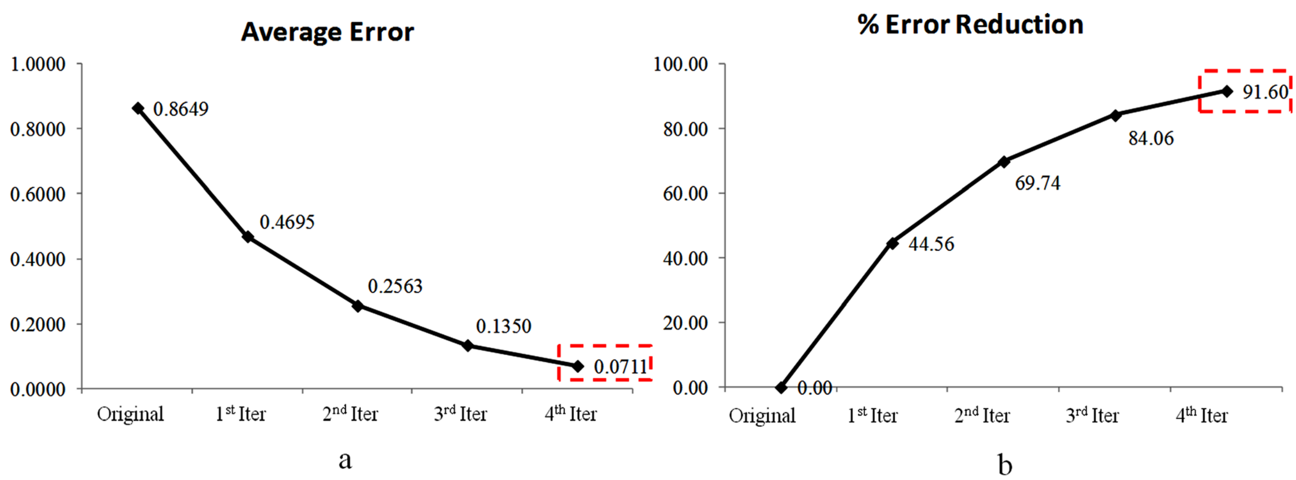


Fig. 14 (*a*) Average error versus iteration, and (*b*) % error reduction versus iteration for test surface 1

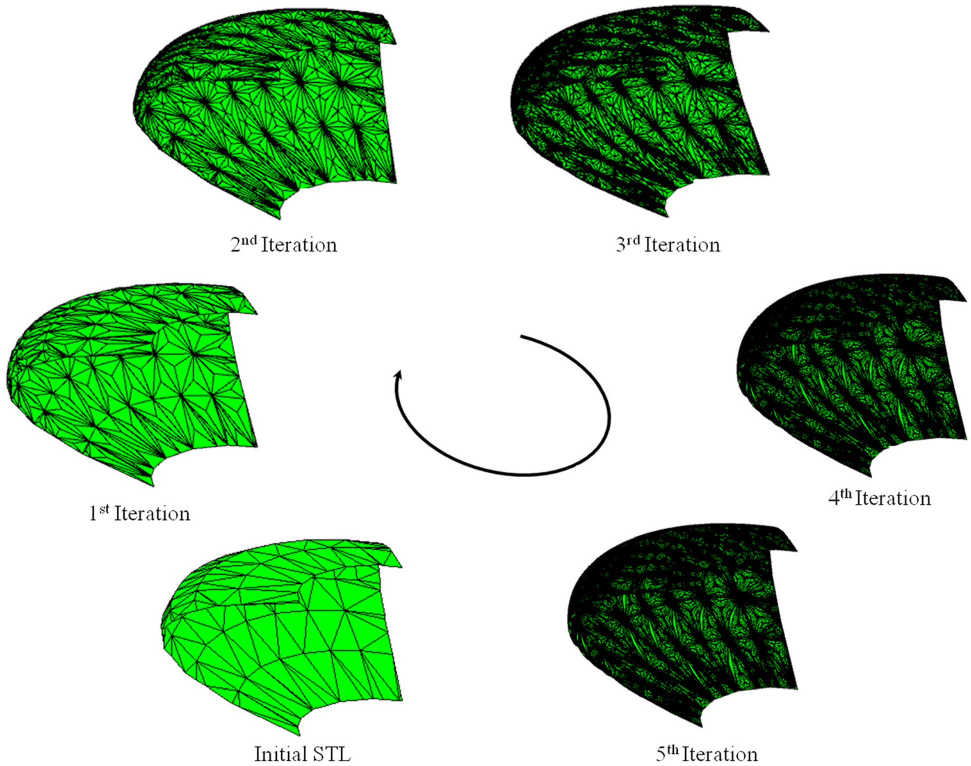


**Fig. 15 Multiple iterations for VTA for test surface 2**

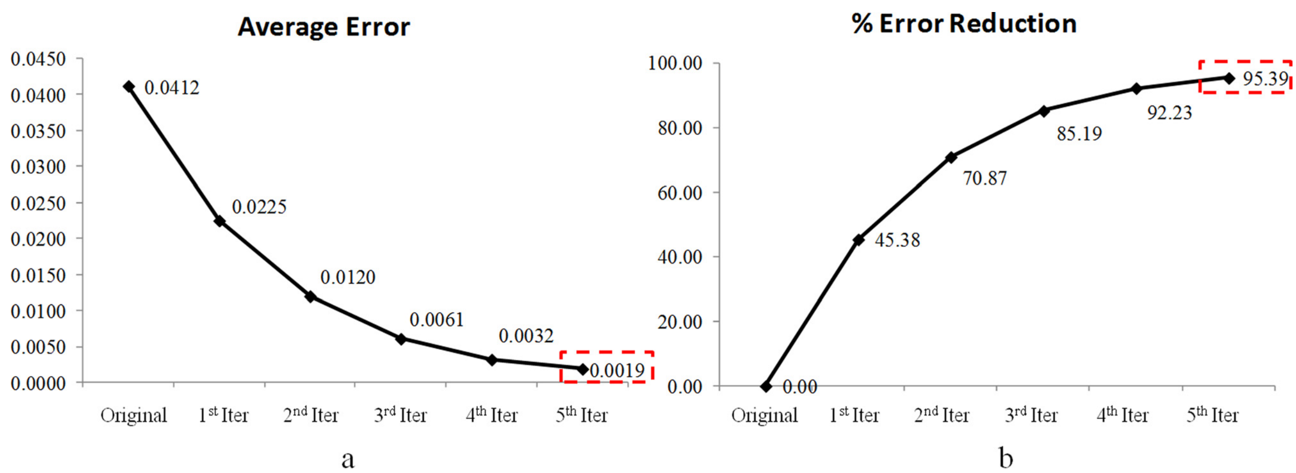


**Fig. 16 (*a*) Average error versus iteration, and (*b*) % error reduction versus iteration for test surface 2**

**Table 2 VTA results summary for test surface 1**

| Stage | Number of facets | Average error (mm) | % Error reduction |
|---|---|---|---|
| Initially | 16 | 0.8469 | — |
| 1st Iteration | 48 | 0.4695 | 44.56 |
| 2nd Iteration | 144 | 0.2563 | 69.74 |
| 3rd Iteration | 432 | 0.135 | 84.06 |
| 4th Iteration | 1296 | 0.0711 | 91.6 |

**Table 3 VTA results summary for test surface 2**

| Stage | Number of facets | Average error (mm) | % Error reduction |
|---|---|---|---|
| Initially | 213 | 0.0412 | — |
| 1st Iteration | 639 | 0.0225 | 45.38 |
| 2nd Iteration | 1879 | 0.012 | 70.87 |
| 3rd Iteration | 5631 | 0.0061 | 85.19 |
| 4th Iteration | 16725 | 0.0032 | 92.23 |
| 5th Iteration | 18747 | 0.0019 | 95.39 |

then the vertex is assumed to satisfy the NURBS equation and kept in the intermediate STL file. Any facet whose vertex does not lie on the NURBS surface per Eq. (3) is deleted from the intermediate STL file. The final STL file with only the facets corresponding to the desired NURBS surface is shown in Fig. 20(*b*).

Thus, the FIA can be used to selectively extract the STL facets corresponding to the surfaces that have to be modified by the VTA. The following section presents how the FIA and VTA can be applied in conjunction to adaptively and locally minimize the chordal errors for different surfaces and compares this approach to the uniform modification of the entire STL file.

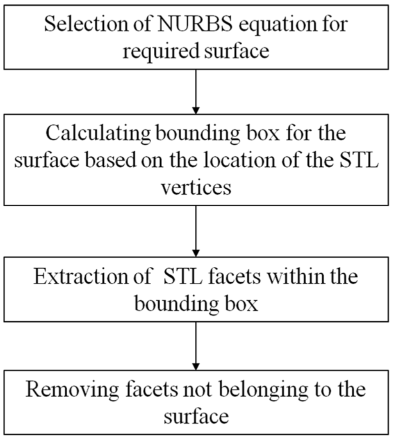


**Fig. 17 FIA methodology**

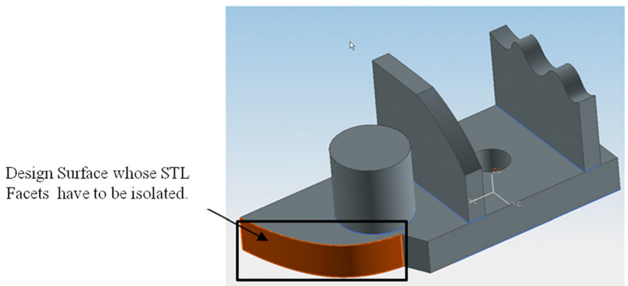


**Fig. 18 FIA example, test part 1**

**4.2 Comparing VTA Approach to Global Refinement.** This section presents an example of how VTA can be applied to modify an STL file with dissimilar levels of tessellations for different surfaces based on their specified error requirements. Figure 21 shows an industrial part, test part 2, which has multiple freeform surfaces with curvatures in both directions. This test part has two critical surfaces, surface 1 with error threshold of 0.008 mm and surface 2 with threshold of 0.02 mm.

The chordal errors specified in the different surfaces in test part 2 can be achieved in two ways (a) globally refining the entire STL file or (b) by adaptively modifying the STL file using the VTA in conjunction with the FIA. The two approaches are shown as follows.

*4.2.1 Global Refinement.* In this approach, the native CAD model of the test part 2 is exported to an STL file iteratively with different CAD-STL conversion tolerances until the chordal error on both of the freeform surfaces becomes less than the minimum of the two specified tolerances, i.e., 0.008 mm. However, in this approach all other surfaces along with the freeform surface with the higher error specification of 0.02 mm are also modified which leads to a higher number of facets. The total number of facets using the global refinement approach is 15 158. The progressive global refinement of the test part is shown in Fig. 22.

*4.2.2 Adaptive Refinement Using VTA.* In this approach, the part model is first exported from the CAD system to an STL file. The STL facets corresponding to the freeform surfaces with the specified tolerances are then isolated using the FIA and stored as intermediate STL files, as shown in Fig. 23. These intermediate STL files are then modified by applying VTA until the chordal errors on the respective surfaces become less than their error thresholds. The individual VTA modified STL files are then stitched back together to form a watertight STL volume. The total number of facets using the VTA approach is 7723, a 49% reduction in the number of facets compared to the global refinement method described in the previous section. The selective refinement of the STL file of test part 2 by VTA is shown in Fig. 23. Figure 24 shows the final STL files achieved by both the schemes and clearly shows that VTA leads to a fewer number of facets as compared to global refinement scheme while still satisfying the error requirements.

## 5 Applying VTA to Reduce Profile and Form Errors

This section analyzes the effect of applying VTA for minimizing profile and form errors of parts manufactured by LM processes. Since the VTA ensures that the new STL facets approximate their corresponding design surface with reduced error, the end result is a tighter approximation of the design surface. Therefore, the part manufactured from the VTA modified STL file will have lower profile and form errors. The general steps involved in the procedure for calculating the effect of VTA on reducing the profile and form errors of the critical features are

(1) The LM part is virtually manufactured using the original unmodified STL file and points are sampled from the virtually manufactured part for inspection analysis. The virtual manufacturing of the part from an STL file using an LM process is explained in detail later in the section.
(2) The form and profile errors are calculated for the required features and surfaces.

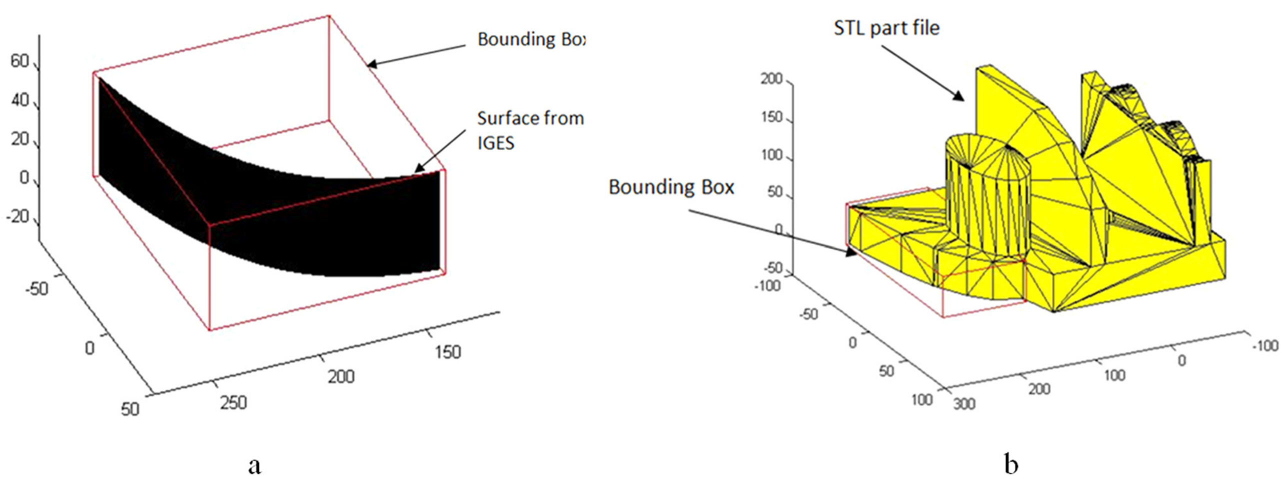


**Fig. 19 (*a*) Extracted NURBS surface from IGES file, and (*b*) superimposition of bounding box on STL file**

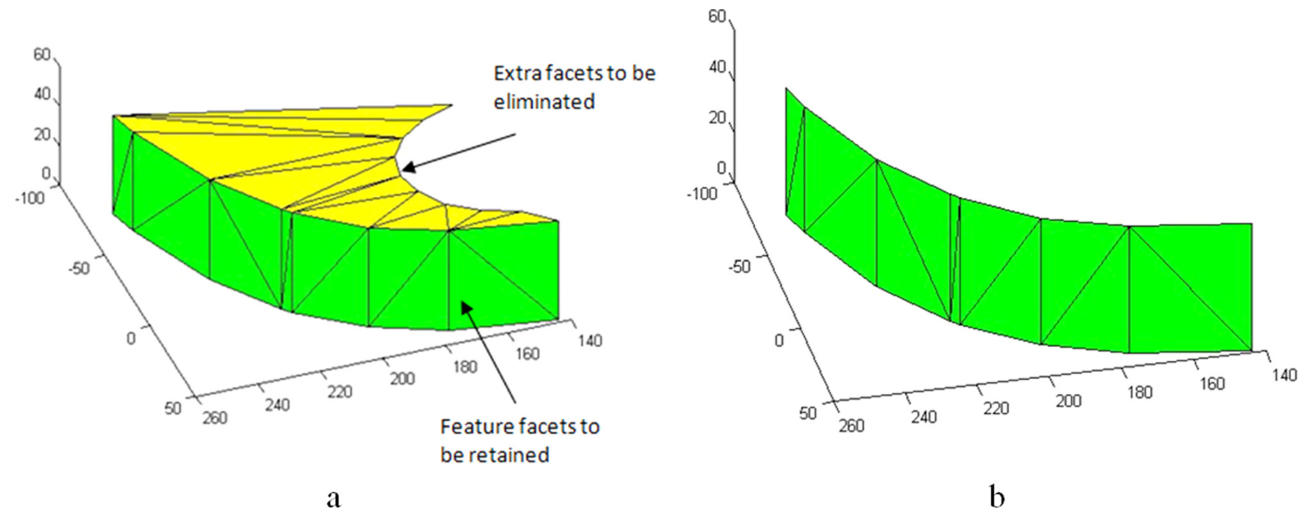


**Fig. 20** (*a*) Intermediate STL file with additional facets, and (*b*) final STL file with extra facets removed

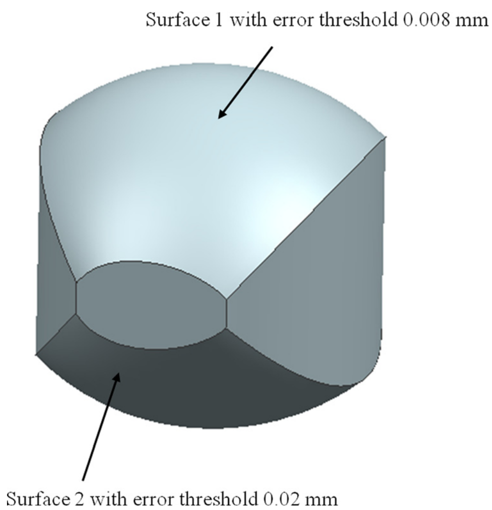


**Fig. 21** Test part 2

(3) If the error on any feature or surface exceeds the tolerance callout, the STL facets corresponding to that feature or surface are isolated using the FIA. The rest of the STL facets are not isolated or modified.
(4) The isolated STL facets are modified by the VTA using a user defined chordal error threshold.
(5) The modified STL facets are then subsequently stitched back together with the unmodified STL facets to create a complete watertight STL facet.
(6) Steps 1–5 are then repeated on this modified STL file until all the form and profile tolerance callouts are met.

The above-mentioned methodology is validated with the help of a test example, test part 1 as shown in Fig. 18. The part is first modeled in NX 7.5 and then exported to the STL file format with a CAD to STL conversion tolerance factor of 0.8 mm. Figure 25 shows the critical features of the part, while Fig. 26 and Table 4 show the form and profile tolerance specifications on the critical features. For the VTA, the overall chordal error threshold is set to 0.05 mm. In this paper, the chordal error specification is assigned arbitrarily. However, in the future, mathematical relationships between this threshold and the actual form and profile errors will be developed so that the chordal error threshold can be assigned more meaningfully. The critical features in the test part are isolated using the FIA and the extracted features are shown in Fig. 27.

For calculating the cylindricity and profile errors for the part features, the part is virtually manufactured with a uniform slice thickness of 0.1 mm and the part is rotated such that axis of the boss is oriented arbitrarily in the direction (0.7071, 0.5, 0.5). Such an orientation is usually selected by the designer based on build time, support structures or other appropriate parameters [15,19,29]. The calculation of the profile and cylindricity errors for the critical features of the manufactured part is based on the ANSI standards [30]. The virtual manufacturing and sampling of points from the simulated surface is performed using the methodology presented in Paul and Anand [15]. The results of the iterative application of VTA on form and profile errors of the different critical features are shown in Tables 5–7. The tables show that it takes three iterations of the VTA to achieve the cylindricity tolerance, five iterations to achieve the profile tolerance on the freeform surface 1 and only two iterations for the freeform surface 2. There is a 73.43% reduction in the cylindricity error while the profile errors on the freeform surfaces 1 and 2 are minimized by 48.98% and 14.36%, respectively. Once the VTA iterations are completed, the modified STL facets are then stitched back

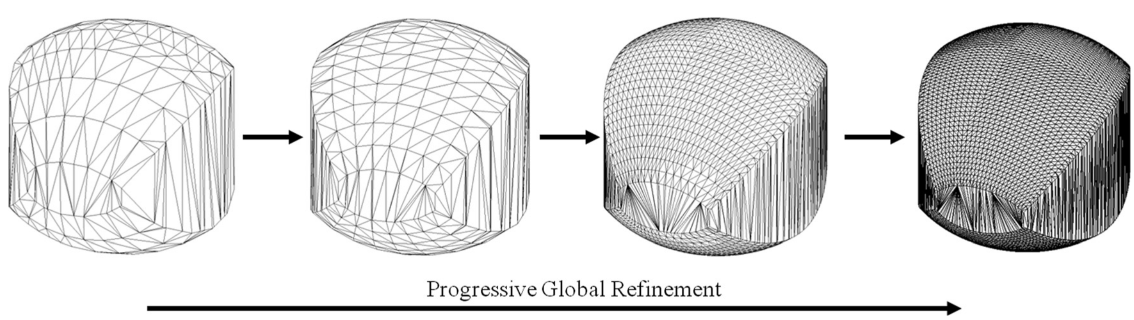


**Fig. 22** Global refinement of test part 2

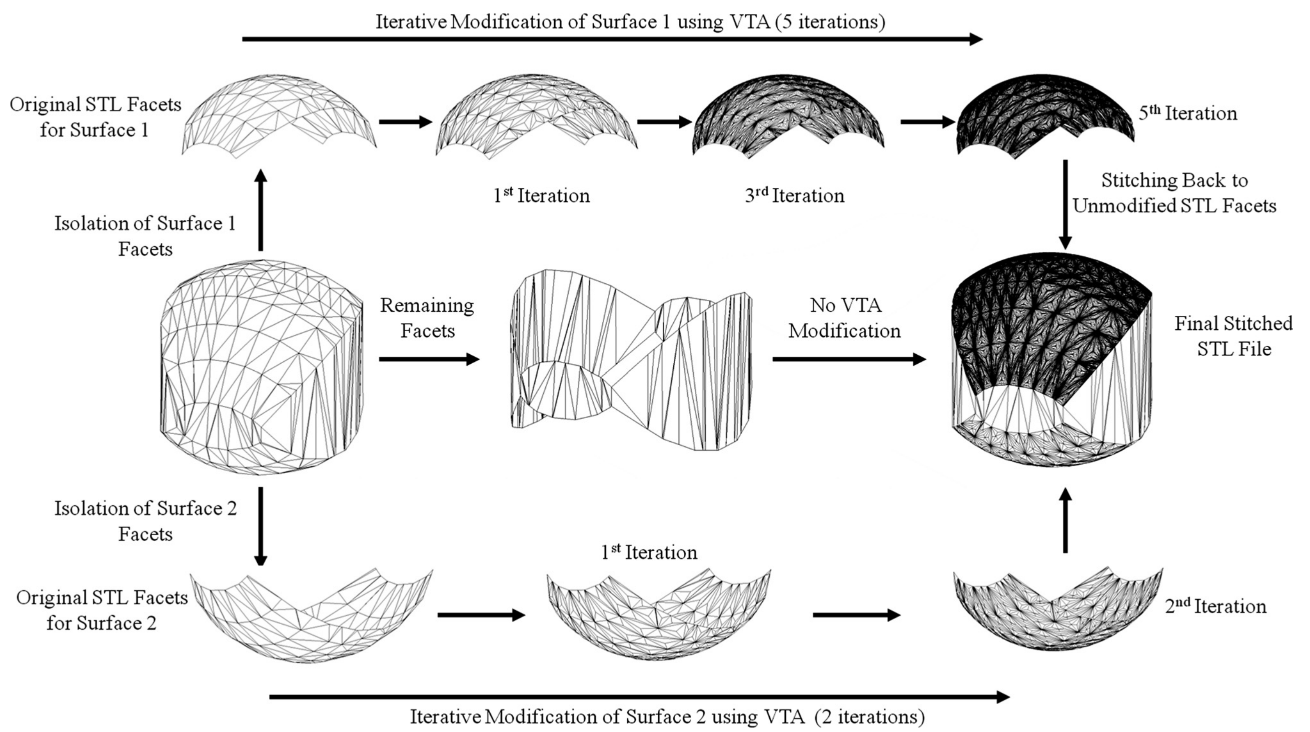


**Fig. 23 Selective refinement scheme for test part 2 STL file by VTA**

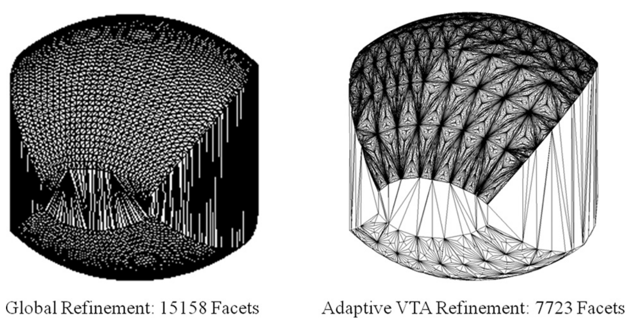


**Fig. 24 Comparison of global refinement and VTA approach**

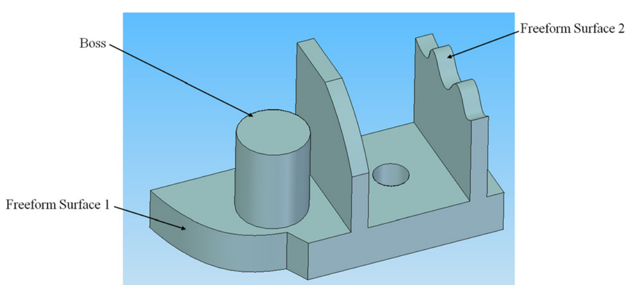


**Fig. 25 Test part 1 for applying VTA to minimize cylindricity and surface profile error**

**Table 4 GD&T tolerances on critical features in test part 1**

| Critical feature | Type of GD&T tolerance | Tolerance value (mm) |
|---|---|---|
| Boss | Cylindricity (⌭) | 0.07 |
| Freeform surface 1 | Profile of a surface (⌓) | 0.035 |
| Freeform surface 2 | Profile of a surface (⌓) | 0.023 |

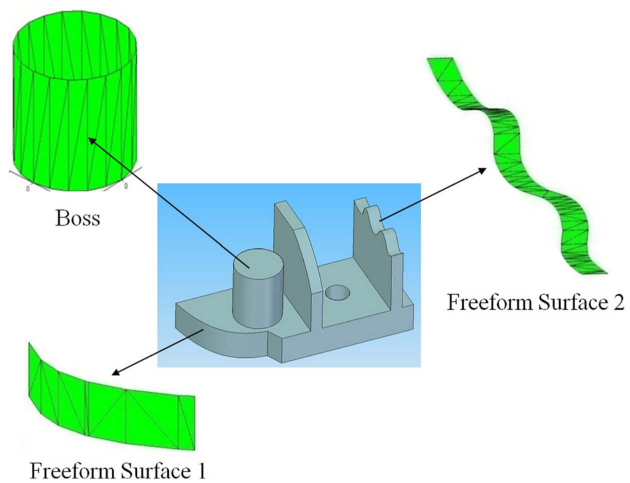


**Fig. 27 Isolated STL feature files using FIA**

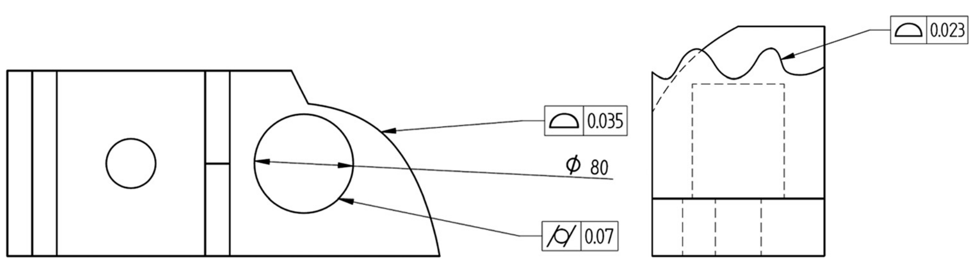


**Fig. 26 Test part 1 tolerance specifications**

Table 5 Effect of VTA in reducing cylindricity error for boss

| Boss | Unmodified STL file from CAD | VTA iterations 1 | 2 | 3 | Tolerance callout specified |
|---|---|---|---|---|---|
| Cylindricity error (mm) | 0.2548 | 0.1330 | 0.0926 | 0.0677 | 0.07 |
| % Improvement—cylindricity error | — | 47.78 | 63.64 | 73.43 | |
| Number of facets | 120 | 360 | 936 | 2376 | |

Table 6 Effect of VTA in reducing surface profile error for freeform surface 1

| Freeform surface 1 | Unmodified STL file from CAD | VTA iterations 1 | 2 | 3 | 4 | 5 | Tolerance callout specified |
|---|---|---|---|---|---|---|---|
| Profile error (mm) | 0.06784 | 0.05106 | 0.04301 | 0.03886 | 0.03603 | 0.03461 | 0.035 |
| % Improvement—profile error | — | 24.73 | 36.60 | 42.72 | 46.89 | 48.98 | |
| Number of facets | 14 | 42 | 126 | 378 | 1134 | 3402 | |

Table 7 Effect of VTA in reducing surface profile error for freeform surface 2

| Freeform surface 2 | Unmodified STL file from CAD | VTA iterations 1 | 2 | Tolerance callout specified |
|---|---|---|---|---|
| Profile error (mm) | 0.02653 | 0.02404 | 0.02272 | 0.023 |
| % Improvement—profile error | — | 9.39 | 14.36 | |
| Number of facets | 76 | 156 | 288 | |

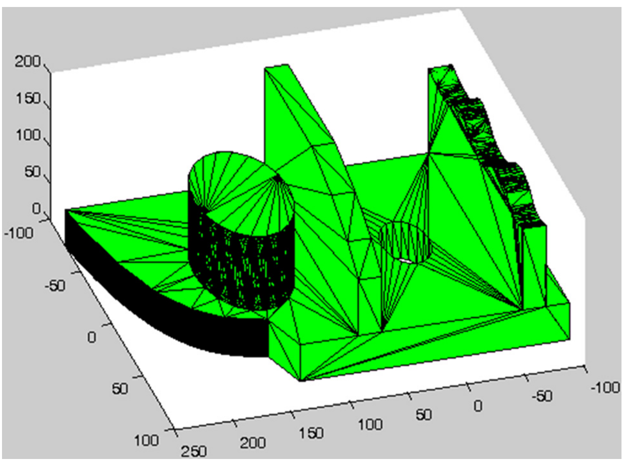


Fig. 28 Final modified STL file

together with the unmodified facets to complete the STL file. The final modified STL file is shown in Fig. 28 which shows the modified facets of the critical features and surfaces.

Thus, the VTA was able to minimize both the cylindricity and the profile errors of the part in order to achieve the GD&T tolerance callouts specified. Therefore, it can be concluded that VTA can be used to selectively modify certain facets of the STL file such that when this modified STL file is used to manufacture the LM part in a specified orientation and slice thickness, the tolerance callouts specified on the critical part features are satisfied. This modified STL file will ensure that all specified tolerance callouts are satisfied the first time the part is manufactured.

## 6 Conclusion and Future Scope

In this paper, a new algorithm for localized STL file modification has been presented. The algorithm named as the vertex translation algorithm (VTA) modifies the STL file based on the chordal error requirements by translating the point on each STL facet with the maximum chordal error to its corresponding design points. A facet isolating algorithm (FIA) was developed which isolates the STL facets corresponding to the surfaces being analyzed. The facets extracted from the FIA along with the specified error are used as an input to the VTA. The translation algorithm was applied successfully on two test surfaces and was able to reduce their chordal errors by 91.6% and 95.39%. In addition to the chordal error, the VTA was also applied to reduce the form and profile errors on critical features of a service part manufactured using an LM process. The VTA was able to reduce the cylindricity errors of a cylindrical feature by about 73.43% and the profile errors of two freeform surfaces by approximately 48% and 14%. The methodology developed in this paper will provide LM engineers a method for selectively modifying the STL file quality for achieving the required tolerances specified on the part features. This will eliminate the manufacturing of defective parts and reduce the time associated with producing parts in the LM process, thereby leading to reduced material expenditure and lower costs.

The present algorithm has a limitation in that it ignores a point with maximum chordal error if that point lies on the edge of the STL facet. This limitation has to be removed in order to make this algorithm more robust and foolproof. One method to circumvent this limitation is to include additional points closer to the edge of each facet for chordal error calculation. The current research concentrates on modifying STL file of the part. Future work may involve modifying the slice contours by comparing the STL and NURBS slices to reduce the error locally at the slice level and rebuilding the modified STL files from the slice contours. Incorporating LM machine errors while modifying the STL file by the VTA can be another approach for minimizing the errors on the final part manufactured by the LM machine. Current STL files approximate the curved surfaces of a part with planar triangular facers. If these planar facets can be replaced wholly or partially by spherical or Bezier triangles, the chordal errors and by extension, form and profile errors, can be minimized drastically.

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