TCAD Simulations for FinFet Transistors

Project report submitted in partial fulfillment of the requirement for the degree of

Bachelor of Technology

Submitted by

Koteswara Bezawada(2010111057)
And
Maddipatla Bhardwaj(2010110372)

Under Supervision of

Dr.Atul Vir Singh
Department of Electrical Engineering

and
Dr.Jitendra Prajapati
Department of Electrical Engineering

Department of Electrical Engineering
School of Engineering
Shiv Nadar Institution of Eminence

(December 2023)

Candidate Declaration

We hereby declare that the thesis entitled "TCAD Simulations for FinFet Transistors" submitted for the B. Tech. degree program. This thesis has been written in our own words. We have adequately cited and referenced the original sources.

Koteswara Bezawada
(2010111057)

Maddipatla Bharadwaj
(2010110372)

Certificate

It is certified that the work contained in the project report titled "TCAD Simulations for FinFet Transistors," by "Koteswara Bezawada" has been carried out under our supervision and that this work has not been submitted elsewhere for a degree.

Dr.Atul Vir Singh
Dept. of Electrical Engineering
School of Engineering
Shiv Nadar Institution of Eminence
Date: 28/11/2023

Dr.Jitendra Prajapati
Dept. of Electrical Engineering
School of Engineering
Shiv Nadar Institution of Eminence
Date: 28/11/2023

Certificate

It is certified that the work contained in the project report titled "TCAD Simulations for FinFet Transistors," by "Maddipatla Bharadwaj" has been carried out under my/our supervision and that this work has not been submitted elsewhere for a degree.

Dr.Atul Vir Singh
Dept. of Electrical Engineering
School of Engineering
Shiv Nadar Institution of Eminence
Date: 28/11/2023

Dr.Jitendra Prajapati
Dept. of Electrical Engineering
School of Engineering
Shiv Nadar Institution of Eminence
Date: 28/11/2023

Abstract

In this project, we aim to observe TCAD simulations of FinFET Transistors with different technology nodes and parameters. A FinFET or Fin Field-Effect Transistor is classified as a multi-gate MOSFET (Metal Oxide Semiconductor FET). A multi-gate transistor incorporates more than one gate into one single device. These devices are used in switching or amplifying signals. FinFETs are designed to overcome certain limitations of traditional planar MOSFETs as transistor sizes continue to shrink. In FinFETs, the channel is a raised and "fin" structure above the substrate, allowing better control over current flow. This fin is made from a thin layer of semiconductor material (typically silicon) that rises vertically from the silicon substrate. The gate electrode surrounds the sides of the fin, allowing for better control of the transistor's operation. This design provides improved performance, reduced leakage current, and better scalability. TCAD tools enable us to develop and optimize various physical models and observe the effects on different parameters. In the following report, we will present the Id-Vg characteristics of different 2-D FinFET models. We will be simulating models on different material properties and device structure characteristics like dimensions. Furthermore, we will also observe the threshold voltage, which is the voltage required to turn the transistor on. TCAD tools help analyze how the threshold voltage changes with different design parameters and bias conditions.

Contents

List of Figures

Chapter 1

Introduction

In the realm of semiconductor technology, FinFET transistors stand out as a promising advancement. They play a pivotal role in enhancing the performance and energy efficiency of our electronic devices, particularly in cutting-edge technology nodes. Unlike traditional flat transistors, FinFETs employ a three-dimensional structure with multiple gates surrounding the transistor body, which enables precise control over their operation. This results in the effective suppression of power leaks and improved performance.

Accurate modeling and simulation are essential to harness the potential of FinFET transistors. This project focuses on TCAD (Technology Computer-Aided Design) simulations tailored to the specific requirements of FinFET devices. By leveraging insights gained from TCAD simulations in planar nodes, we delve into 3D FinFET process modeling. We investigate how channel and extension source/drain (S/D) implantation and annealing processes affect crucial device characteristics, including electrostatic control and threshold voltage mismatch. These factors are pivotal in achieving optimal performance in advanced semiconductor technologies.

This report provides a comprehensive overview of our research in this domain, offering insights into the design and optimization of FinFET-based integrated circuits. Our aim is to contribute to the ongoing progress of semiconductor technology by unlocking the full potential of FinFET transistors. As we explore this technology, we'll uncover how it holds the key to further improving the electronic devices that have become integral to our daily lives, setting the stage for a more powerful and energy-efficient future.

1.1 Motivation:

Proficiency in TCAD simulations of FinFETs is a valuable skill in the semiconductor industry. Moore's Law, which predicts the doubling of the number of transistors on a microchip every two years, has been a driving force in the tech industry. Individuals working on FinFETs and TCAD simulations play a part in ensuring this law continues to hold true, enabling the development of faster and more efficient electronic devices.

The complex and innovative nature of FinFETs piques the intellectual curiosity of researchers. Understanding the intricacies of their design and optimizing their performance through simulations can be intellectually rewarding.

1.2 Problem Statement:

There is a need to develop comprehensive TCAD simulation methodologies to accurately model the behavior of FinFET transistors, predict their electrical characteristics, and overcome existing limitations. Specifically, this research addresses issues related to power efficiency, reliability, and variability in FinFET devices.

Our goal is to leverage TCAD Software and observe FinFETs characteristics like the Id - Vg curve, doping profiles, electron densities and electron mobilities, etc.

Chapter 2

Literature Survey

The landscape of semiconductor technology has witnessed a transformative shift with the advent of FinFET transistors, offering a three-dimensional architecture that addresses the challenges faced by traditional planar transistors. The effective utilization of Technology Computer-Aided Design (TCAD) simulations in understanding and optimizing FinFET devices is critical for advancing semiconductor technology. This literature survey explores existing research and developments in TCAD simulations of FinFET transistors, focusing on key aspects such as design optimization, electrical characteristics, and practical applications.

2.1 Understanding the working of a MOSFET:

A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a fundamental electronic device that plays a pivotal role in modern electronics. It is a type of transistor used for switching and amplifying electronic signals in a wide range of applications, from microprocessors in computers to power amplifiers in audio equipment. Its operation is based on the modulation of the conductivity of a semiconductor channel through the application of an electric field. MOSFETs have three terminals: the Source, Drain, and Gate. There are two main types of MOSFETs: N-channel (NMOS) and P-channel (PMOS).

The NMOS transistor operates primarily in the enhancement mode, meaning it is normally off and requires a voltage at the Gate terminal to turn it on. The Gate voltage controls the conductivity of the channel, making the NMOS a voltage-controlled device. It is worth noting that the operation of the NMOS is fundamentally based on the principle of majority carriers (holes in this case) and minority carriers (electrons), allowing for precise control of the flow of current.

The operation of the PMOS is complementary to the NMOS. In this case, the transistor is normally in an "on" state when the Gate voltage is zero or positive. When a sufficient positive voltage is applied to the Gate, the accumulation region is created, allowing current to flow between the Source and Drain terminals. Conversely, lowering the Gate voltage turns the transistor off, depleting the accumulation region and interrupting the conductive path.

2.2 Transition from planar MOSFETs to FinFets:

Traditional planar MOSFETs were widely used in electronics for many years. However, as technology nodes scaled down, these devices faced several challenges, including increased power leakage and short-channel effects. The semiconductor industry transitioned to FinFETs (Fin Field-Effect Transistors) to address these limitations.

FinFETs are a new generation of transistors with a 3D structure. Instead of a planar channel, they feature a thin vertical fin-like structure. The Gate in a FinFET fully wraps around the fin, providing enhanced control and improving electrostatics. The use of FinFETs allowed for the continued scaling of technology nodes, ensuring that electronic devices could become faster, more power-efficient, and smaller.

2.3 FinFETs:

FinFETs are characterized by a 3D transistor structure, replacing the planar channel with a thin vertical fin-like structure. The term "Fin" is aptly derived from this unique feature. These transistors have Source and Drain terminals and a Gate terminal, much like traditional MOSFETs. However, it's the design of the channel that sets FinFETs apart. The fin's vertical orientation enables multiple gates to wrap around it, ensuring enhanced electrostatic control. The operation of FinFETs relies on the modulation of the channel's conductivity by applying an electric field through the Gate.

There are two primary types of FinFETs, each characterized by the type of charge carrier they predominantly use. These types are N-channel FinFETs (NFET) and P-channel FinFETs (PFET). Let's explore each of these in more detail:

2.3.1 N-Channel FinFet(NFET):

Structure: NFETs are designed with an N-type fin, where the fin is composed of N-type (negatively doped) semiconductor material. The Source and Drain regions in NFETs are typically P-type. Operation: In an NFET, when a positive voltage is applied to the Gate terminal, it forms an electric field in the N-type fin. This electric field attracts negatively charged electrons (majority carriers) toward the silicon-oxide layer and repels positively charged holes (minority carriers) away from it. This creates an accumulation of electrons at the silicon-oxide interface, allowing current to flow between the Source and Drain terminals. NFETs are often used in electronic circuits for amplification, signal processing, and switching functions.

2.3.2 P-Channel FinFet(PFET):

Structure: PFETs have a P-type fin, with the fin composed of P-type (positively doped) semiconductor material. The Source and Drain regions in PFETs are usually N-type. Operation: In a PFET, when a negative voltage is applied to the Gate terminal, an electric field is established within the P-type fin. This electric field attracts positively charged holes (majority carriers) toward the silicon-oxide layer and repels negatively charged electrons (minority carriers) away from it. This creates an accumulation of holes at the silicon-oxide interface, allowing current to flow between the Source and Drain terminals.

PFETs complement NFETs in electronic circuits, often used for complementary metal-oxide-semiconductor (CMOS) technology, where they work together to create digital logic gates and other applications.

2.4 Analyzing FinFet behavior with TCAD Simulations:

TCAD simulations provide a powerful means to gain insights into the performance, characteristics, and reliability of FinFET devices. Here's an overview of how TCAD simulators are employed for this purpose:

2.4.1 Device Characterization:

TCAD simulations are used to characterize the electrical behavior of FinFETs. By inputting parameters such as material properties, gate voltages, and physical dimensions, researchers can model how FinFETs respond to different operating conditions.

2.4.2 Performance Optimization:

TCAD simulators help in optimizing the performance of FinFETs. Researchers can explore various design parameters, including gate length, fin width, and doping profiles, to determine the configurations that yield the best results in terms of speed, power consumption, and leakage current.

2.4.3 Scaling and Technology Node Advancement:

As semiconductor technology advances, TCAD simulations are invaluable for scaling FinFETs to smaller technology nodes. Researchers use TCAD to assess how FinFETs perform at increasingly smaller sizes and to predict their behavior at advanced nodes.

2.4.4 Short Channel Effects Analysis:

Short-channel effects become more pronounced as FinFETs are scaled down. TCAD simulators are used to study and address these effects, such as drain-induced barrier lowering (DIBL) and subthreshold swing, which can impact device performance.

Chapter 3

Work Done

Our initial research was based on acquiring knowledge of the working of MOSFETs and the transition from MOSFET to FinFET and then the working of FinFET. Later, we have used a simulation software for transistor modelling called Synopsys Sentaurus TCAD tool. This tool helped us to design a 2-D FinFET model. Sentaurus TCAD tool allows us to test the designed device under various physics models. We had to use three of the tool's components to study our design. Sentaurus Structure Editor (sde)- This is a 2D and 3D editor, Sentaurus Device is used to simulate the electrical characteristics of the device. Finally, Sentaurus Visual is used to visualize the output from the simulation in 2D and 3D and inspect is used to plot the electrical characteristics. We have also used a GitHub TCAD model called MuGFET tool by nanoHUB.org. This model helped us in giving the Id-Vg curves for most parts of the project.

3.1 TCAD Model

Here's a detailed explanation on how we had modelled our first FinFET:

1. After opening the sde from terminal, we proceed to start drawing our 2-D Cross-section of the FinFET. We needed to make sure that we draw using the exact coordinates.

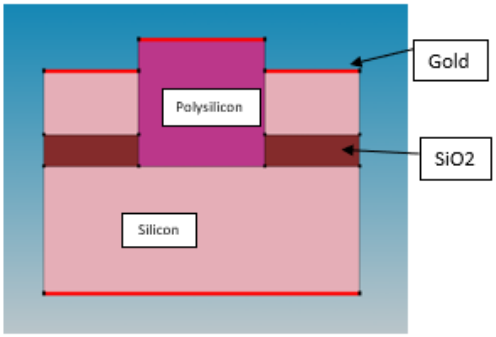

Figure 3.1: 2-D FinFET Model

The following table refers to the dimensions of the 2-D Model

Material/Region	Width (X-axis)	Length(Y-axis)
Silicon (Substrate Region)	10µm	4µm
SiO2 (Source Base Region)	3µm	1µm
Si (Source Material Region)	3µm	2µm
Polysilicon (Gate Region)	4µm	4µm
Gold Metal Contact (S,D)	3µm	0.05µm

Figure 3.2: Table1. Dimensions of 2-D FinFET model

2. Now we set our contacts for all the four electrodes Drain, Gate Source and Body (D,G,S,B).

3. The next step is to dope the regions with Phosphorus active concentrations. The substrate region (Si) and Source and Drain regions (Si) are doped with Phosphorus. While the Gate region is doped with Phosphorus.

4. After doping, we define our boundary conditions by creating reference evaluation windows in two regions. First, we create a reference evaluation window for the entire model. Next, we create a window for the entire channel region, which covers the source gate, drain and only some part of the substrate region. We make these windows to build a mesh.

5. We then refine our placement evaluation windows by defining the maximum and minimum values of the elements present in the mesh. The size of the elements in the bigger evaluation window is greater than the size of the elements in the smaller evaluation window.

6. We also define our interfaces, which essentially are the places where two materials within the structure meet. (Eg. Silicon-Polysilicon, SiO2-Polysilicon, SiO2-Silicon etc). The Green window covers channel region while yellow covers the entire model.

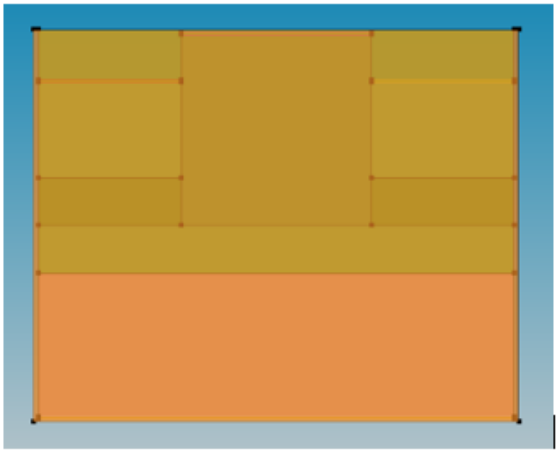

Figure 3.3: Reference Evaluation Windows (GreenYellow)

7. The mesh when generated discretizes the semiconductor structure into a grid of small elements, allowing the numerical solution of these complex equations. This dis-

cretization is essential for approximating the behavior of semiconductor materials and devices. It defines the boundary conditions of the device, including contacts and interfaces. It ensures that appropriate conditions are applied to simulate real-world device behavior.

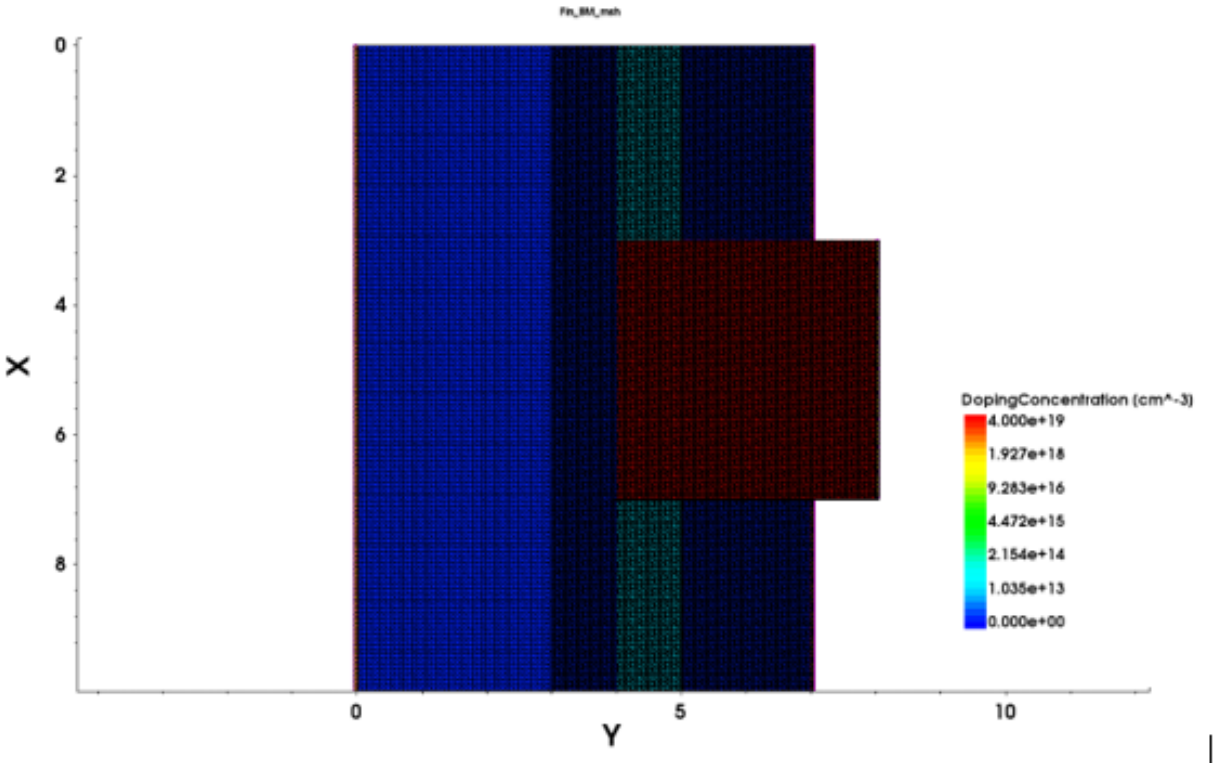

Figure 3.4: Generated Mesh Window in svisual

8. After building the mesh, we needed to obtain our Id-Vg Characteristic curve, which is plotted by taking X-axis as Gate OuterVoltage and Y-axis as Drain eCurrent.

9. In order to get this curve, we need to write a sdevice file for the model. This file contains information related to semiconductor devices and is used in the simulation and analysis of semiconductor processes and devices. These files are used to specify the parameters and characteristics of the semiconductor devices you want to model and simulate using Sentaurus.

10. The specific contents of a "sdevice" file can vary depending on the simulation and analysis being performed, but it generally includes information such as: Device Geometry, Doping Profiles, Material Properties, Operating Conditions, Model Parameters, Boundary Conditions etc.

While implementing this code, we faced a few discrepancies for which we had used another online CAD tool called MuGFET Tool by nanoHUB.org to replicate the scenario. This tool helped us in obtaining Id-Vg curve.

```
File {
*-Input
        Grid=       "Fin_BM_msh.tdr"
        Parameter= "Silicon.par"
        Parameter= "Polysilicon.par"
        Parameter= "SiO2.par"
*-Output
        Current=    "Fin.plt"
        Plot=       "Fin_msh.tdr"
        Output=     "Fin_msh.log"
}
Electrode {
        { Name= "Drain"   Voltage= 4}
        { Name= "Gate"   Voltage= -5 }
        { Name= "Source"   Voltage= 0 }
        { Name= "Body"   Voltage= 0}
}
Physics {
        *AreaFactor= 5                  *geometry scaling in z direction
        Temperature= 300                * temperature in Kelvin
        Thermionic
        Mobility(Enormal DopingDep)
        Recombination (SRH(DopingDependence))
        EffectiveIntrinsicDensity(OldSlotboom)
}
Plot {
*- Doping Profiles
        DopingConcentration DonorConcentration AcceptorConcentration
*- Carrier Densities:
        eDensity hDensity
*- Fields, Potentials and Charge distributions
        Potential
*- Currents
        eCurrent hCurrent
        eMobility hMobility
}
Math {
        Extrapolate
        RelErrcontrol
        Digits= 5
        Notdamped= 40
        Iterations= 30
        ElementEdgeCurrent
        ErrRef(electron)= 1e-1
        ErrRef(hole)= 1e-1
        TrapDLN=50
        method=pardiso
}
Solve {
        Coupled (Iterations= 200){ Poisson Electron Hole }
        Plot (FilePrefix= "Fin")

        Quasistationary (
                InitialStep= 1e-2
                MinStep= 1e-4     MaxStep= 0.01
                Goal { Name="Gate" Voltage= 0 }
        ){ Coupled { Poisson Electron Hole } }

}
```

Figure 3.5: Sdevice code for the FinFET Model

3.2 MuGFET CAD Tool

MuGFET simulates quantum transport at the nanoscale, which is close to the atomistic dimension. This tool operates on the Drift-Diffusion way which makes it work well enough to demonstrate characteristics of relatively long and large devices. This tool further works on two models which are as follows.

3.2.1 PADRE

The "Padre Simulator" is a comprehensive tool for simulating semiconductor devices, taking into account various physical phenomena and models to provide insights into the behavior of carriers in a semiconductor material. The simulation includes considerations for advanced effects such as hot carrier transport, concentration-dependent mobility, and impact ionization.

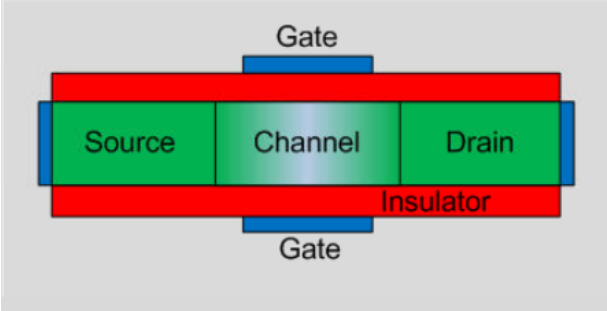

Figure 3.6: 2-D FinFET in MuGFET

3.2.2 PROPHET

Prophet is a simulator designed specifically for equilibrium conditions in electronic devices. It provides options for different plot dimensions, includes Newton iteration parameters for convergence, and incorporates models such as quantum corrections and Lombardi's transverse field-dependent mobility model to capture the intricacies of semiconductor device behavior.

3.2.3 Results and Observations in MuGFET

In the online TCAD tool, we chose the PADRE Simulator. Using this simulator, we arrive at our Id-Vg characteristic curves by varying a few parameters which are as follows:

Firstly, we select our standard models with two gate types with the following parameters:(Figure 3.7)

- Gate Type: Metal and Poly
- Channel Width: 30nm, Oxide thickness: 2.5nm
- Doping: Channel Concentration = 1e+16/cm3
- Gate Work Function: 4.6eV
- Dielectric Material: SiO2(3.9)

After this we start varying the parameters to analyse the model. Refer to Figure 3.8.

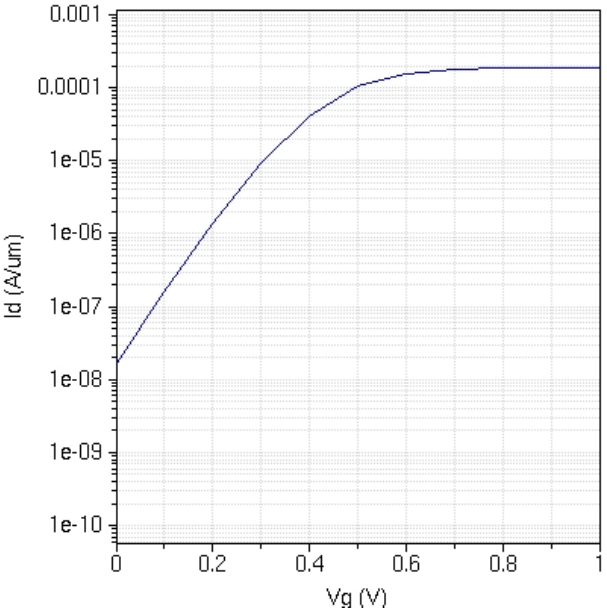

Figure 3.7: Id-Vg Curve of Standard Model with Gate type as Metal

Observations:

- For Figure 3.9: The graph likely shows a typical Id-Vg characteristic of a FinFET with a moderate channel width, indicating good gate control over the channel.
- For Figure 3.10: A further increase in channel width may show a trend of increased drain current, suggesting less electrostatic control by the gate.
- For Figure 3.11: This graph could represent the effects of varying doping concentrations on the drain current, potentially indicating threshold voltage shifts due to changes in the doping levels.
- For Figure 3.12: Similar to the previous, variations in doping might be shown to affect the sub-threshold slope or drive current.
- For Figure 3.13: A different gate work function value (4.28eV) would alter the threshold voltage, which may be reflected in the graph as a shift in the Id-Vg curve.
- For Figure 3.14: This suggests that the work function of the gate material is set to 4.5eV, which may influence the threshold voltage and turn-on characteristics of the FinFET.
- For Figure 3.15: If this is related to using Aluminum Oxide as a dielectric with a thickness of 9 units (perhaps angstroms), it could show its effect on the leakage current and gate capacitance.
- For Figure 3.16: This might indicate the use of Hafnium Oxide with a thickness of 25 units, which could highlight its high-k dielectric properties affecting the device's scalability and performance.

Metal	Poly
• Channel Width: 15nm 45nm	
• Doping: Source and Drain Conc.: 1e+19/cm^3 Channel Concentration: 1e+20/cm^3 Source and Drain Conc: 1e+18/cm^3 Channel Concentration: 1e+19/cm^3	
• Gate Work Function: 4.28 (Aluminium) 4.5 (Chromium)	
• Dielectric Material: HfO_2 Al_2O_3	

Figure 3.8: Tables with Parameters which we have varied

- For Figure 3.17: The sub-threshold slope appears steep, and the drive current is high, which may indicate a thin gate oxide or high channel mobility.
- For Figure 3.18: The Id-Vg curve indicates a higher threshold voltage or weaker inversion, possibly due to a thicker gate oxide or less effective gate material.
- For Figure 3.19: The overall shape of the curve suggests good electrostatic control, but with a slightly increased leakage current, potentially due to the thicker gate oxide or higher doping levels.
- For Figure 3.20: The curve shows an abrupt turn-on characteristic, indicating a low threshold voltage, which could result from aggressive scaling or a highly effective gate work function.
- For Figure 3.21: The curve indicates a transistor with a slightly lower threshold voltage than in the poly(4.5) case, likely due to the different gate work function.
- For Figure 3.22: The Id-Vg curve indicates a relatively flat sub-threshold region and a gradual current increase, suggesting a higher threshold voltage or weaker inversion in the transistor.
- For Figure 3.23: The curve reveals a smooth but less steep sub-threshold region, hinting at stable but possibly less aggressive transistor behavior with the given dielectric material.

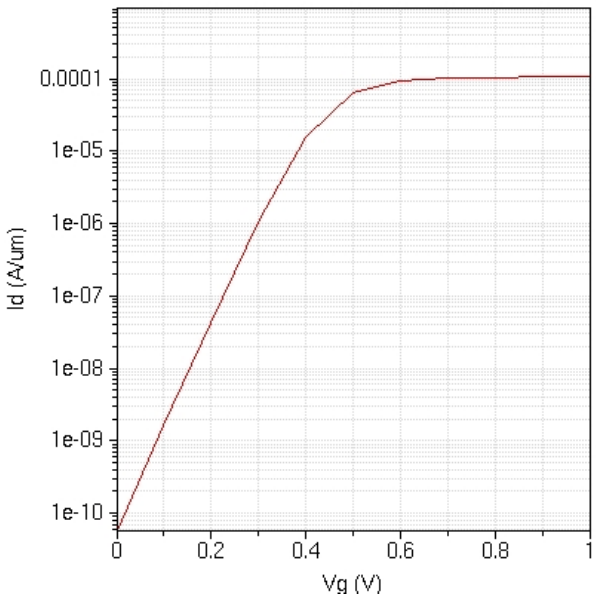

Figure 3.9: Channel Width Metal=15nm

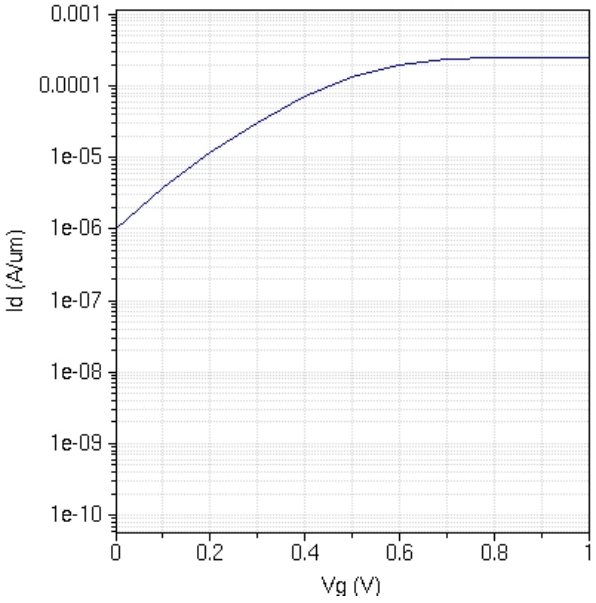

Figure 3.10: Channel Width Metal=45nm

- For Figure 3.24: The graph suggests a well-controlled off-state with low leakage current and a sharp transition to the on-state, characteristic of high-k dielectrics at work.

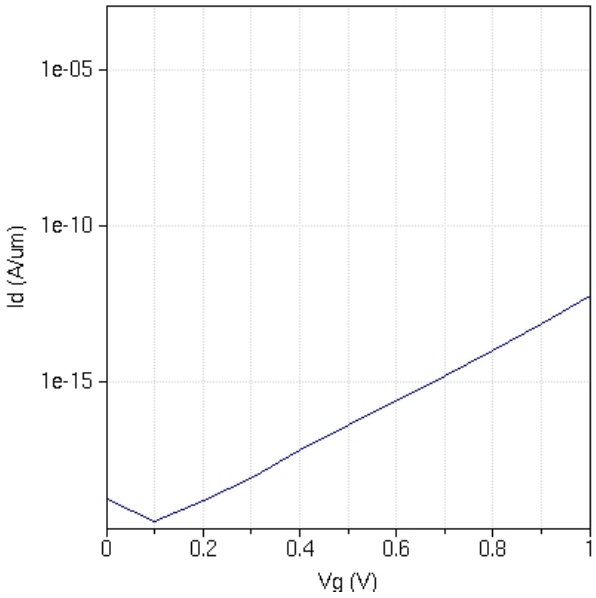

Figure 3.11: Channel Doping Concentration=1e+19cm3

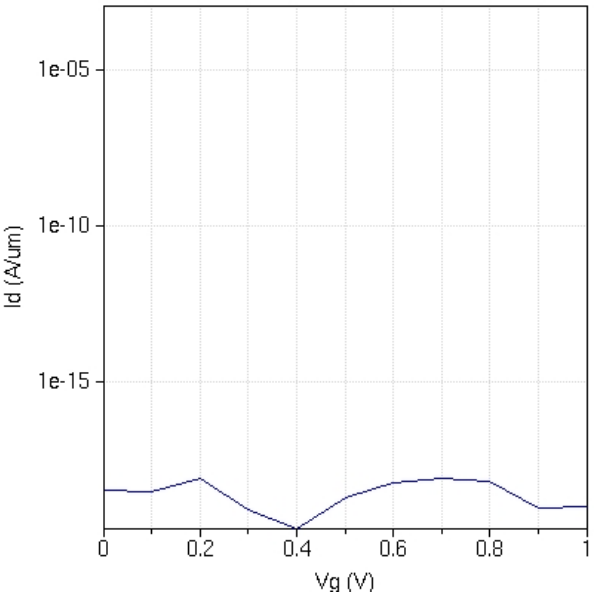

Figure 3.12: Channel Doping Concentration=1e+20cm3

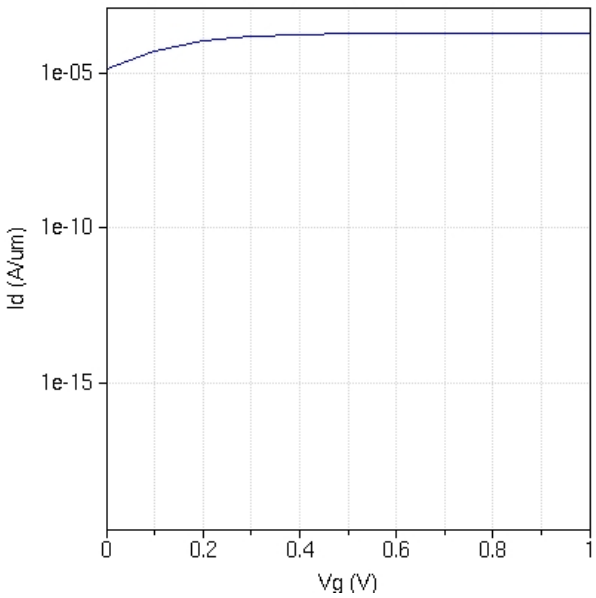

Figure 3.13: Gate Work Function: Aluminium 4.28eV

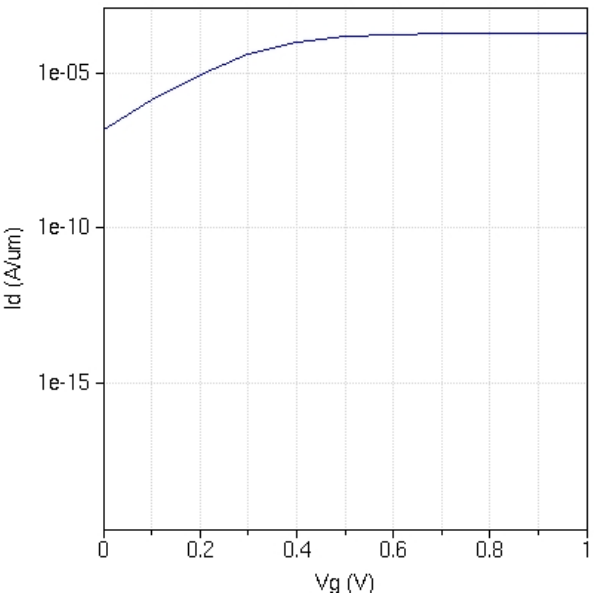

Figure 3.14: Gate Work Function: Chromium 4.5eV

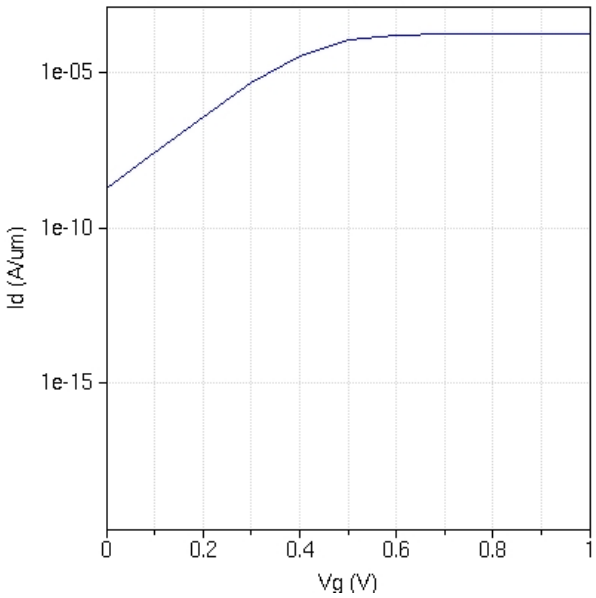

Figure 3.15: Dielectric Material: Al203(9)

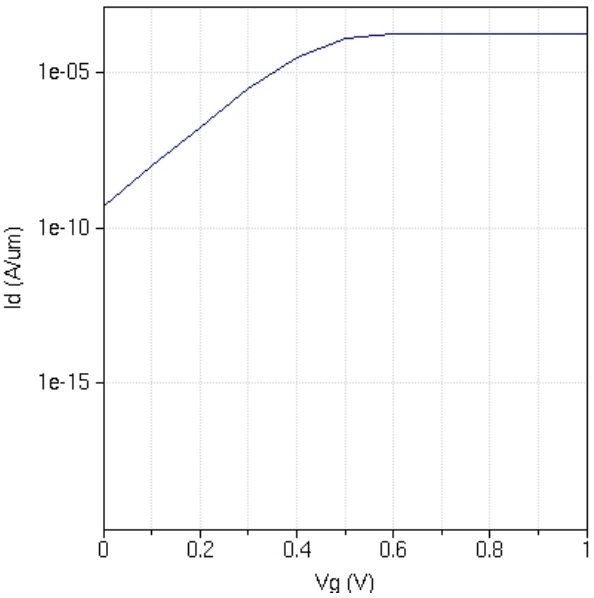

Figure 3.16: Dielectric Material: HfO2(25)

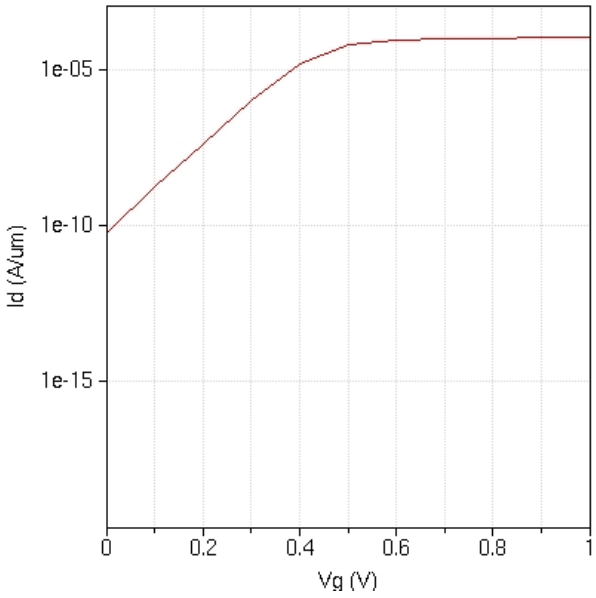

Figure 3.17: Channel Width Poly=15nm

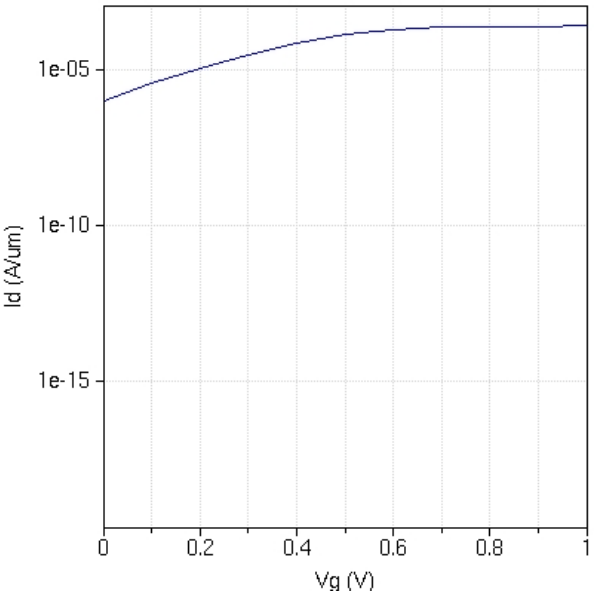

Figure 3.18: Channel Width Poly=45nm

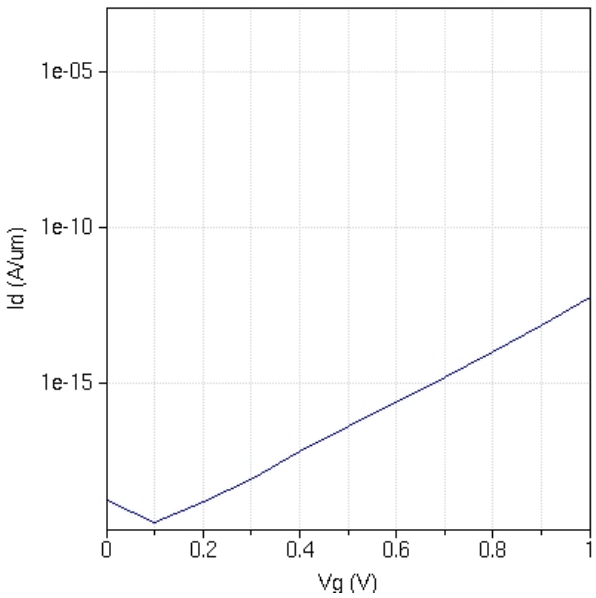

Figure 3.19: Channel Doping Concentration(P)=1e+19cm3

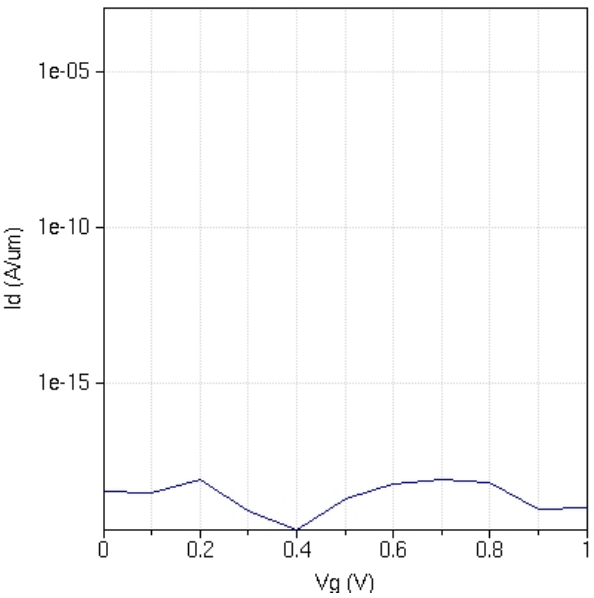

Figure 3.20: Channel Doping Concentration(P)=1e+20cm3

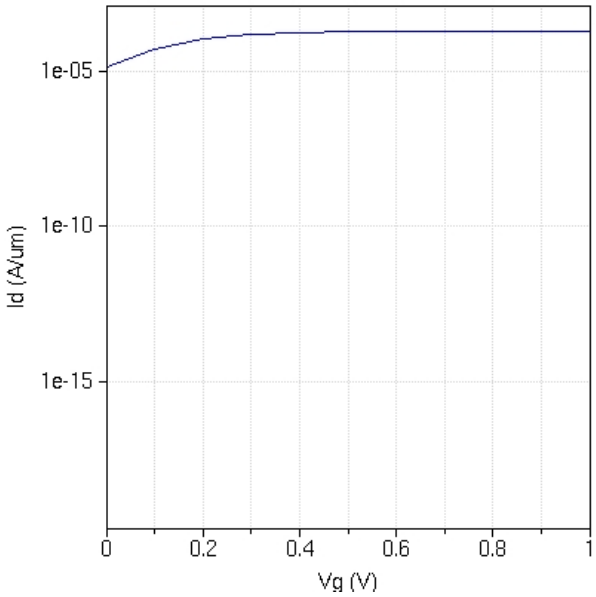

Figure 3.21: Gate Work Function(P): Aluminium 4.28eV

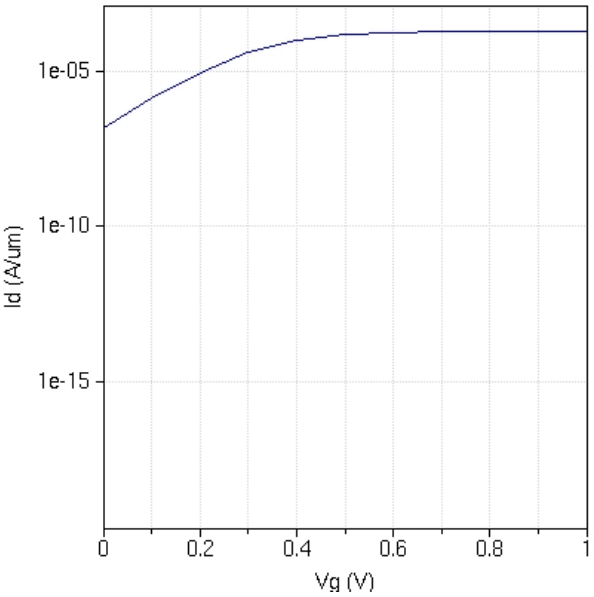

Figure 3.22: Gate Work Function(P): Chromium 4.5eV

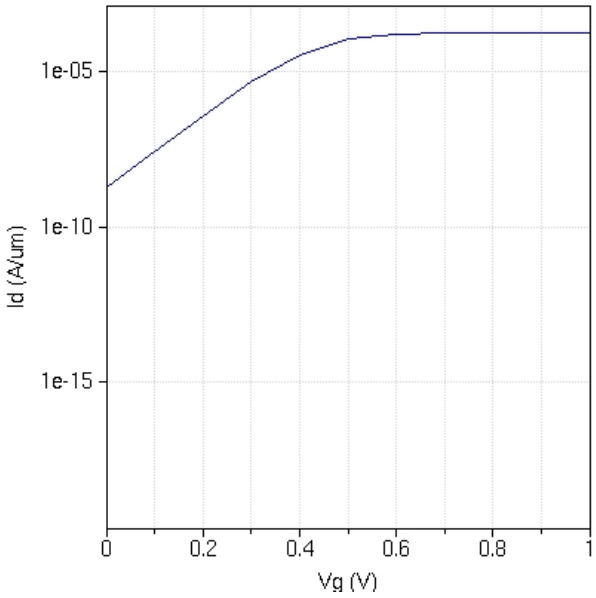

Figure 3.23: Dielectric Material(P):Al203(9)

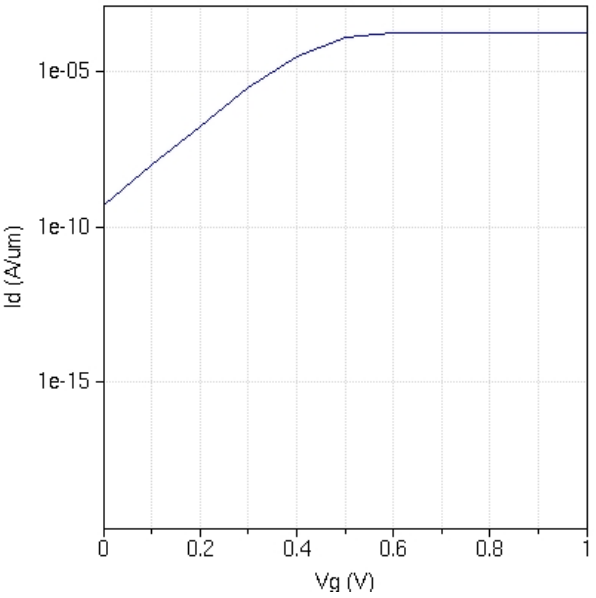

Figure 3.24: Dielectric Material(P):HfO2(25)

Chapter 4

Conclusion

In conclusion, the analysis of the Id-Vg curves for a 2D FinFET transistor reveals the significant impact of various parameters on its electrical characteristics. The variations in parameters such as channel width, doping concentrations, gate work function, dielectric material, and thickness play crucial roles in shaping the transistor's performance.

- Channel Width (CW): As the channel width increases, there is a trend of higher drain current, indicating improved current-carrying capability. However, extremely wide channels may exhibit reduced electrostatic control by the gate.
- Doping Concentrations: Different doping concentrations influence the threshold voltage and subthreshold slope. Steeper slopes and higher drive currents are associated with optimized doping profiles.
- Gate Work Function: Varied gate work functions lead to shifts in threshold voltage. Higher work functions generally result in higher threshold voltages and weaker inversion, impacting the transistor's turn-on characteristics.
- Dielectric Material: The choice of dielectric material, such as Aluminum Oxide (Al2O3) or Hafnium Oxide (HfO2), affects leakage current and gate capacitance. High-k dielectrics contribute to improved gate control and reduced leakage.
- Dielectric Thickness: Thicker dielectrics can lead to higher threshold voltages and increased leakage current. However, optimal thickness choices can balance gate control and leakage, impacting the overall transistor behavior.
- Poly-Silicon Gate Material: The type and work function of the poly-silicon gate material significantly influence the transistor's threshold voltage and subthreshold behavior.

Overall, these variations highlight the intricate trade-offs involved in optimizing FinFET performance. Engineers must carefully select and tune these parameters to achieve desired device characteristics, considering factors like power consumption, speed, and reliability. The analysis of Id-Vg curves provides valuable insights into the impact of these parameters on the FinFET's electrical behavior, aiding in the design and optimization of advanced semiconductor devices.

Chapter 5

Future Prospects

- In the future, we could use TCAD Sentaurus to model new FinFET designs with different fin structures.
- Implement machine learning algorithms to optimize transistor parameters based on desired device characteristics. Use artificial intelligence to efficiently navigate the complex design space and identify configurations that meet specific performance targets.
- Explore the potential of FinFET-like structures for quantum computing applications. Investigate how quantum dots or other quantum phenomena can be harnessed within the FinFET architecture for quantum information processing.
- Focus on enhancing the power efficiency of FinFET transistors, especially for applications demanding low power consumption. Investigate techniques such as power gating, dynamic voltage and frequency scaling, and other energy-saving strategies.

Bibliography

- J. C. Pravin, P. Prajoon, F. P. Nesamania, G. Srikesh, P. S. Kumar and D. Nirmal, "Nanoscale High-k Dielectrics for Junctionless Nanowire Transistor for Drain Current Analysis", Journal of Electronic Materials, vol. 47, no. 5, pp. 2679-2686, 2018.
- J. C. Pravin, D. Nirmal, P. Prajoon and J. Ajayan, "Implementation of nanoscale circuits using dual metal gate engineered nanowire MOSFET with high-k dielectrics for low power applications. Physica E: Low-dimensional Systems and Nanostructures", vol. 83, pp. 95-100, 2016.
- P. M. Solomon, K. W. Guarini, Y. Zhang et al., "Two gates are better than one", IEEE Circuits and Devices Magazine, vol. 19, no. 1, pp. 48-62, 2003.
- Digh Hisamoto, Member, IEEE, Wen-Chin Lee, Jakub Kedzierski, Hideki Takeuchi, Kazuya Asano, Member, IEEE, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, Fellow, IEEE, and Chenming Hu, Fellow, IEEE "FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Transactions on Electron Devices, VOL. 47, NO. 12, December 2000