VLSI Report – Batch 1
Energy Dissipation Analysis in Sequential Circuits using QCA and QCA Pro

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Abstract: This paper represents energy dissipation analysis for SR latch ,D latch ,D flip flop and novel design of SR latch ,D latch flip flop. Basically, in this paper, the part we are going to concentrate on is sequential circuits such as SR Latch and D Latch. We will show the energy dissipation analysis of SR Latch and D Latch. After performing all the simulations we came to an analysis that SR Latch implemented with 72 QCA cells and the delay or latency between input and output is 2 clock cycles and we have reduced to 34 cells with latency of 0.75 clock cycles. Same, after performing the simulations for D Latch, we observe that it is implemented with 29 QCA cells, and the delay or latency between input and output is 1 clock cycle we have reduced to 24 cells and 0.75 clock cycle.

Introduction:

1)The First sequential circuit was D latch we have implemented the with using the 2*1 mux with 24 qca cells and output is 0.75 clock cycle latency and we have performed the heat dissipation analysis for this circuit and by using the QCA Designer E we have found the Total energy dissipation and Average energy dissipation per cycle for different temperatures such as 2k,5k,10k and we have plot the graphs for total energy dissipation.

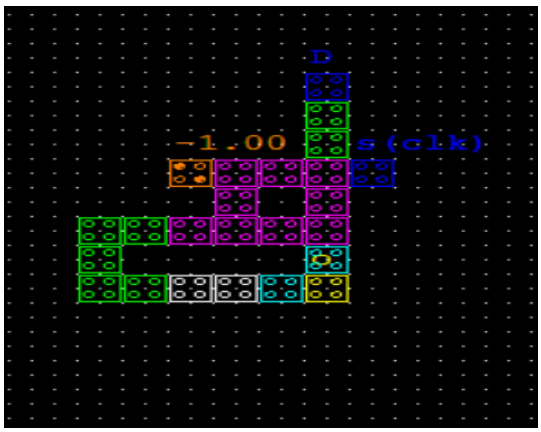

Fig: D latch

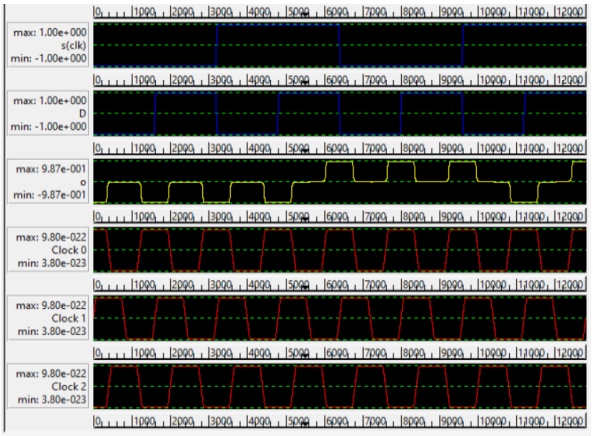

Fig: Output of D latch.

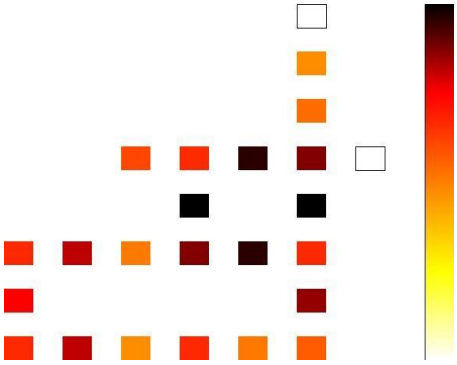

Fig: Thermal Energy Dissipation Analysis of D Latch using QCA Pro

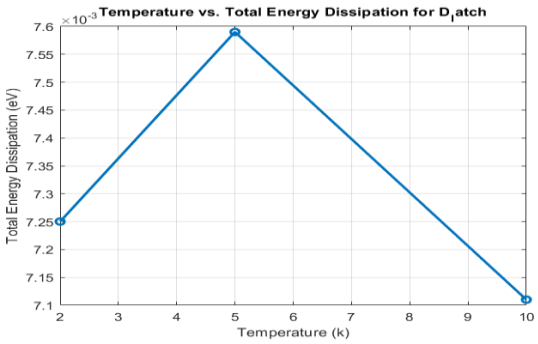

Fig: Total Energy Dissipation vs temperature

2) The Second sequential circuit was SR latch we have implemented the with using the majority gate and not gate with 33 qca cells and output is 0.50 clock cycle latency and we have performed the heat dissipation analysis for this circuit and by using the QCA Designer E we have found the Total energy dissipation and Average energy dissipation per cycle for different temperatures such as 2k,5k,10k and we have plot the graphs for total energy dissipation.

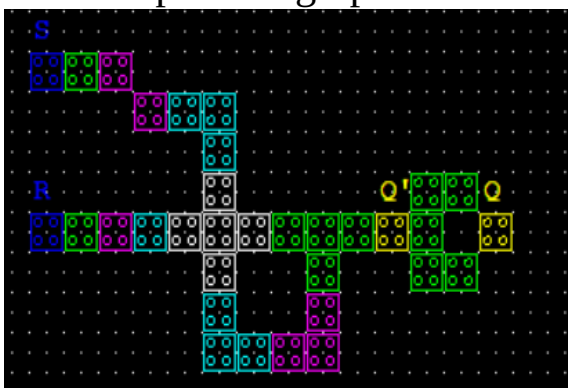

Fig: SR latch

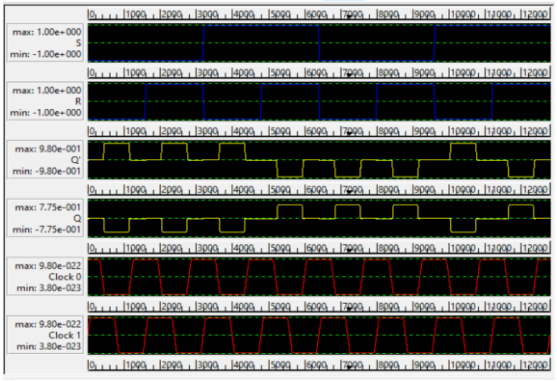

Fig: Output of SR latch

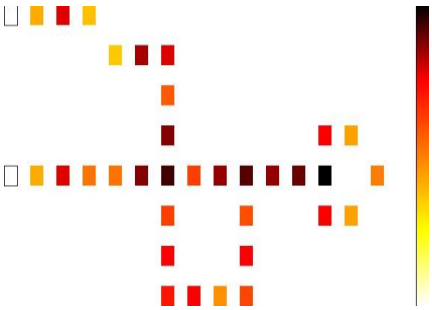

Fig: Thermal Energy Dissipation Analysis of SR Latch using QCA Pro

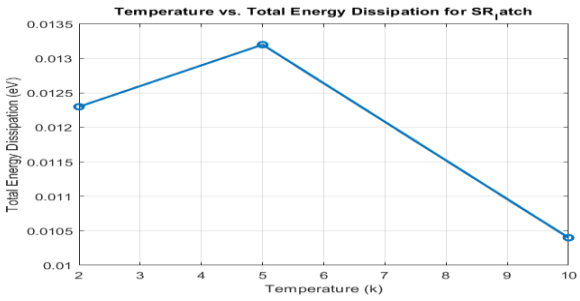

Fig: Total Energy Dissipation vs temperature

3) The Third sequential circuit was D Flip flop we have implemented the with using the with gates such as AND ,OR and NOT gate with 57 qca cells and output is 1 clock cycle latency and we have performed the heat dissipation analysis for this circuit and by using the QCA Designer E we have found the Total energy dissipation and Average energy dissipation per cycle for different temperatures such as 2k,5k,10k and we have plot the graphs for total energy dissipation.

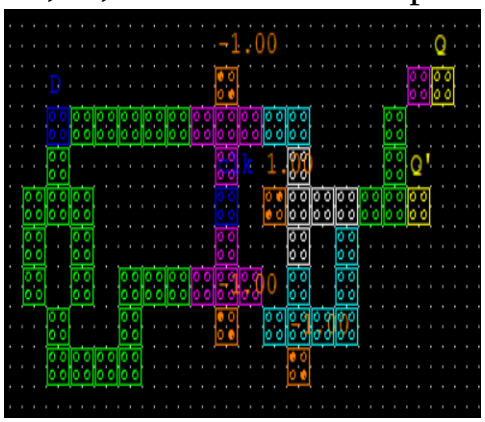

Fig: D flip flop

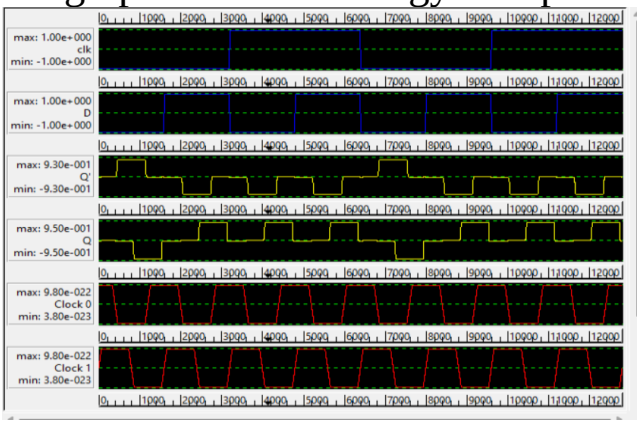

Fig : Output of D flip flop

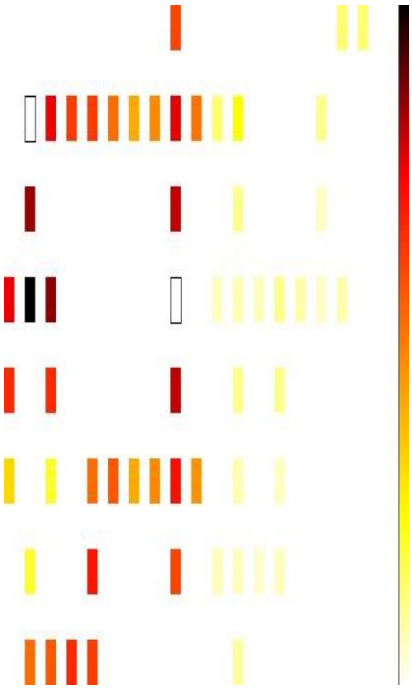

Fig: Thermal Energy Dissipation Analysis of D flip flop using QCA Pro

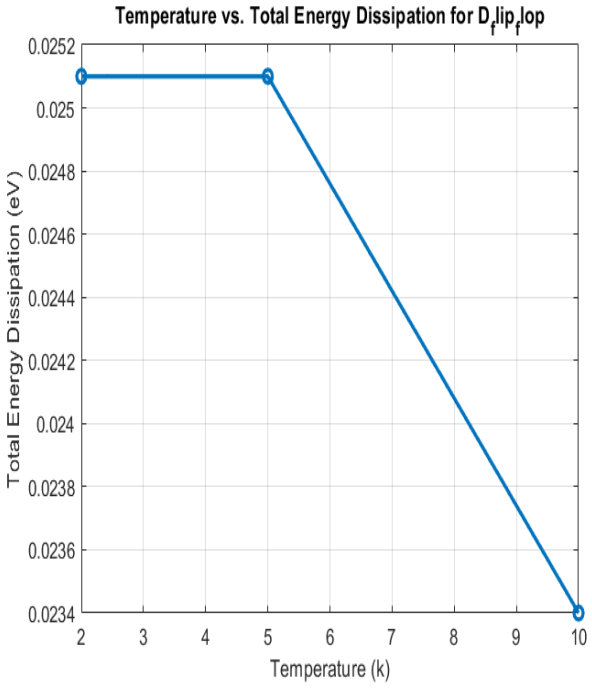

Fig: Total Energy Dissipation vs temperature

4) The Fourth sequential circuit was Positive edged D flip flop we have implemented the with using the 2*1 mux with 24 qca cells and output is 0.75 clock cycle latency and we have performed the heat dissipation analysis for this circuit and by using the QCA Designer E we have found the Total energy dissipation and Average energy dissipation per cycle for different temperatures such as 2k,5k,10k and we have plot the graphs for total energy dissipation.

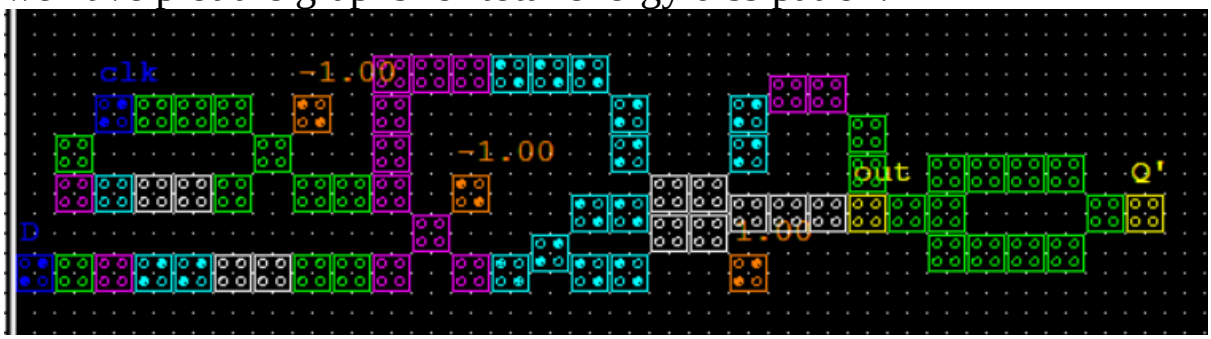

Fig: Positive edged D flip flop

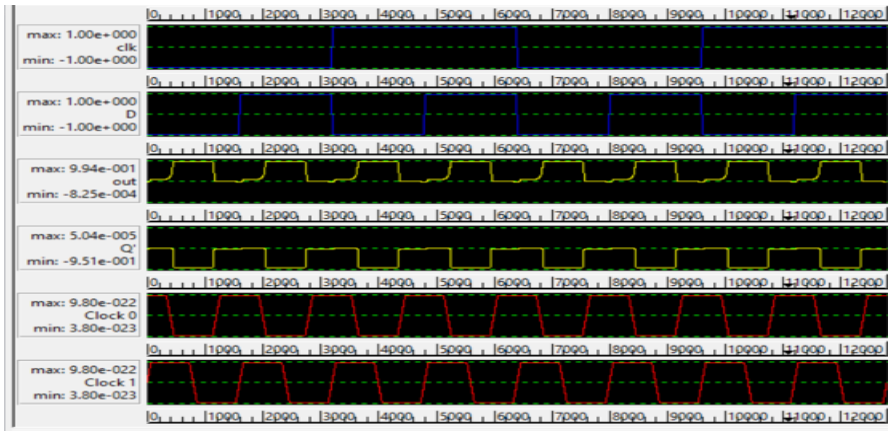

Fig: Output for Positive edged D flip flop.

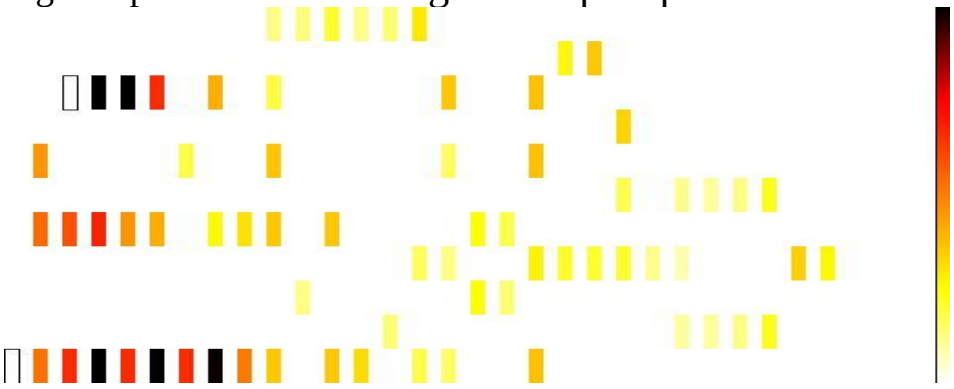

Fig: Thermal Energy Dissipation Analysis of Positive edged D flip flop using QCA Pro

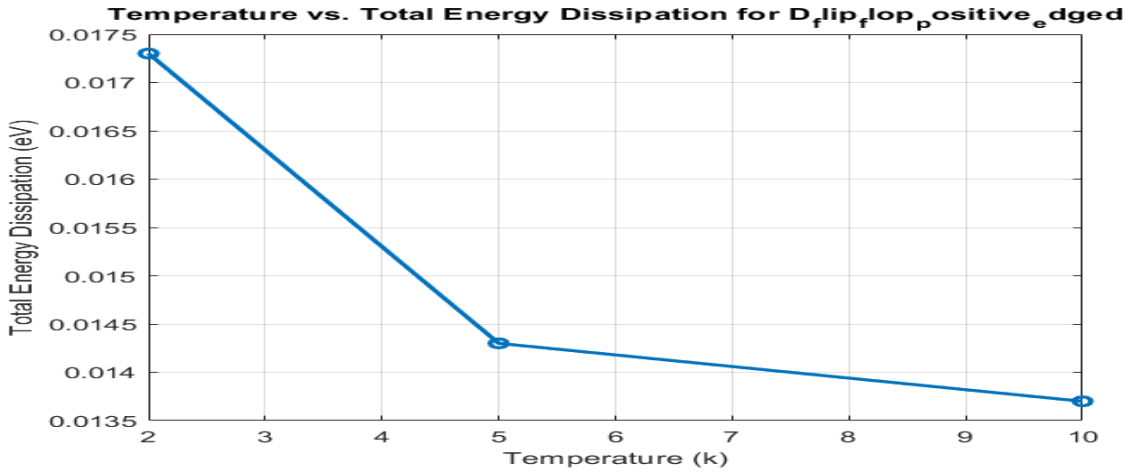

Fig: Total Energy Dissipation vs temperature

Contributions:

- **YALAKANTI Eswar(S20210020332):**

  Modified and design the new D latch, SR latch, D flip flop with a smaller number of cells and also reduced the latency for D latch and SR latch and reduced the power consumption of the circuits and reduced the area and designing the switching set and vector set for Pro tool.

- **Gedda Shyam(S20210020274):**

  Energy Dissipation and Power dissipation for modified circuit using the QCA Pro and QCA Designer E and also plot the graph for Total Energy Dissipation and Average energy dissipation per cycle and plotted the graph using the MATLAB.