ESWIN

EBC77 Series Development Board Datasheet

EIC7702X SoC

Rev1.5
2025-10-11

Overview

The EBC7702 development board platform consists of SOM board and Carrier board. The SOM board includes the smallest systems such as EIC7702X, LPDDR SDRAM, EMMC, EPHY, Power IC, and Reset IC. The carrier board includes rich expansion interfaces and power supply systems.

The SOM board dimensions are 85X85mm. The Carrier board platform supports the Mini-DTX size (170X203mm) specification and can be installed in a 1U chassis.

The EIC7702X chip is a low-power, high-performance AI SoC designed for edge computing applications, fabricated using TSMC's 12nm FFC process. This SoC integrates a CPU that supports the RISC-V instruction set. The chip's NPU delivers up to 2x19.95 TOPS INT8 computing power; it supports LPDDR4X/LPDDR5 with a data transfer speed of 6400 Mbps and a memory bandwidth of 64GB 128bit, achieving high utilization (80%+). For codecs, it enables 8K@100fps decoding and 8K@50fps encoding.

The EIC7702X SOM core board integrates 2x16MB SPI flash, 4x8GB LPDDR4X/LPDDR5 SDRAM, 32GB eMMC, and 4x140-pin board-to-board connectors. These connectors expose the core chip's resources, enabling the expansion of peripherals such as network UART, I2C, SPI, HDMI, SD SATA, USB, EEPROM, CSI, DSI, PCIe, Wi-Fi, and Bluetooth.

Product Application

- Security monitoring
- Education
- AI computing
- Medical Electronics
- Big data
- Video advertising

Product Features

- CPU RISC-V RV64GC 8 core, supports cache consistency, clock frequency up to 1.8GHz
- SDRAM capacity

  32GB/64GB LPDDR5@6400Mbps
- DNN Accelerator: The chip has a computing power of up to 40 TOPS INT8, 20 TPS INT16, and 20 TFLOPS FP16
- Vision DSP multi-core DSP dual cluster 1040MHz
- Video encoding supports up to 8K@50fps Or Route 26 1080P@30fps
- Video decoding supports up to 8K@100fps Or route 64 1080P@30fps
- JPEG codec JPEG ISO/IEC 10918-1, ITU-T T.81
- Vision Engine 2 x HAE (2D Blit, Crop, Resize, Normalization)
- GPU 2 x 3D GPU (supports OpenGL ES 3.2, EGL 1.4, OpenCL 1.2/2.1 EP2, Vulkan 1.2, Android NN HAL)
- Display system 2 x OSD (3 image layers, namely video layer, mouse layer, and background layer)
- 2X16MB SPI flash
- 32GB EMMC
- Four 140 pin board to board connectors
- Working environment temperature: -20~50 ℃
- The core board size is 85X85mm, and the bottom board size is 203.2X170.18mm

Statement

ESWIN is not obligated to notify any modifications to this document and does not represent any commitment from ESWIN. Unless otherwise stated, all statements, information, and recommendations in this document are provided "as is" and ESWIN makes no warranties, guarantees, or commitments of any kind, express or implied, with respect to them. (This paragraph is used in the document)

Revision History

version	date	Instructions
V1.5	2025.10.11	Format modification
V1.4	2025.9.30	EBC7702 Development Board Manual Update
V1.3	2025.9.28	EBC7702 Manual
V1.2	2025.4.22	SOM Core Edition Manual
V1.0	2025.2.28	The initial draft of the EIC7702X SOM core board data manual has been completed.

Content

Content of Tables

Content of Figures

1. System Overview

The product appearance is shown in the following picture:

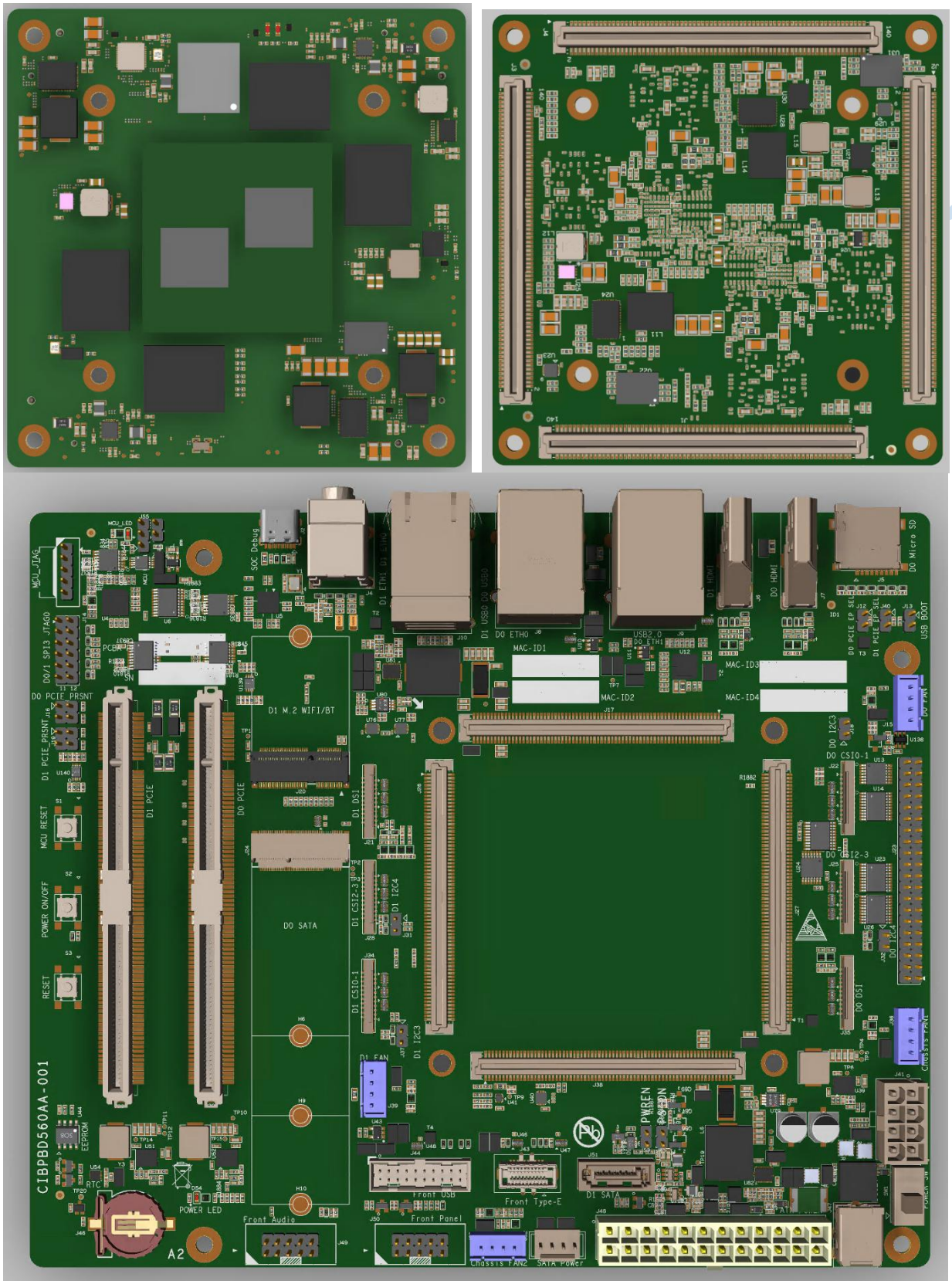

Figure 1-1 EIC7702X SOM Appearance of core board and bottom board

1.1 EIC7702X Chip Block Diagram

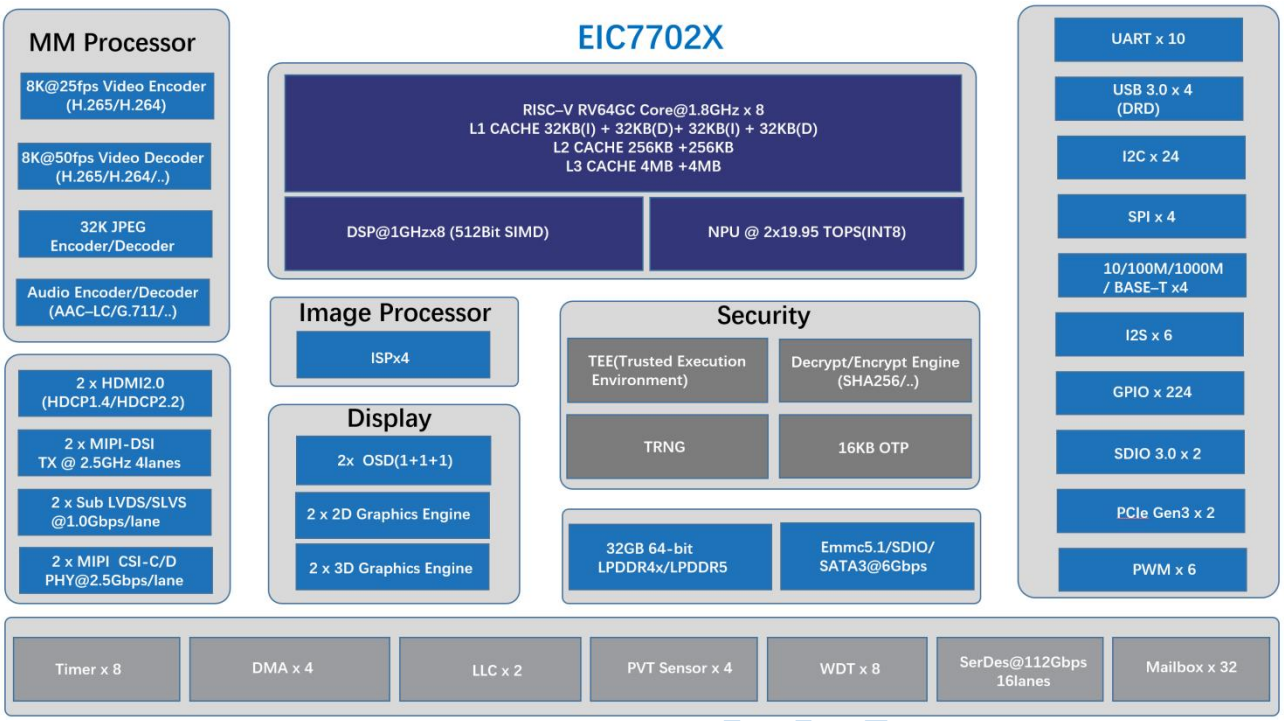

Figure 1-2 EIC7702X block diagram

1.2 EIC7702X Interface resource allocation

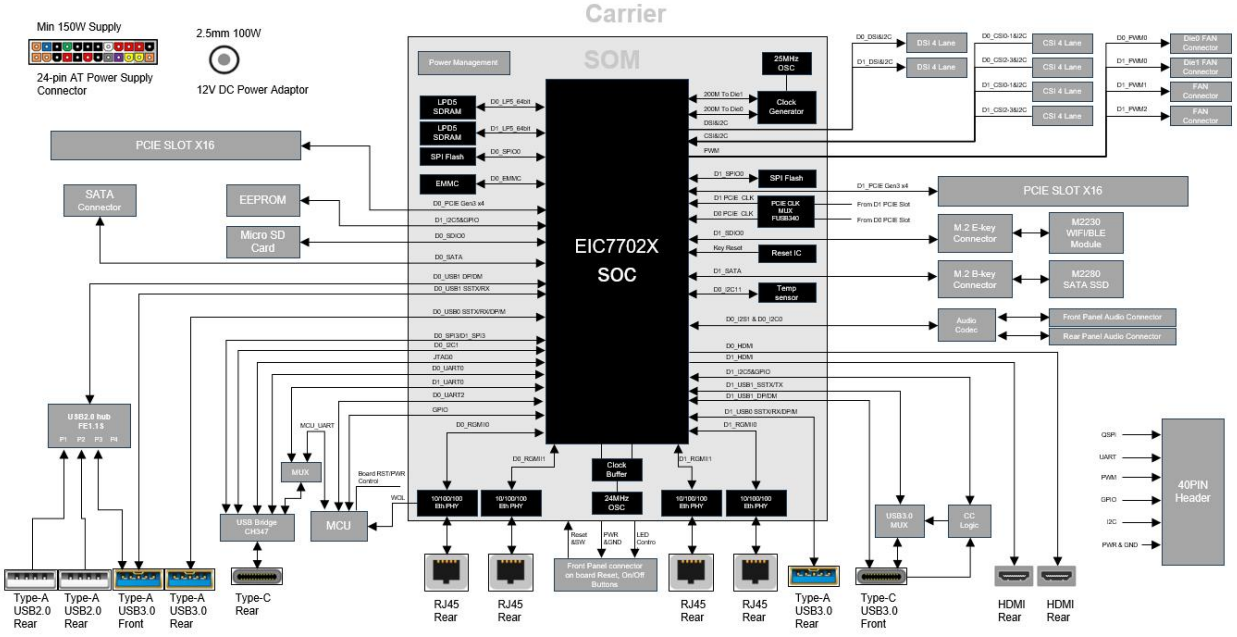

Figure 1-3 EIC7702X SOM Interface allocation diagram

1.3 hardware features

Table 1-1-1 Hardware characteristic parameters

Item	EIC7702X SOM
CPU	RISC-V RV64GC 8 core, supporting cache consistency Clock frequency up to 1.8GHz L1 Cache 64KB(I) + 64KB(D) （private） L2 Cache 512KB（private） L3 Cache 8MB（private） Cache supports ECC (supports SECDED)
DNN Accelerator	40TOPS (INT8) 20TOPS (FP16 or INT16)
Vision DSP	Multi core DSP dual cluster 1040MHz, supporting 512 bit SIMD and single cycle 512 INT8 MAC operations
Memory	4X8GB LPDDR4X/LPDDR5 SDRAM, Operating frequency up to 4266MHz/6400MHz
external storage	32GB EMMC5.1 2X16MB SPI flash
RAS	SRAM DDR supports parity check and ECC
video encoding	Video encoding supports up to 8K@50fps Or Route 26 1080P@30fps H.265 (HEVC)： ITU-T Rec. H.265 (04/2013), ISO/IEC 23008-2 Main Profile, Level 5.1, High Tier Main10 profile, Level 5.1, High Tier Main Still Profile H.264 (AVC)： Spec Version 12:ISO/IEC 14496-10 / ITU-T Rec. H.264 (03/2010) Baseline Profile, levels 1 - 5.2 Main Profile, levels 1 - 5.2 High Profile, levels 1 - 5.2 High 10 Profile, levels 1 - 5.2

video decoding	Video decoding supports up to 8K@100fps Or route 64 1080P@30fps H.265 (HEVC): ITU-T Rec. H.265 (04/2013), ISO/IEC 23008-2 Main Profile, up to Level 5.1, High Tier Main10 profile, up to Level 5.1, High Tier Main Profile, Level 6, High Tier Main10 profile, Level 6, High Tier Main Still Profile H.264 (AVC): Spec Version 12:ISO/IEC 14496-10 / ITU-T Rec. H.264 (03/2010) Baseline Profile, Levels 1 – 5.2 (up to 4K) Main Profile, Levels 1 – 5.2 (up to 4K) High Profile, Levels 1 – 5.2 (up to 4K) Constrained Baseline, levels 1 – 5.2 (up to 4K) Progressive High profile, levels 1 – 5.2 (up to 4K) High 10 profile (progressive only), levels 1 – 5.2 (up to 4K) High 10 Intra profile (progressive only), levels 1 – 5.2 (up to 4K) Constrained Baseline, level 6 (up to 8K) Progressive High profile, level 6 (up to 8K) High 10 profile (progressive only), level 6 (up to 8K) High 10 Intra profile (progressive only), level 6 (up to 8K)
JPEG codec	JPEG ISO/IEC 10918-1, ITU-T T.81. Supports a maximum resolution of 32K x 32K Baseline process (Internal support Huffman coding Interleaved YUV420, YUV422，Monochrome) Lossless process (Internal support 8-bit with Huffman coding Interleaved YUV420，Monochrome) MJPEG format (T.81 Annex H) in AVI container
Vision Engine	2 x HAE (2D Blit, Crop, Resize, Normalization)
GPU	2 x 3D GPU (OpenGL-ES 3.2、EGL 1.4、OpenCL 1.2/2.1 EP2、Vulkan 1.2、Android NN HAL)
display system	2 x OSD (3 image layers, namely video layer, mouse layer, and background layer)
Temperature detection	Integrate 1 temperature sensor
DIE2DIE	Bidirectional 8x lanes 56Gbps per lane
LLC	2 x 4MB (128Bytes cache line，16 ways associativity) ECC（support SECDED）
safety	TEE (Trusted Execution Environment)，TRNG， ECDSA RSA4096，AES，SM4，DES，HMAC(MD5,SHA-1,SHA-224.SHA256,SM-3,SHA512/224,SHA-512/256,SHA-384),CRC32, Dual core hardware acceleration 32KB OTP 2 x RV32I single core L1 CACHE 64KB (I)+64KB (D)

2. SOM Interface description

2.1 Define Interface Section

Table 2-1 J1 Interface Definition

D0_GPIO0	1	2	D0_I2C0_SDA/GPIO45
D0_GPIO92/I2C8_SCL/UART3_TX	3	4	D0_I2C0_SCL/GPIO44
D0_GPIO93/I2C8_SDA/UART3_RX	5	6	D0_SPI2_CS1_N/GPIO12
D0_GPIO28	7	8	D0_SPI2_CS0_N/GPIO6
D0_GPIO27/SATA_ACT_LED	9	10	D0_GPIO5/SPI2_D3

GND	11	12	GND
D0_SPI1_CS0_N/GPIO35	13	14	D0_JTAG0_TDI/SPI2_D1/GPIO3
D0_SPI1_CLK/GPIO36	15	16	D0_JTAG0_TMS/SPI2_D0/GPIO2
D0_SPI1_D0/I2C9_SCL/GPIO37/UART4_TX	17	18	D0_JTAG0_TCK/SPI2_CLK/GPIO1
D0_SPI1_D1/I2C9_SDA/GPIO38/UART4_RX	19	20	D0_JTAG0_TDO/SPI2_D2/GPIO4
D0_SPI1_D2/GPIO39	21	22	GND
D0_SPI1_D3/PWM1/GPIO40	23	24	D0_SDIO0_D3
D0_SPI1_CS1_N/PWM2/GPIO41	25	26	D0_SDIO0_D2
GND	27	28	D0_SDIO0_CMD
D0_SD0_CD/GPIO13	29	30	GND
D0_GPIO14	31	32	D0_SDIO0_CLK
D0_SPI3_CS_N/GPIO88	33	34	D0_SDIO0_D1
D0_SPI3_CLK/GPIO89	35	36	D0_SDIO0_D0
D0_SPI3_MOSI/GPIO90	37	38	GND
D0_SPI3_MISO/GPIO91	39	40	D0_UART2_RX/I2C7_SDA/GPIO63
GND	41	42	D0_UART2_TX/I2C7_SCL/GPIO62
D0_I2C1_SCL/GPIO46	43	44	D0_UART1_RTS/I2C6_SDA/GPIO61
D0_I2C1_SDA/GPIO47	45	46	D0_UART1_CTS/I2C6_SCL/GPIO60
D0_I2C10_SCL/GPIO102	47	48	D0_UART1_RX/GPIO_59
D0_I2C10_SDA/GPIO103	49	50	D0_UART1_TX/GPIO_58
D0_USB1_PWREN	51	52	D0_UART0_RX
GND	53	54	D0_UART0_TX
D0_USB1_SSTX_P	55	56	D0_USB0_PWREN
D0_USB1_SSTX_M	57	58	GND
GND	59	60	D0_USB1_DP
D0_USB1_SSRX_P	61	62	D0_USB1_DM
D0_USB1_SSRX_M	63	64	GND
GND	65	66	D0_USB0_DP
D0_USB0_SSTX_P	67	68	D0_USB0_DM
D0_USB0_SSTX_M	69	70	GND
GND	71	72	D0_SATA_TXP
D0_USB0_SSRX_P	73	74	D0_SATA_TXM
D0_USB0_SSRX_M	75	76	GND
GND	77	78	D0_SATA_RXM
D0_EPHY0_MDI0+	79	80	D0_SATA_RXP
D0_EPHY0_MDI0-	81	82	GND
GND	83	84	D0_EPHY1_MDI3-
D0_EPHY0_MDI1+	85	86	D0_EPHY1_MDI3+
D0_EPHY0_MDI1-	87	88	GND
GND	89	90	D0_EPHY1_MDI2-
D0_EPHY0_MDI2+	91	92	D0_EPHY1_MDI2+
D0_EPHY0_MDI2-	93	94	GND
GND	95	96	D0_EPHY1_MDI1-
D0_EPHY0_MDI3+	97	98	D0_EPHY1_MDI1+
D0_EPHY0_MDI3-	99	100	GND
GND	101	102	D0_EPHY1_MDI0-
D0_EPHY0_LED2	103	104	D0_EPHY1_MDI0+
D0_EPHY0_LED1	105	106	GND
D0_RGMII0_WOL	107	108	D0_EPHY1_LED2
5VSB	109	110	D0_EPHY1_LED1

GND	111	112	GND
GND	113	114	GND
GND	115	116	GND
GND	117	118	GND
GND	119	120	GND
GND	121	122	GND
GND	123	124	GND
VCC5V	125	126	VCC5V
VCC5V	127	128	VCC5V
VCC5V	129	130	VCC5V
VCC5V	131	132	VCC5V
VCC5V	133	134	VCC5V
VCC5V	135	136	VCC5V
VCC5V	137	138	VCC5V
VCC5V	139	140	VCC5V

Table 2-2 J2 Interface Definition

GND	1	2	GND
D0_PCIE_SLOT_CLKN	3	4	D0_HDMI_TXCKN
D0_PCIE_SLOT_CLKP	5	6	D0_HDMI_TXCKP
GND	7	8	GND
D0_PCIE_RX0N	9	10	D0_HDMI_TX0N
D0_PCIE_RX0P	11	12	D0_HDMI_TX0P
GND	13	14	GND
D0_PCIE_RX1N	15	16	D0_HDMI_TX1N
D0_PCIE_RX1P	17	18	D0_HDMI_TX1P
GND	19	20	GND
D0_PCIE_RX2N	21	22	D0_HDMI_TX2N
D0_PCIE_RX2P	23	24	D0_HDMI_TX2P
GND	25	26	GND
D0_PCIE_RX3N	27	28	D0_HDMI_SDA
D0_PCIE_RX3P	29	30	D0_HDMI_SCL
GND	31	32	D0_HDMI_CEC
D0_PCIE_TX0N	33	34	D0_HDMI_HPD
D0_PCIE_TX0P	35	36	D0_PCIE_CLKREQ_N
GND	37	38	D0_PCIE_PERST_N
D0_PCIE_TX1N	39	40	D0_PCIE_WAKE_N
D0_PCIE_TX1P	41	42	GND
GND	43	44	D0_MIPI_DSI_D0P
D0_PCIE_TX2N	45	46	D0_MIPI_DSI_D0N
D0_PCIE_TX2P	47	48	GND
GND	49	50	D0_MIPI_DSI_D1P
D0_PCIE_TX3N	51	52	D0_MIPI_DSI_D1N
D0_PCIE_TX3P	53	54	GND
GND	55	56	D0_MIPI_DSI_CKP
D0_MIPI_CSI2_D0N	57	58	D0_MIPI_DSI_CKN
D0_MIPI_CSI2_D0P	59	60	GND
GND	61	62	D0_MIPI_DSI_D2P
D0_MIPI_CSI2_D1N	63	64	D0_MIPI_DSI_D2N

D0_MIPI_CSI2_D1P	65	66	GND
GND	67	68	D0_MIPI_DSI_D3P
D0_MIPI_CSI2_CKN	69	70	D0_MIPI_DSI_D3N
D0_MIPI_CSI2_CKP	71	72	GND
GND	73	74	D0_MIPI_CSI1_D1P
D0_MIPI_CSI3_D0N	75	76	D0_MIPI_CSI1_D1N
D0_MIPI_CSI3_D0P	77	78	GND
GND	79	80	D0_MIPI_CSI1_D0P
D0_MIPI_CSI3_CKN	81	82	D0_MIPI_CSI1_D0N
D0_MIPI_CSI3_CKP	83	84	GND
GND	85	86	D0_MIPI_CSI0_CKP
D0_MIPI_CSI3_D1N	87	88	D0_MIPI_CSI0_CKN
D0_MIPI_CSI3_D1P	89	90	GND
GND	91	92	D0_MIPI_CSI0_D1P
D0_MIPI_CSI1_CKN	93	94	D0_MIPI_CSI0_D1N
D0_MIPI_CSI1_CKP	95	96	GND
GND	97	98	D0_MIPI_CSI0_D0P
D0_I2S_MCLK/GPIO22	99	100	D0_MIPI_CSI0_D0N
D0_I2S2_BCLK/GPIO23	101	102	GND
D0_I2S2_WCLK/GPIO24	103	104	D0_MIPI_CSI3_MCLK/GPIO81
D0_I2S2_SDI/GPIO25	105	106	D0_MIPI_CSI3_XHS/GPIO80
D0_I2S2_SDO/GPIO26	107	108	D0_MIPI_CSI3_XVS/GPIO79
D0_I2S1_BCLK/GPIO30	109	110	D0_MIPI_CSI2_MCLK/GPIO78
D0_I2S1_WCLK/GPIO31	111	112	D0_MIPI_CSI2_XHS/GPIO77
D0_I2S1_SDI/GPIO32	113	114	D0_MIPI_CSI2_XVS/GPIO76
D0_I2S1_SDO/GPIO33	115	116	GND
GND	117	118	D0_MIPI_CSI1_XHS/GPIO74
D0_I2C2_SCL/GPIO48	119	120	D0_MIPI_CSI1_MCLK/GPIO75
D0_I2C2_SDA/GPIO49	121	122	D0_MIPI_CSI1_XVS/GPIO73
D0_I2C3_SCL/GPIO50	123	124	D0_MIPI_CSI0_MCLK/GPIO72
D0_I2C3_SDA/GPIO51	125	126	D0_MIPI_CSI0_XHS/GPIO71
D0_I2C4_SCL/GPIO52	127	128	D0_MIPI_CSI0_XVS/GPIO70
D0_I2C4_SDA/GPIO53	129	130	GND
D0_I2C5_SCL/GPIO54	131	132	D0_GPIO18
D0_I2C5_SDA/GPIO55	133	134	D0_GPIO19
GND	135	136	CARRIER_PWR_EN
D0_FAN_PWM/GPIO68	137	138	BOOT_SEL0
D0_FAN_TACH/GPIO69	139	140	-

Table 2-3 J3 Interface Definition

GND	1	2	GND
D1_PCIE_SLOT_CLKN	3	4	D1_HDMI_TXCKN
D1_PCIE_SLOT_CLKP	5	6	D1_HDMI_TXCKP
GND	7	8	GND
D1_PCIE_RX0N	9	10	D1_HDMI_TX0N
D1_PCIE_RX0P	11	12	D1_HDMI_TX0P
GND	13	14	GND
D1_PCIE_RX1N	15	16	D1_HDMI_TX1N
D1_PCIE_RX1P	17	18	D1_HDMI_TX1P

GND	19	20	GND
D1_PCIE_RX2N	21	22	D1_HDMI_TX2N
D1_PCIE_RX2P	23	24	D1_HDMI_TX2P
GND	25	26	GND
D1_PCIE_RX3N	27	28	D1_HDMI_SDA
D1_PCIE_RX3P	29	30	D1_HDMI_SCL
GND	31	32	D1_HDMI_CEC
D1_PCIE_TX0N	33	34	D1_HDMI_HPD
D1_PCIE_TX0P	35	36	D1_PCIE_CLKREQ_N
GND	37	38	D1_PCIE_PERST_N
D1_PCIE_TX1N	39	40	D1_PCIE_WAKE_N
D1_PCIE_TX1P	41	42	GND
GND	43	44	D1_MIPI_DSI_D0P
D1_PCIE_TX2N	45	46	D1_MIPI_DSI_D0N
D1_PCIE_TX2P	47	48	GND
GND	49	50	D1_MIPI_DSI_D1P
D1_PCIE_TX3N	51	52	D1_MIPI_DSI_D1N
D1_PCIE_TX3P	53	54	GND
GND	55	56	D1_MIPI_DSI_CKP
D1_MIPI_CSI2_D0N	57	58	D1_MIPI_DSI_CKN
D1_MIPI_CSI2_D0P	59	60	GND
GND	61	62	D1_MIPI_DSI_D2P
D1_MIPI_CSI2_D1N	63	64	D1_MIPI_DSI_D2N
D1_MIPI_CSI2_D1P	65	66	GND
GND	67	68	D1_MIPI_DSI_D3P
D1_MIPI_CSI2_CKN	69	70	D1_MIPI_DSI_D3N
D1_MIPI_CSI2_CKP	71	72	GND
GND	73	74	D1_MIPI_CSI1_D1P
D1_MIPI_CSI3_D0N	75	76	D1_MIPI_CSI1_D1N
D1_MIPI_CSI3_D0P	77	78	GND
GND	79	80	D1_MIPI_CSI1_D0P
D1_MIPI_CSI3_CKN	81	82	D1_MIPI_CSI1_D0N
D1_MIPI_CSI3_CKP	83	84	GND
GND	85	86	D1_MIPI_CSI0_CKP
D1_MIPI_CSI3_D1N	87	88	D1_MIPI_CSI0_CKN
D1_MIPI_CSI3_D1P	89	90	GND
GND	91	92	D1_MIPI_CSI0_D1P
D1_MIPI_CSI1_CKN	93	94	D1_MIPI_CSI0_D1N
D1_MIPI_CSI1_CKP	95	96	GND
GND	97	98	D1_MIPI_CSI0_D0P
D1_I2S_MCLK/GPIO22	99	100	D1_MIPI_CSI0_D0N
D1_I2S2_BCLK/GPIO23	101	102	GND
D1_I2S2_WCLK/GPIO24	103	104	D1_MIPI_CSI3_MCLK/GPIO81
D1_I2S2_SDI/GPIO25	105	106	D1_MIPI_CSI3_XHS/GPIO80
D1_I2S2_SDO/GPIO26	107	108	D1_MIPI_CSI3_XVS/GPIO79
D1_I2S1_BCLK/GPIO30	109	110	D1_MIPI_CSI2_MCLK/GPIO78
D1_I2S1_WCLK/GPIO31	111	112	D1_MIPI_CSI2_XHS/GPIO77
D1_I2S1_SDI/GPIO32	113	114	D1_MIPI_CSI2_XVS/GPIO76
D1_I2S1_SDO/GPIO33	115	116	GND
GND	117	118	D1_MIPI_CSI1_XHS/GPIO74

D1_I2C2_SCL/GPIO48	119	120	D1_MIPI_CSI1_MCLK/GPIO75
D1_I2C2_SDA/GPIO49	121	122	D1_MIPI_CSI1_XVS/GPIO73
D1_I2C3_SCL/GPIO50	123	124	D1_MIPI_CSI0_MCLK/GPIO72
D1_I2C3_SDA/GPIO51	125	126	D1_MIPI_CSI0_XHS/GPIO71
D1_I2C4_SCL/GPIO52	127	128	D1_MIPI_CSI0_XVS/GPIO70
D1_I2C4_SDA/GPIO53	129	130	GND
D1_I2C5_SCL/GPIO54	131	132	D1_GPIO18
D1_I2C5_SDA/GPIO55	133	134	D1_GPIO19
GND	135	136	D1_GPIO20
D1_FAN_PWM/GPIO68	137	138	D1_GPIO21
D1_FAN_TACH/GPIO69	139	140	-

Table 2-4 J4 Interface Definition

D1_GPIO0	1	2	D1_I2C0_SDA/GPIO45
D1_GPIO92/I2C8_SCL/UART3_TX	3	4	D1_I2C0_SCL/GPIO44
D1_GPIO93/I2C8_SDA/UART3_RX	5	6	D1_SPI2_CS1_N/GPIO12
D1_GPIO28	7	8	D1_SPI2_CS0_N/GPIO6
D1_GPIO27/SATA_ACT_LED	9	10	D1_GPIO5/SPI2_D3
GND	11	12	GND
D1_SPI1_CS0_N/GPIO35	13	14	D1_JTAG0_TDI/SPI2_D1/GPIO3
D1_SPI1_CLK/GPIO36	15	16	D1_JTAG0_TMS/SPI2_D0/GPIO2
D1_SPI1_D0/I2C9_SCL/GPIO37/UART4_TX	17	18	D1_JTAG0_TCK/SPI2_CLK/GPIO1
D1_SPI1_D1/I2C9_SDA/GPIO38/UART4_RX	19	20	D1_JTAG0_TDO/SPI2_D2/GPIO4
D1_SPI1_D2/GPIO39	21	22	GND
D1_SPI1_D3/PWM1/GPIO40	23	24	D1_SDIO0_D3
D1_SPI1_CS1_N/PWM2/GPIO41	25	26	D1_SDIO0_D2
GND	27	28	D1_SDIO0_CMD
D1_SD0_CD/GPIO13	29	30	GND
D1_GPIO14	31	32	D1_SDIO0_CLK
D1_SPI3_CS_N/GPIO88	33	34	D1_SDIO0_D1
D1_SPI3_CLK/GPIO89	35	36	D1_SDIO0_D0
D1_SPI3_MOSI/GPIO90	37	38	GND
D1_SPI3_MISO/GPIO91	39	40	D1_UART2_RX/I2C7_SDA/GPIO63
GND	41	42	D1_UART2_TX/I2C7_SCL/GPIO62
D1_I2C1_SCL/GPIO46	43	44	D1_UART1_RTS/I2C6_SDA/GPIO61
D1_I2C1_SDA/GPIO47	45	46	D1_UART1_CTS/I2C6_SCL/GPIO60
D1_I2C10_SCL/GPIO102	47	48	D1_UART1_RX/GPIO_59
D1_I2C10_SDA/GPIO103	49	50	D1_UART1_TX/GPIO_58
D1_USB1_PWREN	51	52	D1_UART0_RX
GND	53	54	D1_UART0_TX
D1_USB1_SSTX_P	55	56	D1_USB0_PWREN
D1_USB1_SSTX_M	57	58	GND
GND	59	60	D1_USB1_DP
D1_USB1_SSRX_P	61	62	D1_USB1_DM
D1_USB1_SSRX_M	63	64	GND
GND	65	66	D1_USB0_DP
D1_USB0_SSTX_P	67	68	D1_USB0_DM
D1_USB0_SSTX_M	69	70	GND
GND	71	72	D1_SATA_TXP

D1_USB0_SSRX_P	73	74	D1_SATA_TXM
D1_USB0_SSRX_M	75	76	GND
GND	77	78	D1_SATA_RXM
D1_EPHY0_MDI0+	79	80	D1_SATA_RXP
D1_EPHY0_MDI0-	81	82	GND
GND	83	84	D1_EPHY1_MDI3-
D1_EPHY0_MDI1+	85	86	D1_EPHY1_MDI3+
D1_EPHY0_MDI1-	87	88	GND
GND	89	90	D1_EPHY1_MDI2-
D1_EPHY0_MDI2+	91	92	D1_EPHY1_MDI2+
D1_EPHY0_MDI2-	93	94	GND
GND	95	96	D1_EPHY1_MDI1-
D1_EPHY0_MDI3+	97	98	D1_EPHY1_MDI1+
D1_EPHY0_MDI3-	99	100	GND
GND	101	102	D1_EPHY1_MDI0-
D1_EPHY0_LED2	103	104	D1_EPHY1_MDI0+
D1_EPHY0_LED1	105	106	GND
GND	107	108	D1_EPHY1_LED2
MR_RESET	109	110	D1_EPHY1_LED1
GND	111	112	GND
GND	113	114	GND
GND	115	116	GND
GND	117	118	GND
GND	119	120	GND
GND	121	122	GND
GND	123	124	GND
VCC5V	125	126	VCC5V
VCC5V	127	128	VCC5V
VCC5V	129	130	VCC5V
VCC5V	131	132	VCC5V
VCC5V	133	134	VCC5V
VCC5V	135	136	VCC5V
VCC5V	137	138	VCC5V
VCC5V	139	140	VCC5V

2.2 J1/J4 Detailed description of the interface

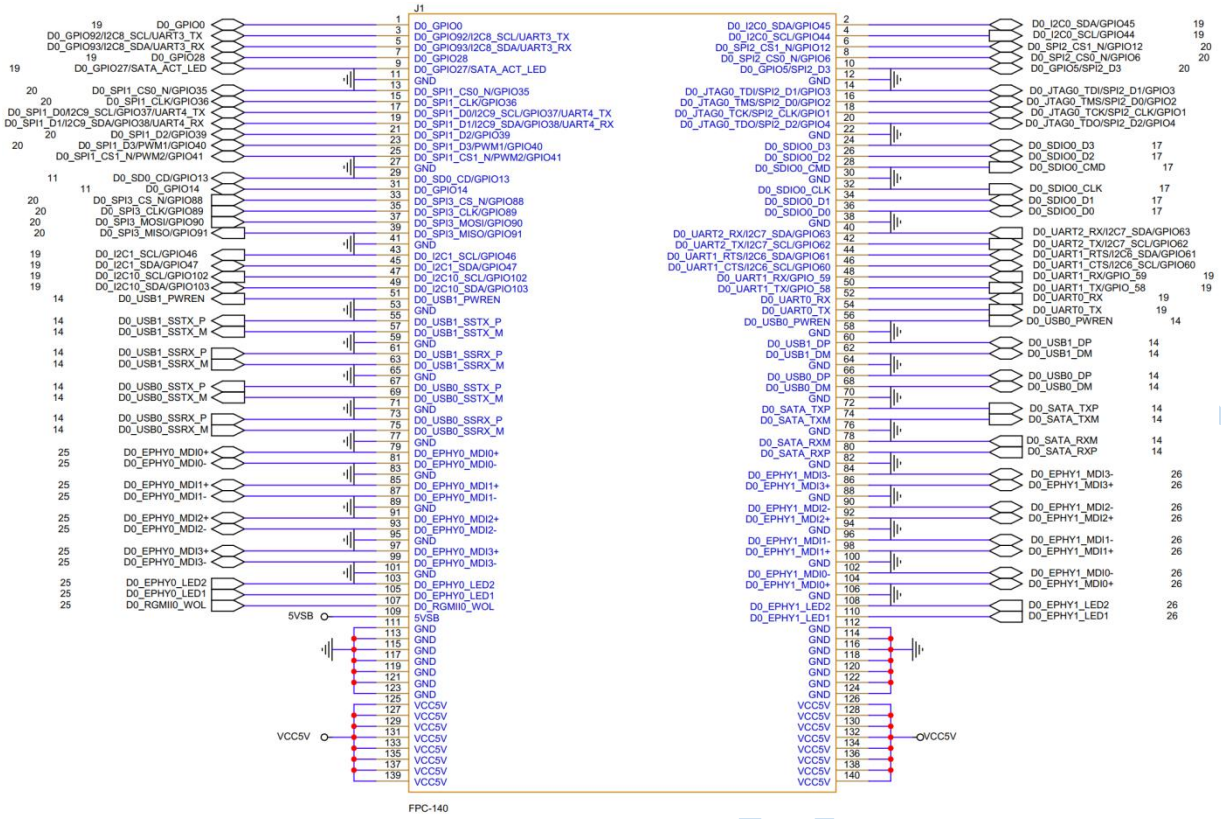

Figure 2-1 J1 Interface schematic diagram

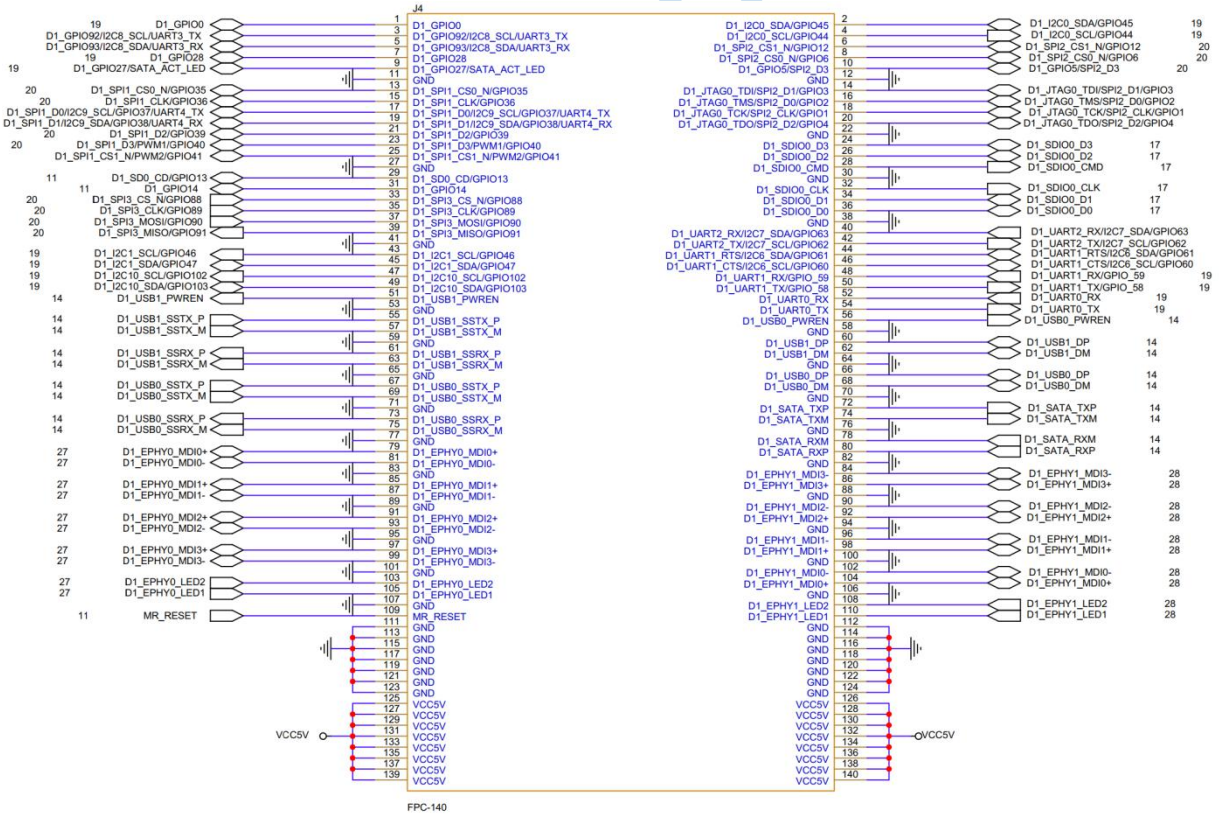

Figure 2-2 J4 Interface schematic diagram

The interface in J1 is basically the same as J4, and the interface in J2 is basically the same as J3. If it is a consistent interface in the following chapters, it will not be repeated.

2.2.1 USB interface description

The J1 interface contains 2 USB 3.0 channels and 2 USB 2.0 channels

Table 2-5 USB Interface description

Signal Name	Description	Type	Power Supply
D0_USB1_PWREN	USB Power enable	O	D0_VDDIO18
D0_USB1_SSTX_P	USB 3.0 SuperSpeed transmitter positive terminal	O	D0_VPTX_USB
D0_USB1_SSTX_M	USB 3.0 SuperSpeed transmitter Lane minus terminal	O	D0_VPTX_USB
D0_USB1_SSRX_P	USB 3.0 SuperSpeed receiver positive terminal	I	D0_VP_USB
D0_USB1_SSRX_M	USB 3.0 SuperSpeed receiver Lane minus terminal	I	D0_VP_USB
D0_USB0_SSTX_P	USB 3.0 SuperSpeed transmitter positive terminal	O	D0_VPTX_USB
D0_USB0_SSTX_M	USB 3.0 SuperSpeed transmitter Lane minus terminal	O	D0_VPTX_USB
D0_USB0_SSRX_P	USB 3.0 SuperSpeed receiver positive terminal	I	D0_VP_USB
D0_USB0_SSRX_M	USB 3.0 SuperSpeed receiver Lane minus terminal	I	D0_VP_USB
D0_USB0_PWREN	USB Power enable	O	D0_VDDIO18
D0_USB1_DP	USB2.0 Data positive	I/O	D0_VDDIO33_USB
D0_USB1_DM	USB2.0 Data minus	I/O	D0_VDDIO33_USB
D0_USB0_DP	USB2.0 Data positive	I/O	D0_VDDIO33_USB
D0_USB0_DM	USB2.0 Data minus	I/O	D0_VDDIO33_USB

2.2.2 EPHY Interface description

The EBC7702 core board has already integrated 4 Gigabit PHY in its design.

The description of D0-EPHY0 is basically the same as that of D0-EPHY1. D0_SGMII0-WOL has a remote wake-up function, and the network signal is transmitted to D0-EPHY0, which then outputs the D0_SGMII0-WOL signal.

Table 2-6 EPHY Interface description

Signal Name	Description	Type	Power Supply
D0_EPHY0_MDI0+	Media Dependent Interface0	IO	D0_VDDIO18
D0_EPHY0_MDI0-		IO	D0_VDDIO18
D0_EPHY0_MDI1+	Media Dependent Interface1	IO	D0_VDDIO18
D0_EPHY0_MDI1-		IO	D0_VDDIO18
D0_EPHY0_MDI2+	Media Dependent Interface2	IO	D0_VDDIO18
D0_EPHY0_MDI2-		IO	D0_VDDIO18
D0_EPHY0_MDI3+	Media Dependent Interface3	IO	D0_VDDIO18
D0_EPHY0_MDI3-		O	D0_VDDIO18
D0_EPHY0_LED2	High=Link Up at 1000Mbps Blinking=Transmitting or Receiving.	O	D0_VDDIO18
D0_EPHY0_LED1	Low=Link Up at 100Mbps Blinking=Transmitting or Receiving.	O	D0_VDDIO18
D0_RGMII0_WOL	Connect to INTB/PMEB, Wake up with network	O	3.3V

2.2.3 SATA Interface description

The core board supports SATA3.0 and can support up to 6Gbps;

Table 2-7 SATA3.0 PIN description

Signal Name	Description	Type	Power Supply
D0_SATA_TXP	SATA Transmitter Lane positive terminal	O	D0_VPTX_SATA
D0_SATA_TXM	SATA Transmitter Lane minus terminal	O	D0_VPTX_SATA
D0_SATA_RXM	SATA Receiver Lane minus terminal	I	D0_VP_SATA

D0_SATA_RXP	SATA Receiver Lane positive terminal	I	D0_VP_SATA

2.2.4 SDIO interface

D0_SDIO-0, D0_SDIO_1, D0_SDIO0_3, D0_SDIO0_4 can support SD cards, up to SDR104 mode, and also support SDIO interface peripherals. D0_SDIO0 supports loading system startup files, so it is recommended in the design to connect D0_SDIO0 to an SD card.

Table 2-8 SDIO PIN description

Signal Name	Description	Type	Power Supply
D0_SDIO0_D0	SDIO data line0	I/O	D0_VDDIO18_EMMCSD D0_VDDIO33_EMMCSD
D0_SDIO0_D1	SDIO data line1	I/O	
D0_SDIO0_D2	SDIO data line2.	I/O	
D0_SDIO0_D3	SDIO data line3	I/O	

2.2.5 JTAG Interface

The main processors of the JTAG0 interface are CPUs (LPCPU NPU D2D CPU and MCPU). JTAG0 of all processors except SCPU and DSP are connected in a daisy chain manner in the chip, and a software configuration bypass mechanism is provided to remove the JTAG of a certain processor from the chain to adapt to different debugging requirements. The JTAG0 PIN pin is a pin reuse function, so the system needs to configure the pin to be effective for JTAG function during power on initialization

Table 2-9 JTAG0 Debugging processor

JTAG	processor
JTAG0	Die0:MCPU, Die0:LPCPU, Die0:NPU, Die0:D2D, Die0:CPU Die1:MCPU, Die1:LPCPU, Die1:NPU, Die1:D2D, Die1:CPU

Table 2-10 JTAG0 PIN description

Signal Name	Description	Type	Power Supply
D0_JTAG0_TDI	D0_JTAG0 Data In	I	VDDIO18
D0_JTAG0_TMS	D0_JTAG0 Mode Select	I	VDDIO18
D0_JTAG0_TCK	D0_JTAG0 Clock	I	VDDIO18
D0_JTAG0_TDO	D0_JTAG0 Data Out	O	VDDIO18

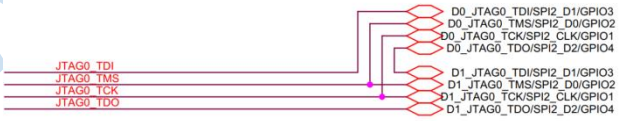

Figure 2-3 JTAG0 Design Reference

2.2.6 MR_RESET interface

Signal Name	Description	Type	Power Supply
MR_RESET	Connect to EIC7702X KEY_RESET_N	I	VDDIO18

2.3 J2/J3 Detailed description of the interface

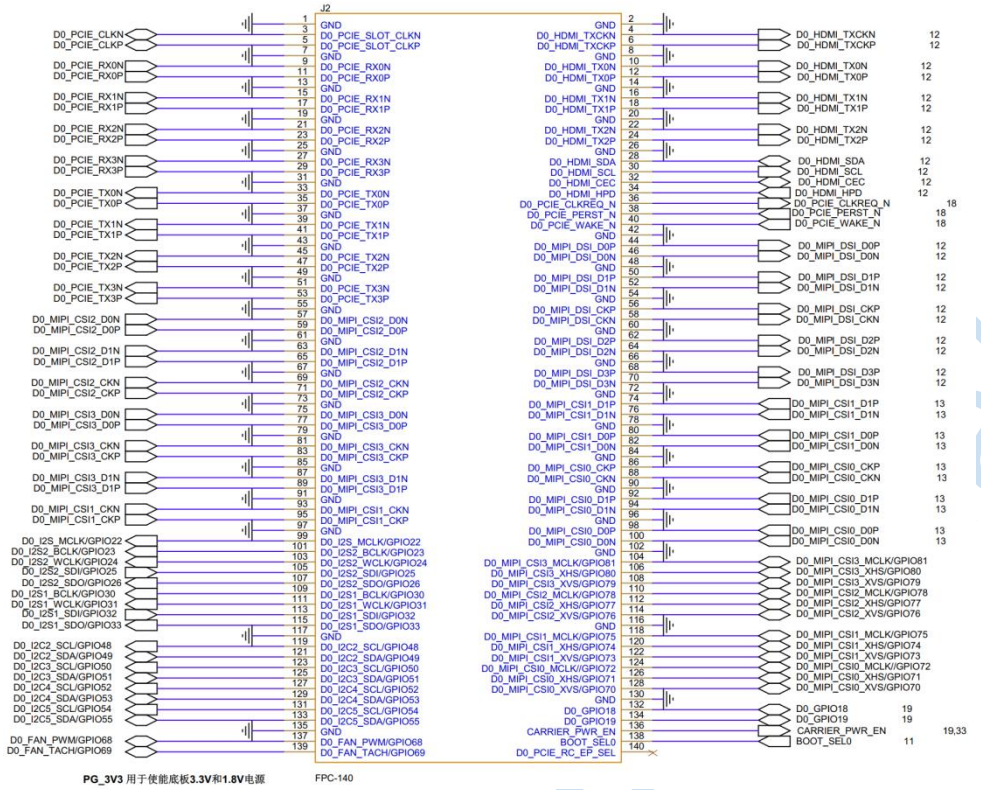

Figure 2-4 J2 Interface schematic diagram

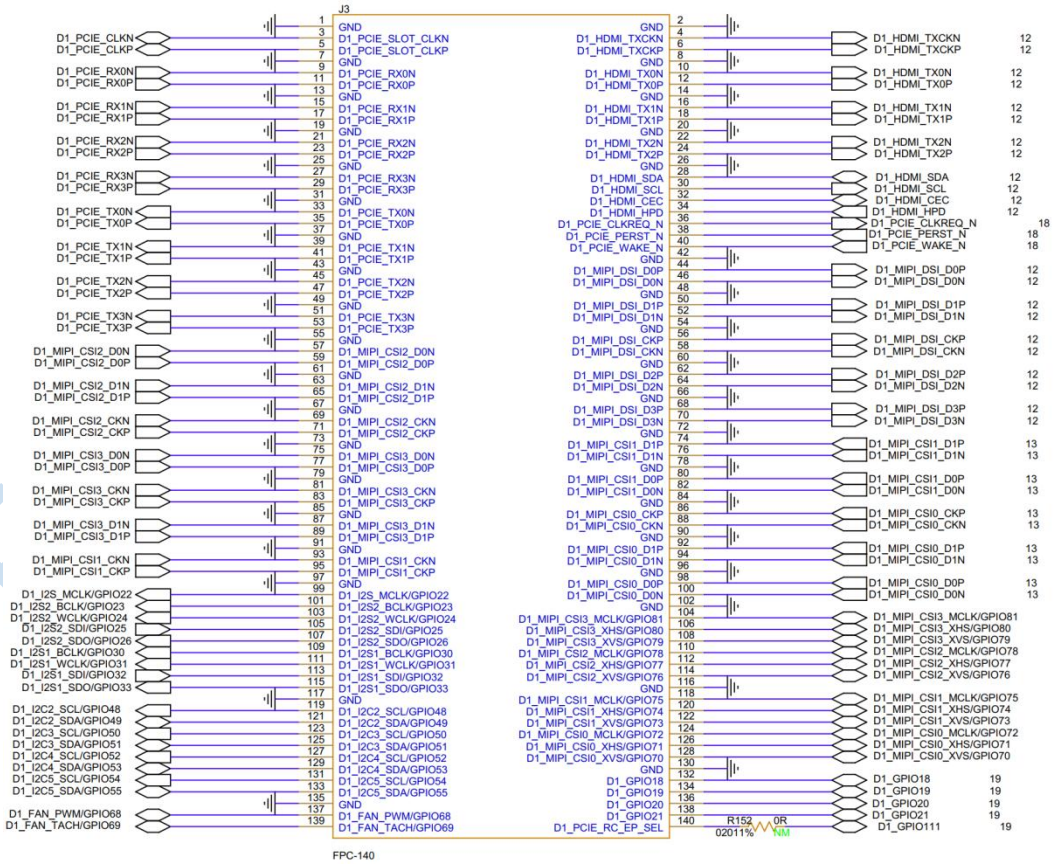

Figure 2-5 J3 Interface schematic diagram

2.3.1 PCIE Interface

PCIE3.0 4-lane interface, supports up to 8Gbps, supports RC and EP modes, switches modes through J12/J40 jumper cap installation, installed in EP mode, not installed in RC mode. One of the signal lists is shown below.

Table 2-11 PCIE3.0 PINdescription

Signal Name	Description	Type	Power Supply
D0_PCIE_CLKN	PCIE reference clock lane negative terminal	I	D0_VP_PCIE
D0_PCIE_CLKP	PCIE reference clock lane positive terminal	I	D0_VP_PCIE
D0_PCIE_RX0N	PCIE RX lane0 negative terminal	I	D0_VP_PCIE
D0_PCIE_RX0P	PCIE RX lane0 positive terminal	I	D0_VP_PCIE
D0_PCIE_RX1N	PCIE RX lane1 negative terminal	I	D0_VP_PCIE
D0_PCIE_RX1P	PCIE RX lane1 positive terminal	I	D0_VP_PCIE
D0_PCIE_RX2N	PCIE RX lane2 negative terminal	I	D0_VP_PCIE
D0_PCIE_RX2P	PCIE RX lane2 positive terminal	I	D0_VP_PCIE
D0_PCIE_RX3N	PCIE RX lane3 negative terminal	I	D0_VP_PCIE
D0_PCIE_RX3P	PCIE RX lane3 positive terminal	I	D0_VP_PCIE
D0_PCIE_TX0N	PCIE TX lane0 negative terminal	O	D0_VP_PCIE
D0_PCIE_TX0P	PCIE TX lane0 positive terminal	O	D0_VP_PCIE
D0_PCIE_TX1N	PCIE TX lane1 negative terminal	O	D0_VP_PCIE
D0_PCIE_TX1P	PCIE TX lane1 positive terminal	O	D0_VP_PCIE
D0_PCIE_TX2N	PCIE TX lane2 negative terminal	O	D0_VP_PCIE
D0_PCIE_TX2P	PCIE TX lane2 positive terminal	O	D0_VP_PCIE
D0_PCIE_TX3N	PCIE TX lane3 negative terminal	O	D0_VP_PCIE
D0_PCIE_TX3P	PCIE TX lane3 positive terminal	O	D0_VP_PCIE
D0_PCIE_CLKREQ_N	PCIE clock requirement	O	VDDIO18
D0_PCIE_PERST_N	PCIE Reset signal	I/O	VDDIO18
D0_PCIE_WAKE_N	PCIE Link Reactivation	I/O	VDDIO18

D0_SCIE_CKN and D0_SCIE_CKP are used as input signals to receive CLK signals provided by the motherboard or external sources.

2.3.2 HDMI interface

The EIC7702X SOM core board supports HDMI PHY and is designed as follows:

- There should be ESD protection on the HDMI signal, and the ESD device should be placed near the HDMI connector with a parasitic capacitance of less than 0.3pF;
- HDMI and MIPI DSI share OSD and cannot be used simultaneously.

Table 2-12 HDMI PIN description

Signal Name	Description	Type	Power Supply
D1_HDMI_TXCKN	TMDS Clock-	O	D1_VPH_HDMI
D1_HDMI_TXCKP	TMDS Clock+	O	D1_VPH_HDMI
D1_HDMI_TX0N	TMDS Data0-	O	D1_VPH_HDMI
D1_HDMI_TX0P	TMDS Data0+	O	D1_VPH_HDMI
D1_HDMI_TX1N	TMDS Data1-	O	D1_VPH_HDMI
D1_HDMI_TX1P	TMDS Data1+	O	D1_VPH_HDMI
D1_HDMI_TX2N	TMDS Data2-	O	D1_VPH_HDMI
D1_HDMI_TX2P	TMDS Data2+	O	D1_VPH_HDMI
D1_HDMI_SDA	SDA (I2C Serial Data Line for DDC)	I/O	D1_VPH_HDMI
D1_HDMI_SCL	SCL (I2C Serial clock for DDC)	O	D1_VPH_HDMI
D1_HDMI_CEC	CEC	I/O	D1_VPH_HDMI

D1_HDMI_HPD	Hot Plug Detect	I	D1_VPH_HDMI

Note: When connecting external HDMI sockets D1-HDMI CEC, D1-HDMI SDA, and D1-HDMI SCL, attention should be paid to level conversion. The reference design is as follows:

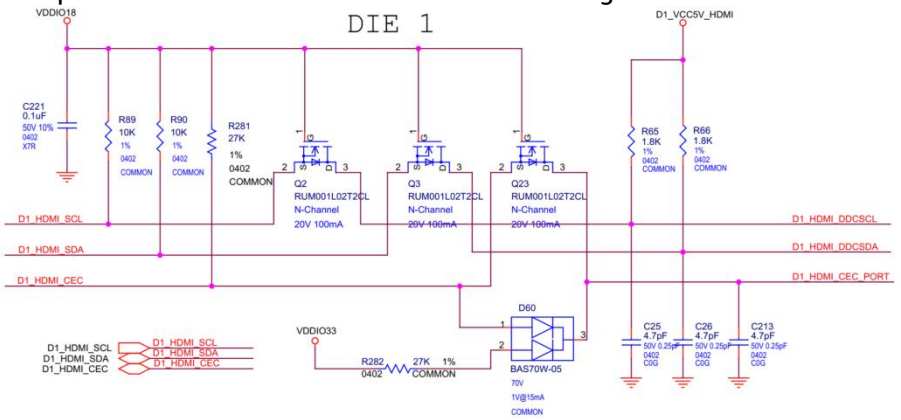

Figure 2-6 HDMI Signal level conversion

2.3.3 MIPI CSI interface

The EIC7702X core board has 8 CSI Combo PHY, all of which support C-PHY and D-PHY. Each PHY has 2 lanes and supports merging 2 PHY into 4 lanes. C-PHY supports up to 1.2 and D-PHY supports up to 2.1. The definition of the CSI pin of Die0 in various modes is shown in the table below.

EIC7702X C-PHY, D-PHY mode description:

Table 2-13 MIPI CSI PIN description

Ball Name	D-PHY mode	C-PHY mode
D0_MIPI_CSI0_CKN	D0_MIPI_CSI0_CKN	D0_MIPI_CSI0_C1
D0_MIPI_CSI0_CKP	D0_MIPI_CSI0_CKP	D0_MIPI_CSI0_C0
D0_MIPI_CSI0_D0N	D0_MIPI_CSI0_D0N	D0_MIPI_CSI0_B0
D0_MIPI_CSI0_D0P	D0_MIPI_CSI0_D0P	D0_MIPI_CSI0_A0
D0_MIPI_CSI0_D1N	D0_MIPI_CSI0_D1N	D0_MIPI_CSI0_B1
D0_MIPI_CSI0_D1P	D0_MIPI_CSI0_D1P	D0_MIPI_CSI0_A1
D0_MIPI_CSI1_CKN	D0_MIPI_CSI1_CKN	D0_MIPI_CSI1_C1
D0_MIPI_CSI1_CKP	D0_MIPI_CSI1_CKP	D0_MIPI_CSI1_C0
D0_MIPI_CSI1_D0N	D0_MIPI_CSI1_D0N	D0_MIPI_CSI1_B0
D0_MIPI_CSI1_D0P	D0_MIPI_CSI1_D0P	D0_MIPI_CSI1_A0
D0_MIPI_CSI1_D1N	D0_MIPI_CSI1_D1N	D0_MIPI_CSI1_B1
D0_MIPI_CSI1_D1P	D0_MIPI_CSI1_D1P	D0_MIPI_CSI1_A1
D0_MIPI_CSI2_CKN	D0_MIPI_CSI2_CKN	D0_MIPI_CSI2_C1
D0_MIPI_CSI2_CKP	D0_MIPI_CSI2_CKP	D0_MIPI_CSI2_C0
D0_MIPI_CSI2_D0N	D0_MIPI_CSI2_D0N	D0_MIPI_CSI2_B0
D0_MIPI_CSI2_D0P	D0_MIPI_CSI2_D0P	D0_MIPI_CSI2_A0
D0_MIPI_CSI2_D1N	D0_MIPI_CSI2_D1N	D0_MIPI_CSI2_B1

D0_MIPI_CSI2_D1P	D0_MIPI_CSI2_D1P	D0_MIPI_CSI2_A1
D0_MIPI_CSI3_CKN	D0_MIPI_CSI3_CKN	D0_MIPI_CSI3_C1
D0_MIPI_CSI3_CKP	D0_MIPI_CSI3_CKP	D0_MIPI_CSI3_C0
D0_MIPI_CSI3_D0N	D0_MIPI_CSI3_D0N	D0_MIPI_CSI3_B0
D0_MIPI_CSI3_D0P	D0_MIPI_CSI3_D0P	D0_MIPI_CSI3_A0
D0_MIPI_CSI3_D1N	D0_MIPI_CSI3_D1N	D0_MIPI_CSI3_B1
D0_MIPI_CSI3_D1P	D0_MIPI_CSI3_D1P	D0_MIPI_CSI3_A1

Table 2-14 EIC7702X D-PHY2/4 Lane mode

Ball Name	D-PHY 2 Lane mode	D-PHY 4 Lane mode
D0_MIPI_CSI0_CKN	D0_MIPI_CSI0_CKN	D0_MIPI_CSI0_CKN
D0_MIPI_CSI0_CKP	D0_MIPI_CSI0_CKP	D0_MIPI_CSI0_CKP
D0_MIPI_CSI0_D0N	D0_MIPI_CSI0_D0N	D0_MIPI_CSI0_D0N
D0_MIPI_CSI0_D0P	D0_MIPI_CSI0_D0P	D0_MIPI_CSI0_D0P
D0_MIPI_CSI0_D1N	D0_MIPI_CSI0_D1N	D0_MIPI_CSI0_D1N
D0_MIPI_CSI0_D1P	D0_MIPI_CSI0_D1P	D0_MIPI_CSI0_D1P
D0_MIPI_CSI1_CKN	D0_MIPI_CSI1_CKN	-
D0_MIPI_CSI1_CKP	D0_MIPI_CSI1_CKP	-
D0_MIPI_CSI1_D0N	D0_MIPI_CSI1_D0N	D0_MIPI_CSI0_D2N
D0_MIPI_CSI1_D0P	D0_MIPI_CSI1_D0P	D0_MIPI_CSI0_D2P
D0_MIPI_CSI1_D1N	D0_MIPI_CSI1_D1N	D0_MIPI_CSI0_D3N
D0_MIPI_CSI1_D1P	D0_MIPI_CSI1_D1P	D0_MIPI_CSI0_D3P

2.3.4 MIPI DSI Interface

The EIC7702X core board MIPI DSI supports D-PHY mode, which is the same as MIPI CSI D-PHY mode, except that MIPI DSI is video output and MIPI CSI is video input, with opposite signal directions. MIPI DSI D-PHY adopts 4Lane mode.

Note: MIPI DSI and HDMI share OSD and cannot be used simultaneously.

Table 2-15 MIPI DSI PIN description

Ball Name	Description	Type	Power Supply
D0_MIPI_DSI_D0P	MIPI D-PHY Data0+	O	D0_VPH_DSI
D0_MIPI_DSI_D0N	MIPI D-PHY Data0-	O	D0_VPH_DSI
D0_MIPI_DSI_D1P	MIPI D-PHY Data1+	O	D0_VPH_DSI
D0_MIPI_DSI_D1N	MIPI D-PHY Data1-	O	D0_VPH_DSI
D0_MIPI_DSI_CKP	MIPI D-PHY clock+	O	D0_VPH_DSI
D0_MIPI_DSI_CKN	MIPI D-PHY clock-	O	D0_VPH_DSI
D0_MIPI_DSI_D2P	MIPI D-PHY Data2+	O	D0_VPH_DSI
D0_MIPI_DSI_D2N	MIPI D-PHY Data2-	O	D0_VPH_DSI
D0_MIPI_DSI_D3P	MIPI D-PHY Data3+	O	D0_VPH_DSI

D0_MIPI_DSI_D3N	MIPI D-PHY Data3-	O	D0_VPH_DSI

2.3.5 PWM/FAN/BOOT_SEL Interface description

Table 2-16 FAN/BOOT_SEL PIN description

Signal Name	Description	Type	Power Supply
D0_FAN_PWM/GPIO68	FAN pwm control	O	VDDIO18
D0_FAN_TACH/GPIO69	FAN TACH	I	VDDIO18
BOOT_SEL0	If Input High,boot from USB02.0 If Input Low,boot from SPI0	I	VDDIO18

BOOT_SEL0 is pulled down by default on the core board, and the core board starts from SPI FLASH by default. If you want to switch to USB 02.0 startup, you need to short-circuit J13

BOOT_SEL0 USB02.0 boot reference design:

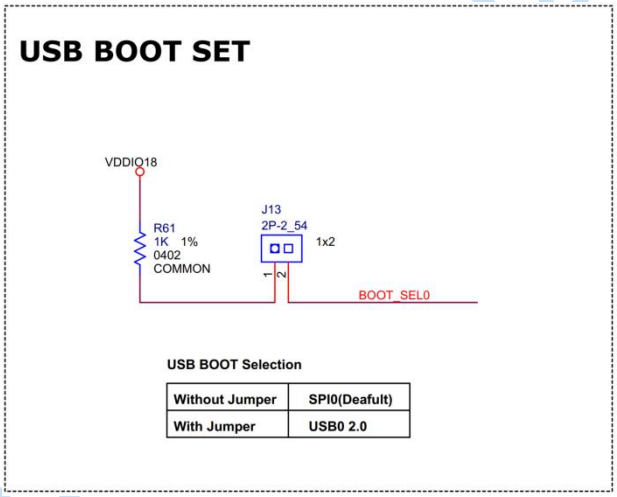

Figure 2-7 BOOT from USB02.0 Reference design circuit

3. Carrier Board Interface description

Table 3-1 Interface description

type	interface	quantity	description
Rear panel interface	SOC TYPE-C	1	debug Used for debugging EIC7702X or MCU debug
	USB 3.0	2	
	USB 2.0	2	
	SDIO	1	Micro SD card slot, supports onboard flash expansion
	RJ45	4	Supports 10/100/1000Mbps speeds, D0 ETH0 has network wake-up function
	HDMI	2	HDMI2.0
	Audio	1	Speaker and mic
Front panel interface	Front Audio	1	Audio 9-pin
	Front Panel	1	LED/RESET/POWER

	Front USB	1	19-pin for USB
	Front Type-E	1	
In board interface	SDIO WiFi Module	1	Reserved WiFi Module interface for M.2 E-KEY interface
	40 Pin Header	1	Development and use
	PCIE	2	Supports dual PCIe X16 slots, PCIe 3.0 4-lane interface, up to 8Gbps, supports RC and EP modes
	SATA	2	Provide one M.2 M key connector and one SATA 7 pin connector, both supporting SATA3.0 and up to 6Gbps.

4. Recommended working conditions

Table 4-1 Recommended Operating Conditions

Recommended Operating Conditions				
Symbol	Parameter	Min	Max	Unit
12V	ATX power supply or DC power supply voltage	10.8	13.2	V
5VSB	Standby 5 Voltage	4.5	5.5	V
T_A	Operating temperature	-20	50	℃

EIC7702X Development board supports ATX Power or DC12V power supply.
In the bare board state, it supports ATX Power or DC12V power supply. When installed in the chassis, it can only be powered by ATX power supply.
When the load power is high (such as when interface peripherals are used frequently and the power is high; or when computing large models), such as exceeding 60W, it is recommended to use an ATX 24 pin power supply. When the load exceeds 144W, using an ATX 24 pin power supply requires connecting an 8-pin ATX CPU 12V power supply header to increase power supply capacity.

5. Mechanical characteristics

EIC7702X SOM dimensions：85mmX85mm

EIC7702X Carrier board dimensions：203.2mmX170.18mm

5.1 Mechanical dimension diagram

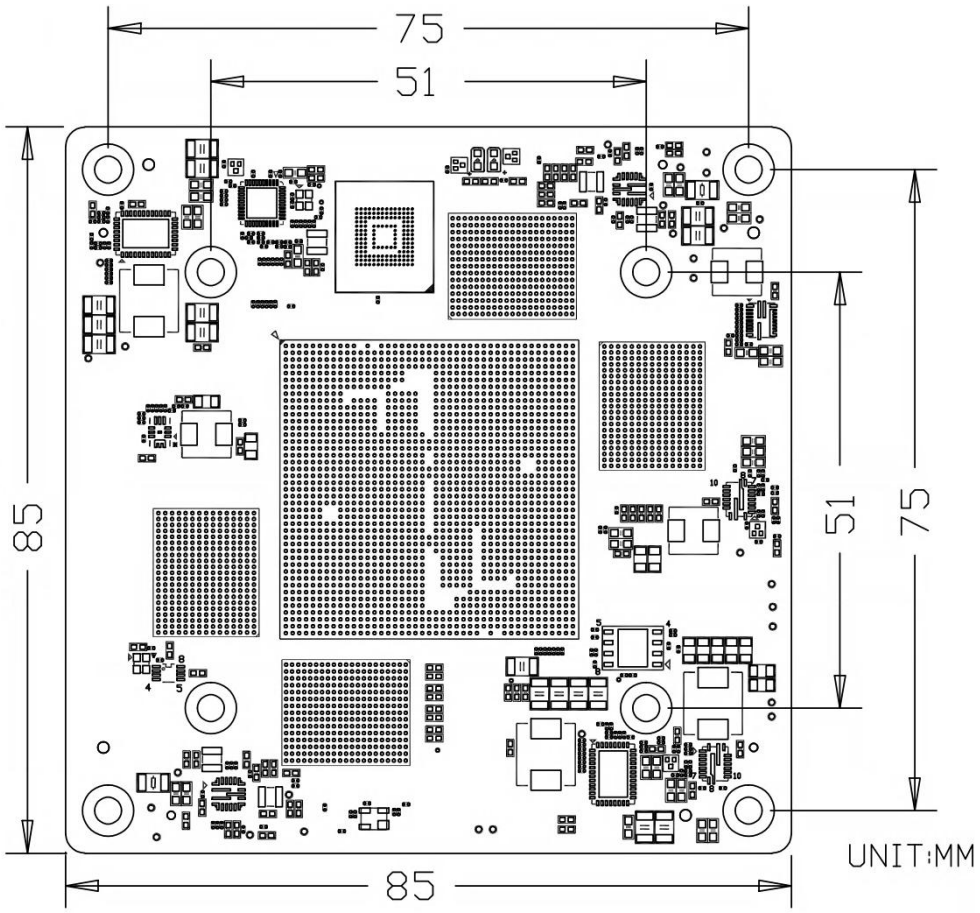

Figure 5-1 EIC7702X SOM Mechanical dimensions

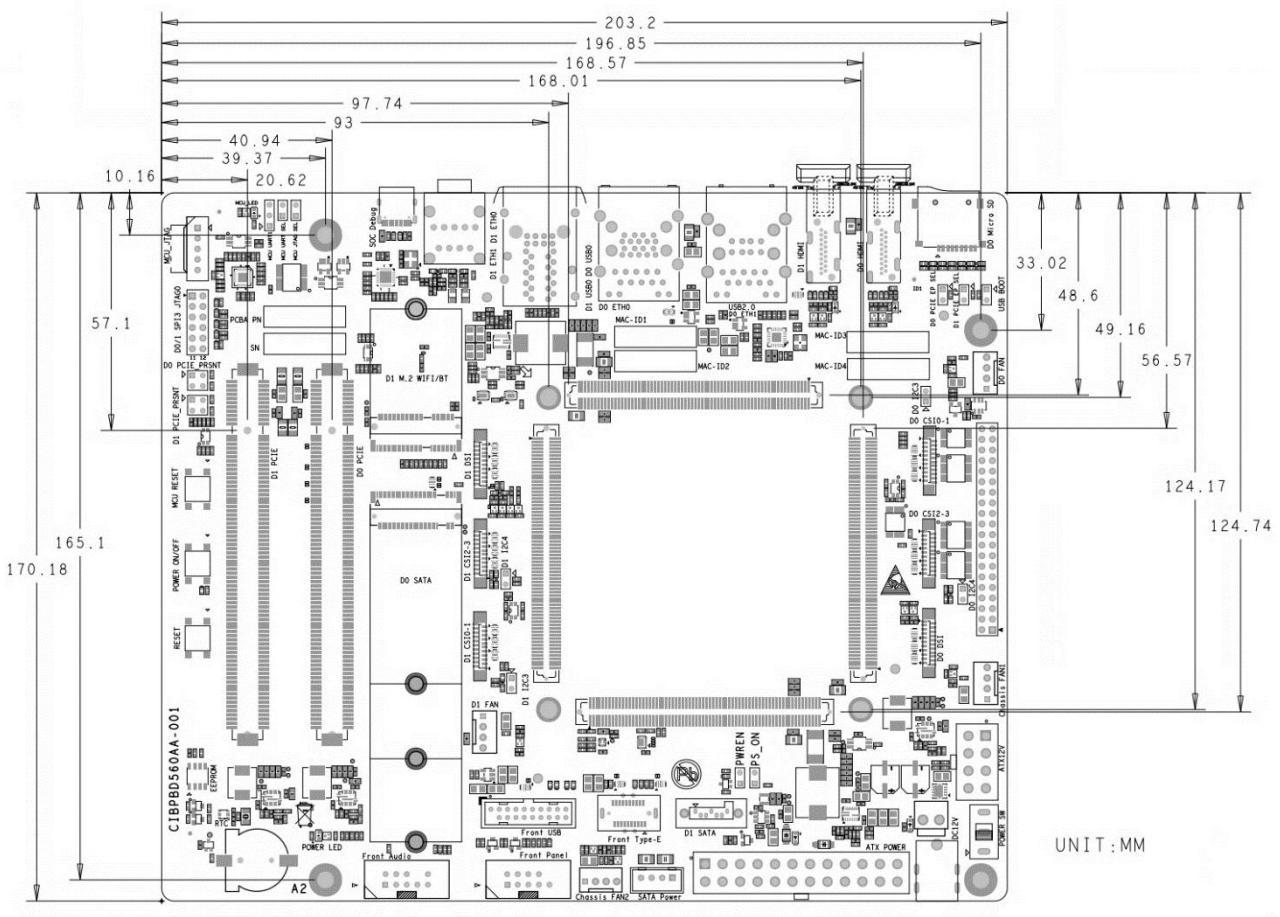

Figure 5-2 EIC7702X Bottom plate mechanical dimensions

5.2 Core board fixing scheme and disassembly precautions

The recommended material list for the fixing scheme of EIC7702X SOM core board is shown in the following table:

Table 5-1 Fixed plan materials

serial number	name	Model parameters	quantity	Remarks
1	Screw/stud	Screw: M3 x5mm, Stud: M3x15mm	4	
2	Core Board	EIC7702X SOM Core Board	1	Including fan and radiator
3	Core board BTB connector	Public IPCB08471ME0S7V (SOM)	4	J1,J2,J3,J4 interfaces
4	Supporting interface components for carrier board	Mother head IPCB08371FE0S7V (Carrier)	4	J1,J2,J3,J4 interfaces

Due to the large amount of materials used for the core board, it is not often unplugged or unplugged. Therefore, when unplugging or unplugging, be careful to avoid causing PCB deformation and to avoid using sharp tools to disassemble the core board.

When disassembling the core board, caution should be exercised. Use hard objects (such as tweezers, screwdrivers, etc.) to slowly lift the four corners of the core board to make them slightly

loose before disassembling. Violent disassembly is prohibited as it may cause damage to the connector.

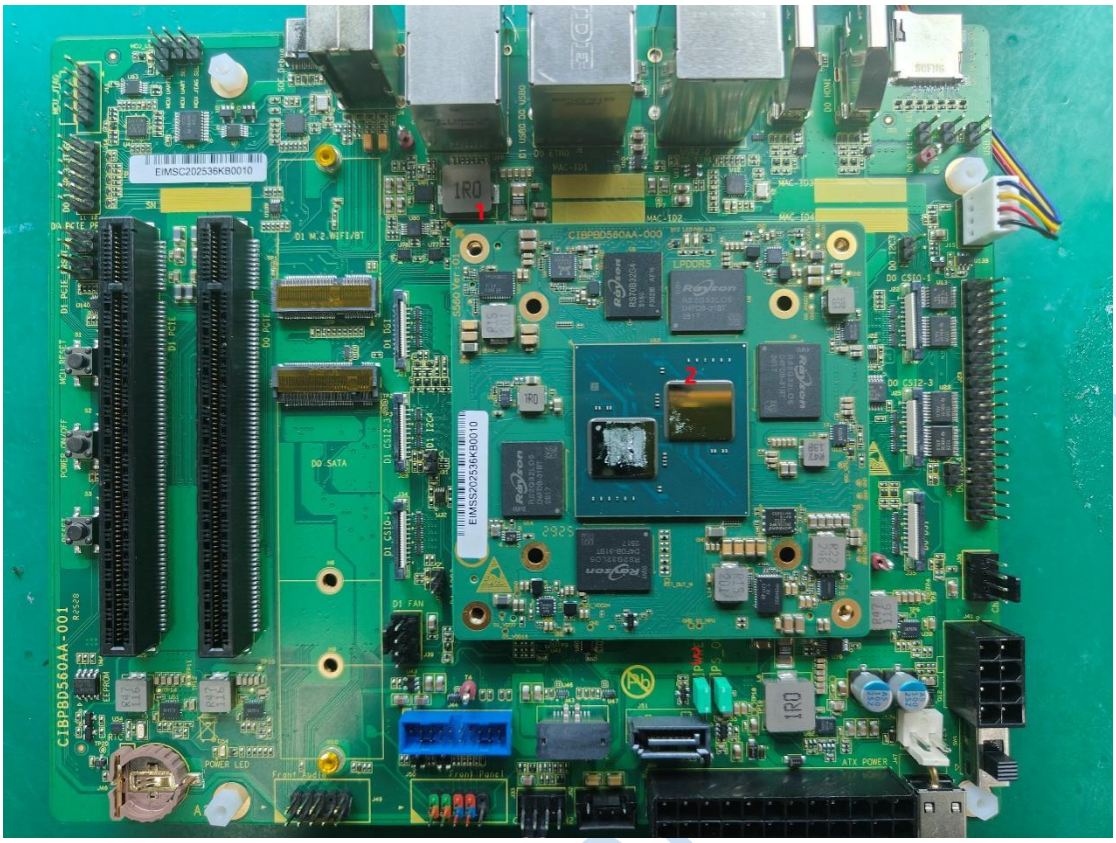

Figure 5-3 EBC7702 Development board Installation Diagram

When installing the SOM and Carrier Board, as shown in the figure above, mark 1 with the corresponding SOM and Carrier Board arrow marks. Align the connectors and press the screw holes with both hands. Press and install SOM in pairs, and check for gaps or warping at the connectors from a cross-sectional perspective;

Mark 2 locations, two bare dies need to be attached with 0.5mm thermal pads. After disassembly, check whether the thermal pads are intact. If there are cracks or damages, replace the thermal pads in a timely manner to avoid affecting the heat dissipation performance; Then install the fan;

It is strictly prohibited to disassemble the core board while it is powered on!