ESWIN

PLIC 设计说明
PLIC Design Specification

Rev 1.0

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Rev 1.0	2025/05/23	初始版本 Initial version

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1. PLIC 简介 Introduction of PLIC

PLIC（Platform-Level Interrupt Controller）是一个处理来自外部的中断的模块，其符合 RISC-V PLIC 规格说明。在此基础上，PLIC 针对安全隔离的需求，添加了安全的扩展。

PLIC (Platform Level Interrupt Controller) is a module that handles interrupts from external sources and complies with the RISC-V PLIC specifications. On this basis, PLIC has added security extensions to meet the requirements of security isolation.

如安全扩展选定，每个内核会增加机器模式、监督模式的中断扩展，在此基础之上，监督模式增加了域（Domain）的扩展。如此可以建立不同模式之间的隔离，以及监督层的不同执行环境中的中断隔离。安全机制的增加不是免费的，会增加相应中断的控制及处理的逻辑。

If the security extension is selected, each core will add interrupt extensions for machine mode and supervisor mode. On this basis, supervisor mode adds domain extensions. In this way, isolation between different modes can be established, as well as interrupt isolation in different execution environments of the supervisory layer. The addition of security mechanisms is not free, it will increase the control and processing logic of corresponding interrupts.

2. PLIC 模块接口 PLIC Module Interface

PCLIC 模块的接口示意图如下。

The interface diagram of the PCLIC module is as follows.

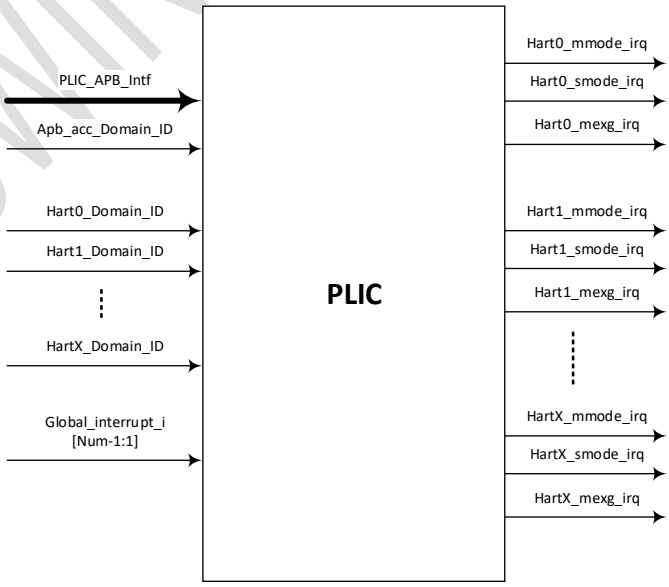

图 2-1 PLIC 接口示意图

Figure 2-1 Schematic Diagram of PLIC Interface

2.1 输入侧 Input Side

1) PLIC APB 接口用于核访问其内部寄存器 。
   The PLIC APB interface is used by the core to access its internal registers.
2) PLIC APB 接口有用户扩展的安全信号 （apb_acc_domain_id)。用于指示当前访问的 domain ID 。
   The PLIC APB interface has a user extended security signal (apd_acc_domain_id). Used to indicate the domain ID currently being accessed.
3) 所有 Hart 的当前域 ID 指示信号。
   The current domain ID indicator signal for all Harts.
4) 外部的终端输入。Global_interrupt[NUM-1： 1]. 由于 global_interrupt 0 在内部固定为 0。
   External terminal input. Global_interrupt [NUM-1:1]. Due to global_interrupt 0 being internal tie 0.

2.2 输出侧 Output Side

1) 每个 Hart 的机器模式中断请求。
   Machine mode interrupt request for each Hart.
2) 每个 Hart 的监督模式中断请求。
   Interrupt requests in supervisor mode for each Hart.
3) 每个 Hart 的监督模式上下文切换中断请求。
   Interrupt request in supervisor mode for switching context for each Hart.

3. PLIC 的功能原理图 Functional Schematic Diagram of PLIC

3.1 PLIC 的模块图 Module Diagram of PLIC

PLIC 模块内部有 APB 接口、寄存器模块、中断检测、中断仲裁 4 个大部分。

The PLIC module has four main components: APB interface, register module, interrupt detection, and interrupt arbitration.

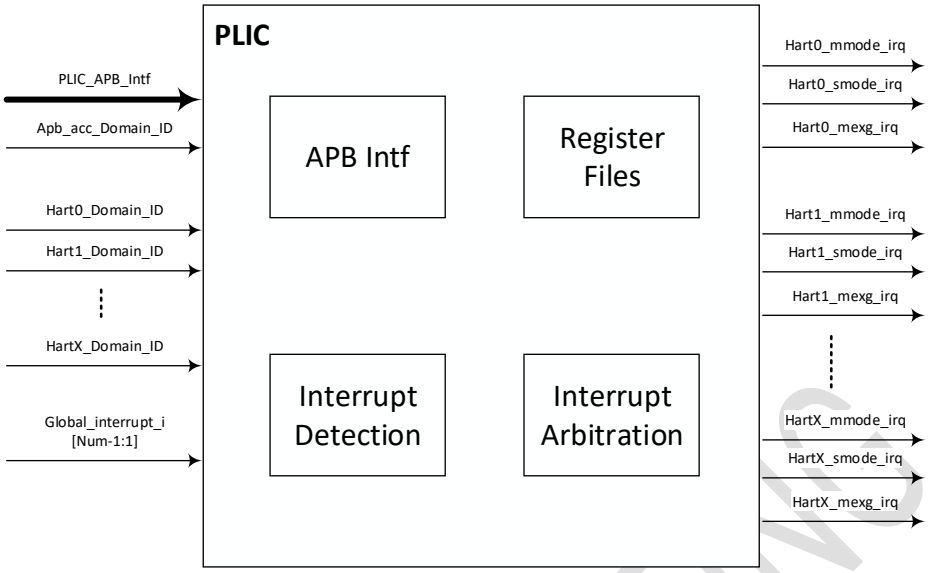

图 3-1 PLIC 模块框图
Figure 3-1 Block Ddiagram of PLIC Module

3.1.1 APB 接口 APB Interface

APB 接口负责将 APB 总线的访问转换为 RAM 接口的形式。这样可以方便对寄存器的访问。从 APB 来访问的安全信号域 ID，特权模式也会送给寄存器模块，用于控制对寄存器的安全访问控制。

The APB interface is responsible for converting the access of the APB bus to the form of the SRAM interface. This can facilitate access to registers. The security signal domain ID accessed from APB, Privilege mode is also sent to the register module to control secure access control to the registers.

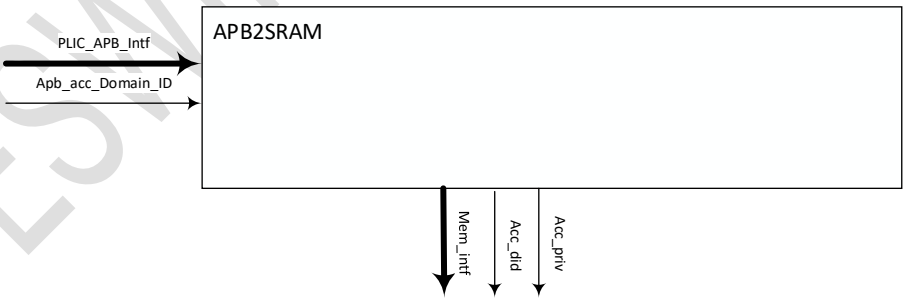

图 3-2 APB2SRAM 接口示意图
Figure 3-2 APB2SRAM Interface Diagram

3.1.2 寄存器模块 Register Module

寄存器模块中寄存器分为公用寄存器和每个核对应的寄存器组。

The registers in the register module are divided into common registers and register groups corresponding to each core.

公用寄存器包括：

Common registers include:

- 每个外部中断控制器的优先级的配置寄存器。
  The configuration register for the priority level of each external interrupt controller.
- 每个外部中断请求状态寄存器。
  Each external interrupt pending status register.

每个核（HartX (X=0,1..N))机器模式(Machine Mode) 对应的寄存器组：

Register groups corresponding to machine mode for each core (HartX (X=0,1.. N)):

- Hart X 的机器模式中断使能配置寄存器。
  Hart X's machine mode interrupt enable configuration register.
- Hart X 的机器模式中断触发阈值（Threshold)配置寄存器。
  Hart X's machine mode interrupt trigger threshold configuration register.
- Hart X 的机器模式中断响应、完成(Claim/Complete)寄存器。
  Hart X's machine mode interrupt claim and complete register.

每个核（Hart X (X=0,1..N))监督模式对应的寄存器组：

Register groups corresponding to the supervisor mode for each core (Hart X (X=0,1.. N)):

- Hart X 的监督模式的安全域 Y(Y =0,1..M)中断使能配置寄存器。
  The domain Y (Y=0,1.. M) interrupt enable configuration register of Hart X's supervisor mode
- Hart X 的监督模式的安全域 Y(Y =0,1..M)配置寄存器。
  The domain Y (Y=0,1.. M) configuration register of Hart X's supervisor mode.
- Hart X 的监督模式的安全域 Y(Y =0,1..M)中断响应、完成(Claim/Complete)寄存器。
  The domain Y (Y=0,1.. M) interrupt response and claim/complete registers of Hart X's supervisor mode.
- Hart X 的监督模式的外部中断上下文请求（Pending)状态寄存器 Mexg。
  The external interrupt context pending status register Mexg of Hart X's supervisor mode.

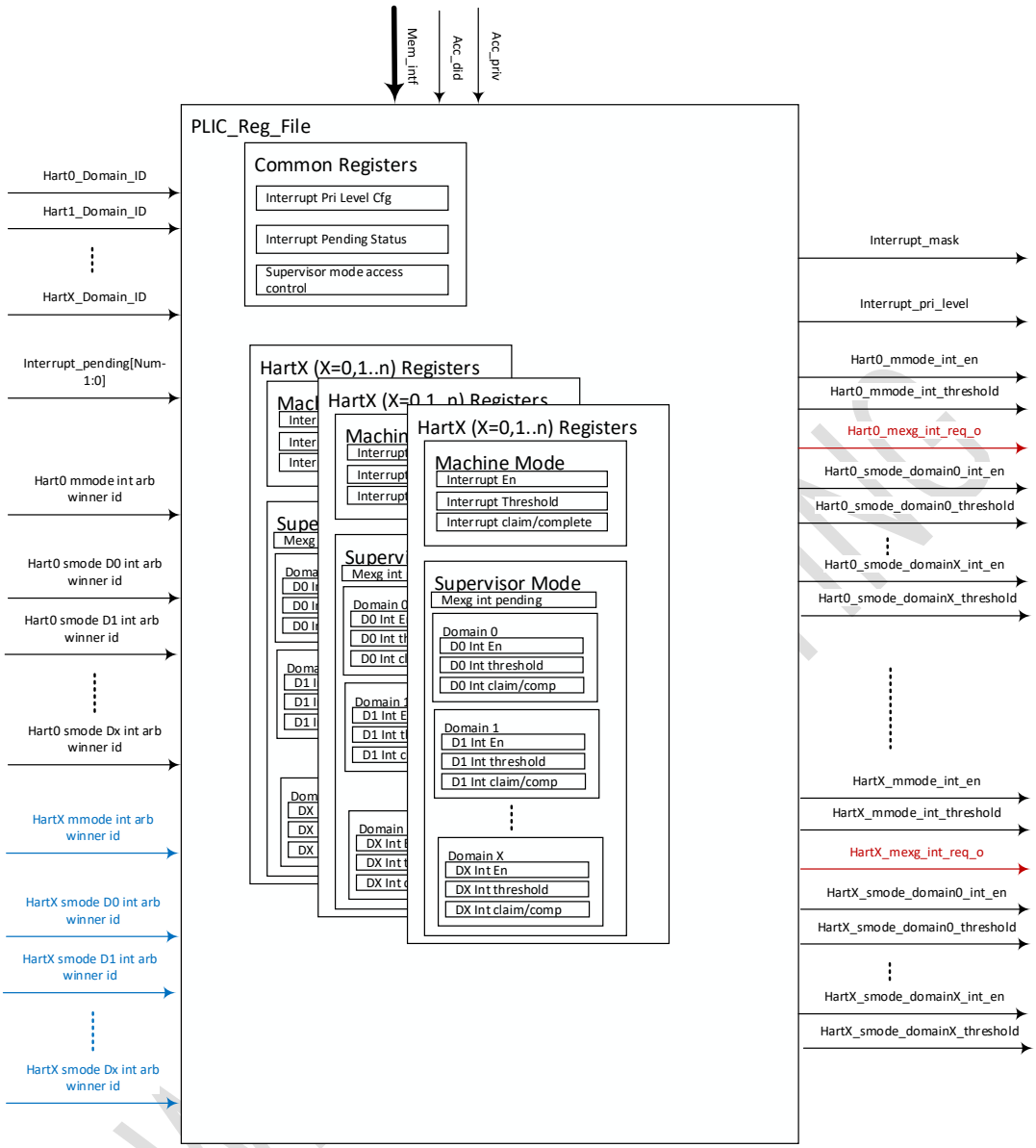

图 3-3 PLIC 寄存器模块图

Figure 3-3 PLIC Register Module Diagram

3.1.3 中断检测 Interrupt Detection

中断检测模块检测每一个外部中断信号是否有高电平，如果当前的中断检测使能，那么当前中断有效。输出相应的请求状态给寄存器模块和中断仲裁模块。

The interrupt detection module detects whether each external interrupt signal has a high level. If the current interrupt detection is enabled, then the current interrupt is valid. Output the corresponding pending status to the register module and interrupt arbitration module.

注意：

Attention:

1) 当中断输入保持为高电平，中断响应后，如果中断服务程序不清除中断请求，中断请求持续保持高电平，中断完成之后，中断检测会认为又一次中断请求有效。
   When the interrupt input remains at a high level, after the interrupt claim, if the interrupt service program does not clear the interrupt request, the interrupt request remains at a high level until the interrupt is completed. Interrupt detection will consider another interrupt request valid.
2) 当中断在中断使能之前已经是高电平，中断使能了之后，也会看作是一次有效请求。
   When an interrupt is already at a high level before it is enabled, and after it is enabled, it is also considered a valid request.

3.1.4 中断仲裁 Interruption of Arbitration

每个 Hart 的机器模式有对应的中断仲裁器。每个 Hart 的监督模式的每一个域（Domain）也有对应的中断仲裁器。每个中断仲裁器的中断机制是一样的。

Each Hart machine mode has a corresponding interrupt arbiter. Each Domain of the supervisor mode of each Hart also has a corresponding interrupt arbiter. The interrupt mechanism of each interrupt arbiter is the same.

中断仲裁机制：

Interruption arbitration mechanism:

1) 如果两个或多个使能的中断，优先级高的中断获胜；
   If two or more enable interrupts, the interrupt with higher priority wins;
2) 如果两个或多个使能的中断，优先级一样，他们的 ID 小的获胜；
   If two or more enable interrupts have the same priority, the one with a smaller ID wins;
   注意： priority=0 时， 不触发中断；
   Note: When priority=0, no interrupt is triggered;

在仲裁的组织上， 当中断很多的话会影响时序（Timing），所以设计加入了中断仲裁树的架构。

In the organization of arbitration, when there are many interrupts, it will affect timing, so the architecture of interrupt arbitration tree has been added.

中断仲裁树架构原理如下。仲裁树分为两级（应该不会大于两级）。

The principle of interrupt arbitration tree architecture is as follows. The arbitration tree is divided into two levels (which should not be greater than two levels).

第一级由多个基本仲裁单元构成。 每个单元只处理固定数量的中断仲裁， 这样当中断很多时，可以做到并行。

The first level consists of multiple basic arbitration units. Each unit only handles a fixed number of interrupt arbitrations, so that when there are many interrupts, parallelism can be achieved.

第二级仲裁由一个基本仲裁单元构成， 这个仲裁单元从第一级仲裁输出的中断中判定出最终的获胜中断请求。

The second level arbitration consists of a basic arbitration unit, which determines the final winning interrupt request from the interrupts output by the first level arbitration.

为了缓解中断的时序，第一级和第二级中可以插入寄存器，这样可以提高中断仲裁逻辑的最大频率。

To alleviate interrupt timing, registers can be inserted in the first and second stages, which can increase the maximum frequency of interrupt arbitration logic.

具体的原理如下图：

The specific principle is shown in the following figure:

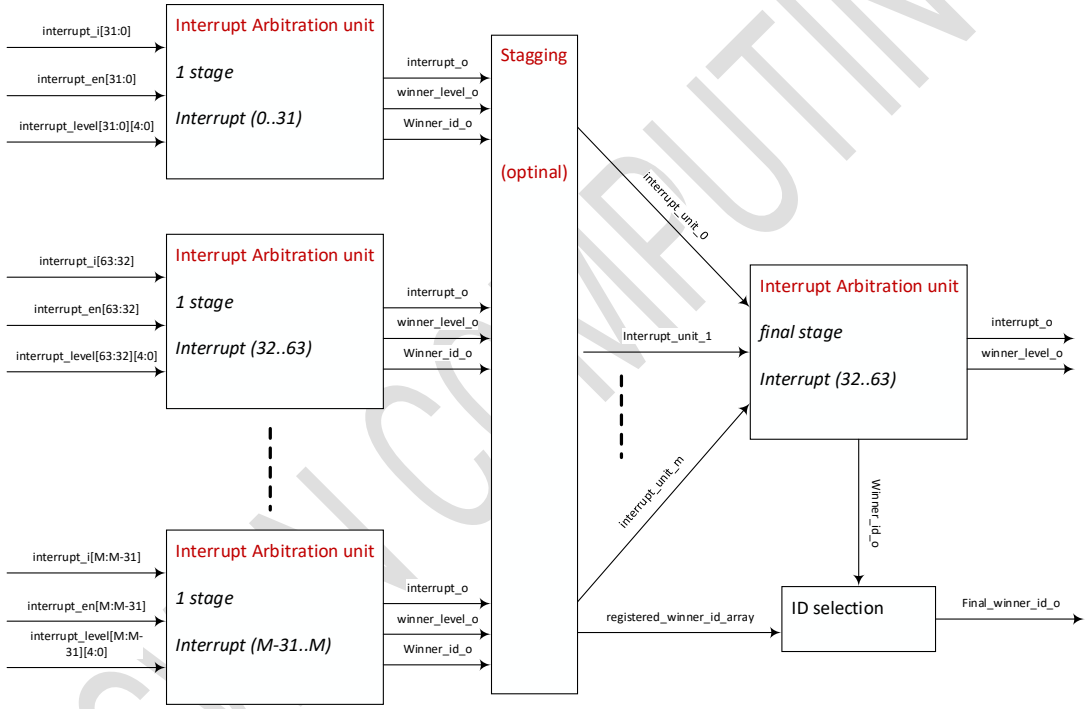

图 3-4 中断仲裁原理图

Figure 3-4 Interrupt Arbitration Schematic

4. PLIC 寄存器 PLIC Register

PLIC 寄存器是地址映射的。 PLIC 的基地址是: 0x0300_0000。

The PLIC register is address mapped. The base address of PLIC is: 0x0300:0000.

寄存器的地址也符合 RISC-V PLIC 的规范，规范详情请见：
https://github.com/riscv/riscv-plic-spec/blob/master/riscv-plic.adoc

The address of the register also complies with the specifications of RISC-V PLIC. For

details of the specifications, please refer to:https://github.com/riscv/riscv-plic-spec/blob/master/riscv-plic.adoc

寄存器地址列表如下。

The register address map is as follows.

表 4-1 寄存器地址列表

Table 4-1 PLIC Register Address Map

PLIC Register Map (Base Address = 0x0300_0000)					
偏移量 Offset	**名称 Name**	**属性 Attr.**	**宽度 Width**	**描述 Description**	**备注 Remarks**
Global Interrupt Priority Level Configuration					
0x0+4xIRQ_ID	Interrupt priority config	RW	4 Byte	外部中断 X (X=0,1..n)优先级配置寄存器 External interrupt X (X=0,1.. N) priority configuration register	1. 外部中断 0 的优先级固定为 0。不可以配置。 2. 中断优先级位宽取决于优先级的数目。 例如 32 个优先级，宽度为 5 位。剩余寄存器 bits 是保留位。 1.The priority of external interrupt 0 is fixed to 0. Cannot be configured. 2.The interrupt priority bit width depends on the number of priorities. For example, 32 priorities with a width of 5 bits. The remaining register bits are reserved bits.
Global Interrupt Pending Status					
0x1000	Interrupt pending status register 0	R	4 Byte	外部中断 31..0 请求状态寄存器 External	1.外部中断 0 的状态绑定为 0 不可改变。

PLIC Register Map (Base Address = 0x0300_0000)					
偏移量 Offset	**名称 Name**	**属性 Attr.**	**宽度 Width**	**描述 Description**	**备注 Remarks**
				Interrupt 31.0 Request Status Register	1. The state of external interrupt 0 is tie to 0 and cannot be changed.
0x1004	Interrupt pending status register 1	R	4 Byte	外部中断 63..32 请求状态寄存器 External interrupt 63.. 32 request status register	
.....	.....	..	..	.....	.....
Supervisor Mode Access Control					
0x20_0FFC	Supervisor mode access control	RW	4 Byte	在监督模式下，Bit0 控制 supervisor 寄存器的可写性。此寄存器只有机器模式可写。监督模式只读。 Bit0 控制 In supervisor mode, Bit0 controls the writability of the supervisor register. This register can only be written in machine mode. Supervisor mode is read-only.	1.中断 0 的状态绑定为 0。不可配置。 31..1 可配置。 1. Bind the state of interrupt 0 to 0. Not configurable. 31.1 configurable.
Hart X (X=0,1..n) Machine Mode & MEXG					
0x2000+0x1000 x hart_id	HartX machine mode interrupt enable	RW	4 Byte	HartX(X=0,1..n) 机器模式中断 (31..0) 使能	1.中断 0 的状态绑定为 0。不可配置。 31..1 可

PLIC Register Map (Base Address = 0x0300_0000)					
偏移量 Offset	名称 Name	属性 Attr.	宽度 Width	描述 Description	备注 Remarks
				(enable)寄存器	配置。 1. Bind the state of interrupt 0 to 0. Not configurable. 31.1 configurable.
0x2004+0x2000x hart_id	HartX machine mode interrupt enable	RW	4 Byte	HartX(X=0,1..n)机器模式中断(63..32) 使能(enable)寄存器 HartX(X=0,1..N) machine mode interrupt (31.0) enable register HartX (X=0,1..N) machine mode interrupt (63.. 32) enable register	
.....	.....	..	..	.....	.....
0x20_0000+0x2_0000x hart_id	HartX machine mode interrupt threshold	RW	4 Byte	HartX(X=0,1..n)机器模式中断阈值寄存器 HartX (X=0,1..N) machine mode interrupt threshold register	
0x20_0004+0x2_0000xhart_id	HartX machine mode interrupt claim/complete	RW	4 Byte	HartX(X=0,1..n)机器模式中断响应和完成寄存器 HartX (X=0,1..N) machine mode interrupt claim and complete register	

PLIC Register Map (Base Address = 0x0300_0000)					
偏移量 Offset	**名称 Name**	**属性 Attr.**	**宽度 Width**	**描述 Description**	**备注 Remarks**
0x20_0008+0x2_0000x hart_id	HartX supervisor mode MEXG pending status	R	4 Byte	HartX(X=0,1..n) 监督模式 Mexg 请求状态寄存器 HartX (X=0,1..N) Supervisor Mode Mexg Pending Status Register	基于 domain ID 宽度为 16， 这里寄存器宽度也为 16。 Based on the domain ID width of 16, the register width here is also 16.
Hart X (X=0,1..n) Supervisor Mode Domain Y (Y =0,1,..m)					
0x2080+0x1000x hart_id + 0x80 x domain_id	HartX supervisor mode interrupt enable	RW	4 Byte	HartX(X=0,1..n) 监督模式 domain Y(Y =0,1,..m)中断 (31..0) 使能寄存器 HartX (X=0,1..N) supervisor mode domain Y (Y=0,1,.. M) interrupt (31.0) enable register	1.中断 0 的状态绑定为 0。不可配置。 31..1 可配置。 1. Bind the state of interrupt 0 to 0. Not configurable. 31.1 configurable.
0x2084+0x1000x hart_id + 0x80 x domain_id	HartX supervisor mode interrupt enable	RW	4 Byte	HartX(X=0,1..n) 监督模式 domain Y(Y =0,1,..m)中断 (63..32) 使能寄存器 HartX (X=0,1..N) supervisor mode domain Y (Y=0,1,.. M) interrupt (63..32) enable register	
.....	.....	..	..	.....	.....
0x20_1000+0x2_0000x hart_id +	HartX supervisor mode interrupt threshold	RW	4 Byte	HartX(X=0,1..n) 监督模式	

PLIC Register Map (Base Address = 0x0300_0000)					
偏移量 Offset	名称 Name	属性 Attr.	宽度 Width	描述 Description	备注 Remarks
0x1000 x domain_id				domain Y(Y =0,1,..m)中断阈值寄存器 HartX (X=0,1.. N) supervisor mode domain Y (Y=0,1,.. M) interrupt threshold register	
0x20_1004+0x2_0000x hart_id + 0x1000 x domain_id	HartX supervisor mode interrupt claim/complete	RW	4 Byte	HartX(X=0,1..n)监督模式 domain Y(Y =0,1,..m)中断响应和完成(claim/complete)寄存器 HartX (X=0,1.. N) supervisor mode domain Y (Y=0,1,.. M) interrupt claim and complete register	

4.1 全局中断优先级配置寄存器 Global Interrupt Priority Configuration Register

每个中断有一个中断优先级配置寄存器。 当中断的优先级为 0 时，表示禁用中断。对于 0 号中断，它的优先级固定为 0。

Each interrupt has an interrupt priority configuration register. When the priority of the interrupt is 0, it indicates that the interrupt is disabled For interrupt number 0, its priority is fixed to 0.

表 4-2 全局中断优先级配置寄存器

Table 4-2 Global Interrupt Priority Configuration Register

地址偏移量 Address Offset		0x0 + 4 x 中断编号 0x0 + 4 x Interrupt ID		
位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
[4:0]	Priority level	RW	0x0	此寄存器机器模式可写，或者监督模式下带监督模式许可时可写；此寄存器机器模式，或者监督模式可读。 This register can be written in machine mode or supervisor mode with smode permission; This register can be read in machine mode or supervisor mode.
[31:0]	reserved	reserved	0x0	

4.2 全局中断请求状态寄存器 Global Interrupt Pending Status Register

每个中断有一个对应位（Bit），显示是否有等待的中断. 对于中断 ID 0，它的状态位始终为 0。

Each interrupt has a corresponding bit that displays whether there are waiting interrupts for interrupt ID 0, its status bit is always 0.

表 4-3 全局中断状态寄存器

Table 4-3 Global Interrupt Status Register

地址偏移量 Address Offset		0x1000 + 4 x (中断数量）/32 0x1000 + 4 x (Interrupt Quantity）/32		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
[31:0]	Pending status	R	0x0	每一位显示当前中断是否有请求存在。 注意：中断 0 的请求绑定为 0。 此寄存器机器模式，或者监督模式可读。 Each display shows whether there is a request for the current interrupt.

地址偏移量 Address Offset		0x1000 + 4 x (中断数量）/32 0x1000 + 4 x (Interrupt Quantity）/32		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
				Note: The request to interrupt 0 is tie to 0. This register can be read in machine mode or supervisor mode.

4.3 监督模式中断控制寄存器 Supervisor Mode Access Control Register

此寄存器的 bit0，用于控制监督模式的监督模式寄存器的写权限。

The bit0 of this register is used to control the write permission of the supervisor mode to the supervisor register.

表 4-4 监督模式中断控制寄存器

Table 4-4 Supervisor Mode Interrupt Control Register

地址偏移量 Address Offset		0x20_0FFC		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
[0:0]	Supervisor register write permission	RW	0x0	此寄存器只是机器模式可读可写。 监督模式只读。 在监督模式下 当 bit0 =0, 监督模式的寄存器只读； 当 bit0 =1, 监督模式的寄存器可读可写。 This register is only readable and writable in machine mode. supervisor mode is read-only. In supervisor mode When bit0=0, the register in supervisor mode is read-only; When bit0=1, the register in supervisor mode is readable and writable.

4.4 Hart X(X=0,1..n)机器模式中断使能寄存器 Hart X(X=0,1..n) Machine Mode Interrupt Enable Register

每个中断有一位使能配置。对于中断 ID 0，它的使能位绑定为 0。

Each interrupt has an enable configuration. For interrupt ID 0, its enable bit is tie to 0.

表 4-5 机器模式中断使能寄存器

Table 4-5 Machine Mode Interrupt Enable Register

地址偏移量 Address Offset		0x2000+ 0x1000xhart_id+ 4 x (中断数量）/32 0x2000+ 0x1000xhart_id+ 4 x (Interrupt Quantity）/32		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
[31:0]	Enable bits	RW	0x0	每一位对应某个 Hart 机器模式一个中断 ID 的使能。 注意：中断 ID 0 的使能位绑定为 0。 此寄存器只可以机器模式读写。 Each interrupt ID corresponding to a Hart machine mode is enabled. Note: The enable bit for interrupt ID 0 is tie to 0. This register can only be read and written in machine mode.

4.5 Hart X(X=0,1..n)机器模式中断优先级阈值配置寄存器 Hart X(X=0,1..n) Machine Mode Interrupt Priority Level Threshold Configuration Register

当 Hart X 使能的中断有效且它的优先级大于阈值，才会触发 Hart X 机器模式中断输出。

When the interrupt enabled by Hart X is valid and its priority level is greater than the threshold, the Hart X machine mode interrupt output will be triggered.

表 4-6 机器模式中断优先级阈值寄存器

Table 4-6 Machine Mode Interrupt Priority Level Threshold Register

地址偏移量 Address Offset		0x20_0000+0x2_0000x 核编号 0x20_0000+0x2_0000x hart_id		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
[4:0]	Threshold	RW	0x0	此寄存器只可以机器模式读写。 This register can only be read and written in machine mode.
[31:0]	reserved	reserved	0x0	

4.6 Hart X(X=0,1..n) 机器模式中断响应与完成寄存器 Machine Mode Interrupt Claim and Complete Register

当读此寄存器时返回 Hart X 当前机器模式挂起的中断 ID。并且，清除相应中断请求状态位（Pending Status Bit）. 如果读返回的中断 ID=0，表示没有中断请求。

When reading this register, return the pending winner interrupt ID of Hart X's current machine mode. And, clear the corresponding interrupt pending status bit. If the interrupt ID returned by the read is 0, it means there is no interrupt pending

当写此寄存器时，表示写入的中断 ID 已经完成中断服务。

When writing this register, it indicates that the interrupt ID written has completed interrupt service.

表 4-7 机器模式中断响应与完成寄存器

Table 4-7 Machine Mode Interrupt Claim and Complete Register

地址偏移量 Address Offset		0x20_0004+0x2_0000x 核编号 0x20_0004+0x2_0000x hart_id		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
[9:0]	Interrupt ID	RW	0x0	中断响应/完成 ID。 此寄存器只可以机器模式读写。 Interrupt claim/complete ID. This register can only be read and written in machine mode.
[31:10]	reserved	reserved	0x0	

4.7 Hart X(X=0,1..n) 监督模式安全域 Y(y=0,1..m) 中断使能寄存器 Hart X (X=0,1.. N) Supervisor Mode Security Domain Y (y=0,1.. M) Interrupt Enable Register

每个中断有一位使能配置。对于中断 ID 0，它的使能位绑定为 0。

Each interrupt has an enable configuration. For interrupt ID 0, its enable bit is tie to 0.

表 4-8 监督模式中断使能寄存器

Table 4-8 Supervisor Mode Interrupt Enable Register

地址偏移量 Address Offset		0x2080+0x1000x hart_id + 4 x (中断数量）/32 + domain_id x 0x80 0x2080+0x1000x hart_id + 4 x (Interrupt Quantity）/32 + domain_id x 0x80		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description

[31:0]	Enable bits	RW	0x0	每一位对应某个 Hart 监督模式 Domain ID Y 下的一个中断 ID 的使能。 注意：中断 ID 0 的使能位绑定为 0. 这个寄存器只有在机器模式或者监督模式下 smode permission enable，并且访问的 DID 和寄存器在的 Domain 匹配才可以写。读的时候条件不需要 smode permission。 Enable each interrupt ID corresponding to a Hart supervisor mode Domain ID Y. Note: The enable bit for interrupt ID 0 is tie to 0 This register can only be written when smode permission is enabled in machine mode or supervisor mode, and the accessed DID match the domain of the register. When reading, there is no need for a smooth permission condition.

4.8 Hart X(X=0,1..n) 监督模式安全域 Y(y=0,1..m)中断优先级阈值配置寄存器 Hart X (X=0,1.. N) Supervisor Mode Security Domain Y (y=0,1.. M) Interrupt Priority Threshold Configuration Register

当 Hart X 使能的中断有效且它的优先级大于阈值，且当前 Hart X 的安全域 ID 和此寄存器的安全域 ID 一致时， 触发 Hart X 监督模式中断输出。 否则触发 Hart X 监督模式的 MEXG 中断。

When the interrupt enabled by Hart X is valid and its priority level is greater than the threshold, and the current domain ID of Hart X matches the domain ID of this register, the Hart X supervisor mode interrupt output is triggered. Otherwise, trigger the MEXG interrupt of the Hart X supervisor mode.

表 4-9 监督模式中断优先级阈值配置寄存器

Table 4-9 Supervisor Mode Interrupt Priority Threshold Configuration Register

地址偏移量 Address Offset		0x20_1000+ 0x2_0000x hart_id + 0x1000 x 域编号 0x20_1000+ 0x2_0000x hart_id + 0x1000 x domain_id		
对应位 Bits	**字段名称 Field Name**	**属性 Attr.**	**重置 Reset**	**描述 Description**
[4:0]	Threshold	RW	0x0	Hart X supervisor mode threshold configure 寄存器只有在机器模式或者监督模式下访问的 DID 和寄存器在的 Domain 匹配才可以读写。

地址偏移量 Address Offset		0x20_1000+ 0x2_0000x hart_id + 0x1000 x 域编号 0x20_1000+ 0x2_0000x hart_id + 0x1000 x domain_id		
对应位 Bits	**字段名称 Field Name**	**属性 Attr.**	**重置 Reset**	**描述 Description**
				The Hart X supervisor mode threshold configuration register can only be read and written when the DID accessed in machine mode or supervisor mode matches the domain of the register.
[31:0]	reserved	reserved	0x0	

4.9 Hart X(X=0,1..n) 监督模式安全域 Y(y=0,1..m) 中断响应与完成寄存器 Hart X (X=0,1.. N) Supervisor Mode Security Domain Y (y=0,1.. M) Interrupt Claim and Complete Register

当读此寄存器时，返回 Hart X 当前监督模式安全域 ID Y(y=0,1..m)的请求挂起的中断 ID。并且，清除相应中断请求状态位（Pending Status Bit）。如果读返回的中断 ID=0，表示没有中断请求。

When reading this register, return the pending winner interrupt ID of Hart X's current supervisor mode domain ID Y (y=0,1.. M). And, clear the corresponding interrupt pending status bit. If the interrupt ID returned by the read is 0, it indicates that there is no interrupt pending.

当写此寄存器时，表示写入的中断 ID 已经完成中断服务。

When writing this register, it indicates that the interrupt ID written has completed interrupt service.

表 4-10 监督模式中断响应与完成寄存器

Table 4-10 Supervisor Mode Interrupt Claim and Complete Register

地址偏移量 Address Offset		**0x20_1004+ 0x2_0000x hart_id + 0x1000 x 域编号 0x20_1004+ 0x2_0000x hart_id + 0x1000 x domain_id**		
对应位 Bits	**字段名称 Field Name**	**属性 Attr.**	**重置 Reset**	**描述 Description**
[9:0]	Interrupt ID	RW	0x0	中断响应/完成 ID。 这个寄存器只有在机器模式或者监督模式下访问的 DID 和寄存器在的 Domain 匹配才可以读写。 Interrupt claim/complete ID. This register can only be read and written when the DID accessed in machine mode or

地址偏移量 Address Offset		0x20_1004+ 0x2_0000x hart_id + 0x1000 x 域编号 0x20_1004+ 0x2_0000x hart_id + 0x1000 x domain_id		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
				supervisor mode matches the domain of the register.
[31:10]	reserved	reserved	0x0	

4.10 Hart X(X=0,1..n) 监督模式 MEXG 中断状态寄存器 Hart X (X=0,1.. N) Supervisor Mode MEXG Interrupt Status Register

当 Hart X 监督模式有中断请求。其相应的中断安全域 ID 和当前 Hart X 的安全域 ID 匹配。请求中断对应安全域 ID 位生效（Assert）.

When the Hart X supervisor has an interrupt pending. The corresponding interrupt domain ID match the current Hart X domain ID. The pending interrupt corresponds to the domain ID bit assert.

表 4-11 监督模式 MEXG 中断状态寄存器

Table 4-11 Supervisor Mode MEXG Interrupt Status Register

地址偏移量 Address Offset		0x20_0008+0x2_0000x 核编号 0x20_0008+0x2_0000x hart_id		
对应位 Bits	字段名称 Field Name	属性 Attr.	重置 Reset	描述 Description
[NUM_DOMAIN-1:0]	Pending status	R	0x0	每一位指示相应的 Supervisor Domain 是否有请求的中断。 此寄存器机器模式或监督模式可读。 Each indicator indicates whether the corresponding Supervisor Domain has a requested interrupt. This register is readable in machine mode or supervisor mode.
[31:NUM_DOMAIN]	reserved	reserved	0x0	