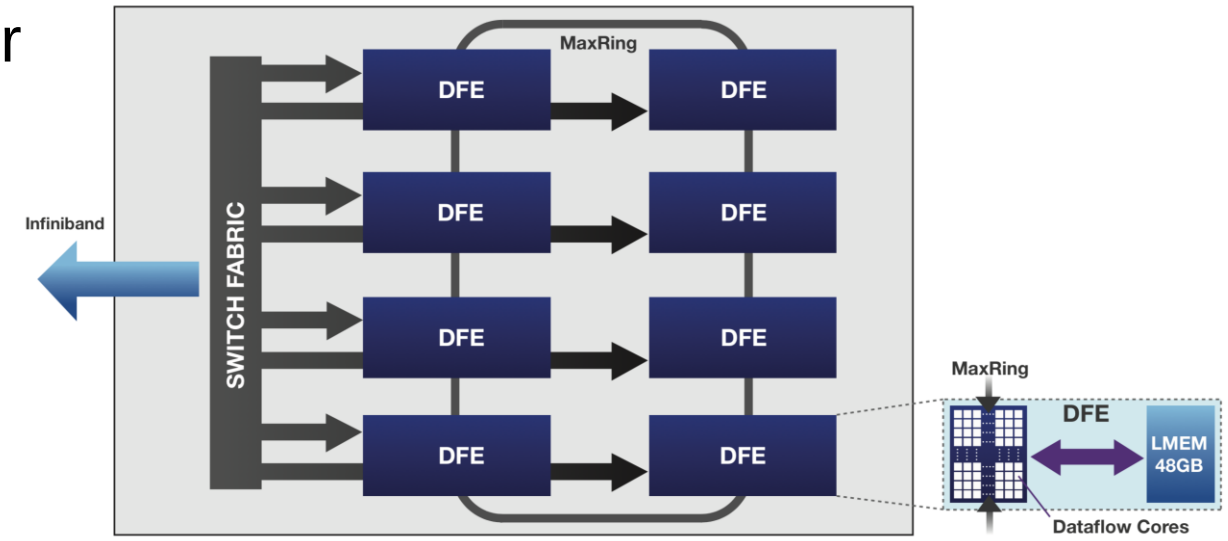
Technical Results Maxeler

Based on newest generation of Data Flow Engine architectures

- MAX5 DFE based on Xilinx Ultrascale FPGAs → low clock rate for power efficiency
- Project impacted MAX5 design

Main R&D focus: Demonstrate usability of architecture for HPC applications

- Application kernels implemented in MaxJ



Maxeler: MAX5 Data Flow Engine

Virtex UltraScale VU9P

- 1,182k Logic units
- 6,840 DSP blocks
- 43.3 MB FMEM

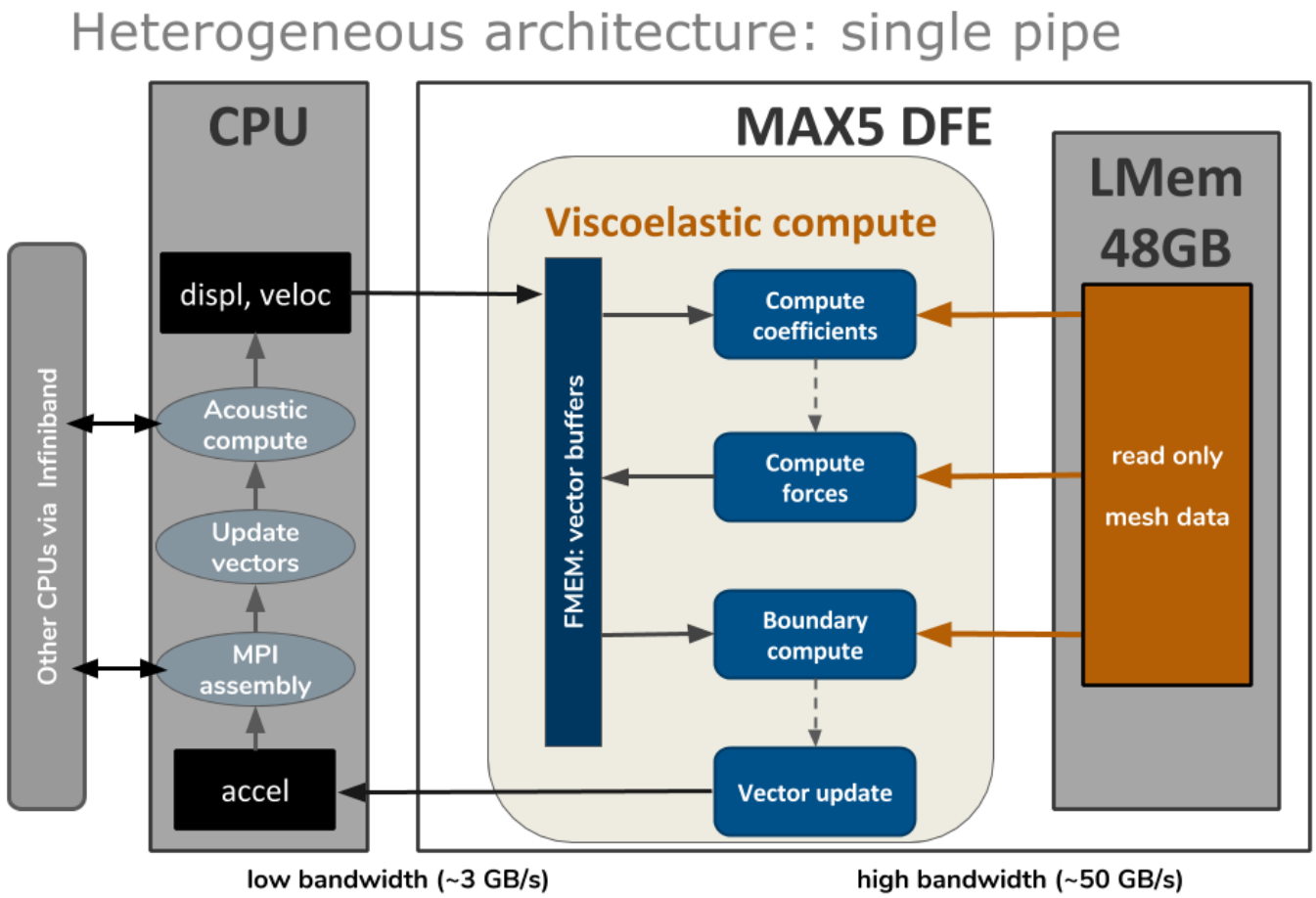
48GB LMEM

- 3 parallel SODIMM
- Low power DDR4

116W peak power consumption

- 81W compute chip
- 10W LMEM
- 13W transceivers
- 12W infrastructure

Maxeler: SpecFEM3D on Data Flow Engine



Maxeler: Application Porting

BQCD

- CG solver with D-Slash operator and clovers on DFE
- Exploring domain decomposition to allow large problem sizes

NEMO

- PDE solver with both implicit and explicit method ported on DFE (including tri-diagonal solver for implicit method)
- Exploring reduced precision and compression

Quantum Espresso

- Propose using architecture with 2 DFEs for FFT + ZGEMM
- Exploring 27-bit fixed-point, 32-bit and 64-bit floating-point precision

SpecFEM3D

- Focus on kernel computing visco-elastic forces
- Multiple computation stages coalesced into single sweep over data on DFE

Pilot System from Maxeler

Smaller pilot system reflecting adjusted Phase III budget

- one 1U MPC-X with 8 MAX5 DFEs
- one 1U AMD EPYC based server
- one 1U login head node

Scaling tests using Amazon AWS cloud

- MAX5 fully compatible with F1 instance
- Elastic scaling between private and public