Lab 10 (All Sections) Prelab: MIPS Pipelining

Name:

Your Name

Sign the following statement:

On my honor, as an Aggie, I have neither given nor received unauthorized aid on this academic work

Type Name

1 Objective

In this lab, you will be implementing a Pipelined MIPS Processor. You should be familiar with the MIPS pipeline (refer to chapter 4 of the text book).

2 Introduction

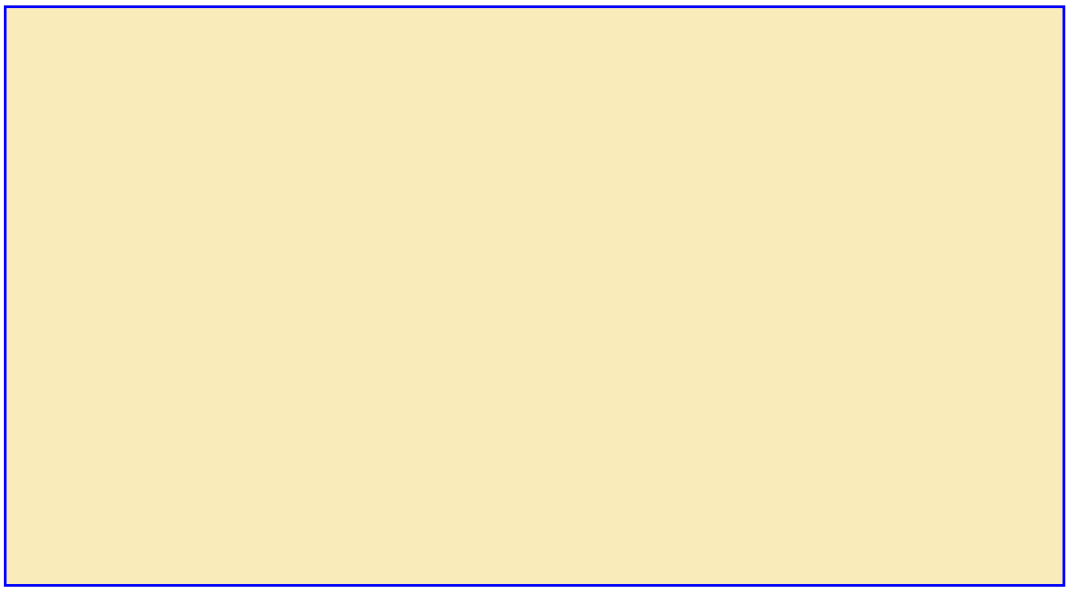
Pipelining is an implementation technique in which multiple instructions are overlapped in execution. Thus the cycle time of the processor is reduced, thereby increasing the instruction throughput in most cases.

3 Questions

1. What are the stages in the canonical MIPS 5-stage pipeline? Explain each stage briefly.

2. For each pipeline stage; list the data path components that will probably be used during that stage.

3. Give a list of pipeline registers that are required. Explain what is the purpose of each register.



4. For each pipeline stage give the list of control signals that need to be enabled when the pipeline is in that stage, ignore pipeline hazards. Explain briefly the purpose of each control line?