

JOHN PETER STEVENSON

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EDUCATION

Stanford University , Ph.D. Electrical Engineering Thesis: <i>Fine-Grain In-Memory Deduplication for Large-Scale Workloads</i> . Faculty advisors: Mark Horowitz and David Cheriton.	2008 – 2013
Stanford University , M.S. Electrical Engineering Focus Areas: Circuit Design and Semiconductor Physics.	2000 – 2002
U.S. Naval Academy , B.S. Control Systems Engineering Graduated 1st in academic standing, degree conferred with distinction. Recipient of Ward Prize for best undergraduate research on multi-aperture camera arrays.	1996 – 2000

EXPERIENCE

HICAMP Systems , Menlo Park, CA, Member of Technical Staff Implemented world's first deduplicated DRAM memory system in FPGA logic. Wrote Verilog RTL for high speed and high strength hash function. Wrote SystemC and C++ test infrastructure that automatically regenerates based on a high level graphical description of system protocol. Code generation implemented in Python and graphical description implemented in GraphViz.	2009 – Present
U.S. Naval Academy , Annapolis, MD, Electrical Engineering Faculty As an officer faculty member, taught undergraduate engineering major and core curriculum classes for 4 semesters. Topics included circuit analysis, logic design, and wireless.	2006 – 2008
Lawrence Livermore National Laboratory , Livermore, CA, Photonics Group Intern As a summer intern, characterized wavelength shift properties of a multiple section edge emitting laser system proposed for use as an optical logic gate.	2007
USS Los Angeles (SSN-688) , Honolulu, HI, Officer As Officer of the Deck, responsible for all operations submerged, surfaced, and in port, in lieu of the ship's Captain. As Engineering Officer of the Watch, responsible for all nuclear power plant operations, in lieu of the ship's Engineer. As Communications Officer and Mechanical Division Officer, supervised a shipboard division (~25 personnel).	2003 – 2006
Honda Research , Mountain View, CA, Computer Vision Intern Investigated algorithms for depth recovery in non-stereoscopic images.	2002
Tensilica , Sunnyvale, CA, Design Verification Intern Wrote scripts to drive verification for customizable RTL code.	2001

HONORS & AWARDS

Best Paper at International Conference on Supercomputing	2012
Best Student Project, Stanford MS&E-273: Punch Mobile	2011
David Cheriton Stanford Graduate Fellowship	2008
Stanford School of Engineering Fellowship	2000
Ward Prize: Best Undergraduate Research Project	2000
Phi Kappa Phi National Honor Society Graduate Study Fellowship	2000
Rhodes Scholarship State Finalist	1999
Eagle Scout	1996

PROJECTS

Zest – Memory Deduplicator for Linux Using LiME, zest counts duplicates in DRAM memory. Captures a snapshot of physical memory from a live instance of Linux. Performs post-mortem fine-grain deduplication to show the benefit of deduplicated memory systems. Shows that memory capacity is increased by over 2x in many common datacenter applications. https://github.com/etep/zest	2012 – Present
The Stanford Circuit Optimization Tool (SCOT) Provides optimal digital circuit design using convex optimization. Integrates with industry standard tools such as SPICE. http://code.google.com/p/thescot	2008 – Present
Punch Mobile Electronic payment processing with integrated consumer loyalty. Provided significant cost savings by disintermediating the credit card payment network using a direct consumer-to-business (C2B) back-end. Voted as top project in MS&E-273 by VC panel.	2011
Solar Boat Project at U.S. Naval Academy – Faculty Mentor Mentored a multidisciplinary team of undergraduates competing in the world championship of solar electric boating.	2006 – 2008
SIMD Floating Point Adder Project – Stanford Independent Projects in VLSI Designed and taped out a fully functional 1x32 / 2x16 bit SIMD floating point adder (IEEE compliant math). Design was fabricated by TSMC in 0.5 μ m technology.	2001

PUBLICATIONS

Sparse Matrix-Vector Multiply on the HICAMP Architecture J.P. Stevenson, A. Firoozshahian, A. Solomatnikov, M. Horowitz, and D. Cheriton, ICS 2012 Winner of Best Paper Award at International Conference on Supercomputing, 2012	2012
HICAMP: Architectural Support for Efficient Concurrency-Safe Shared Structured Data Access D. Cheriton, A. Firoozshahian, A. Solomatnikov, J.P. Stevenson, and O. Azizi, ASPLOS 2012	2012
CPU db: Recording Microprocessor History A. Danowitz, K. Kelley, J. Mao, J.P. Stevenson, and M. Horowitz, CACM 2012	2012
Intermediate Representations for Controllers in Chip Generators K. Kelley, M. Wachs, A. Danowitz, J.P. Stevenson, S. Richardson, M. Horowitz, DATE 2011	2011
An Integrated Framework for Co-Optimization of Architecture and Circuits O. Azizi, A. Mahesri, J.P. Stevenson, N. Zhou, S.J. Patel, and M. Horowitz, DATE 2010	2010