JOHN PETER STEVENSON

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EDUCATION

Stanford University – Ph.D. Candidate, Electrical Engineering 2008 – Present
Fine-grain in-memory deduplication with faculty David Cheriton and Mark Horowitz.

Stanford University – M.S. Electrical Engineering 2000 – 2002
Focus Areas: Circuit Design and Semiconductor Physics

U.S. Naval Academy – B.S. Control Systems Engineering 1996 – 2000
Graduated 1st in academic standing, degree conferred with distinction

WORK EXPERIENCE

Member of Technical Staff, HICAMP Systems – Menlo Park, CA 2009 – Present
Wrote flexible test infrastructure for computer cache and memory subsystems. The test bench, in C++, is generated from a high level directed acyclic graph description so that when the hardware architecture is changed, the test bench automatically updates. Meta-programming accomplished with GraphViz dot language and with Python. Wrote low latency and low power near cryptographic strength in-hardware hash function.

2006 – 2008
Electrical Engineering Faculty, U.S. Naval Academy – Annapolis, MD
As an officer faculty member, taught undergraduate engineering major and core curriculum classes for 4 semesters. Topics included circuit analysis, logic design, and wireless.

Lawrence Livermore National Laboratory Photonics Group – Livermore, CA 2007
As a summer intern, characterized wavelength shift properties of a multiple section edge emitting laser system proposed for use as an optical logic gate.

Officer, Submarines, U.S. Navy – (USS Los Angeles, SSN-688) Pearl Harbor, HI 2002 – 2006
As Officer of the Deck, responsible for all shipboard operations submerged, surfaced, and in port, in lieu of the ship's Captain. As Engineering Officer of the Watch, responsible for all nuclear power plant operations, in lieu of the ship's Engineer. As Communications Officer and Mechanical Division Officer, sole command of a shipboard division (~25 personnel).

Honda Research – Mountain View, CA 2002
As a research intern, investigated algorithms for depth recovery in non-stereoscopic images.

Tensilica – Sunnyvale, CA 2001
As a design verification intern, produced scripts for on-the-fly customized RTL code.

HONORS & AWARDS

Best Paper at International Conference on Supercomputing 2012

Stanford Graduate Fellowship 2008

Stanford School of Engineering Fellowship 2000

Phi Kappa Phi National Honor Society Graduate Study Fellowship 2000

Ward Prize for Best Undergraduate Research Project 2000

Rhodes Scholarship State Finalist 1999

Eagle Scout 1996

PROJECTS

Zest – Memory Deduplicator for Linux 2012 – Present

Captures a snapshot of physical memory from a live instance of Linux. Performs post-mortem fine-grain deduplication to show the benefit of deduplicated memory systems. Memory capacity increased by over 2x in many common datacenter applications.
http://code.google.com/p/thezest

The Stanford Circuit Optimization Tool (SCOT) 2008 – Present

Provides optimal digital circuit design using convex optimization. Integrates with industry standard tools such as SPICE.
http://code.google.com/p/thescot

Punch Mobile 2011

Electronic payment processing with integrated consumer loyalty. Provided significant cost savings by disintermediating the credit card payment network using a direct consumer-to-business (C2B) back-end. Voted as top project in MS&E 273 by VC judging panel.

Solar Boat Project at U.S. Naval Academy – Faculty Mentor 2006 – 2008

Mentored a multidisciplinary team of undergraduates competing in the world championship of solar electric boating.

SIMD Floating Point Adder Project – Stanford Independent Projects in VLSI 2001

Designed and taped out a fully functional 1x32 / 2x16 bit SIMD floating point adder (IEEE compliant math). Design was fabricated by TSMC in 0.5μm technology.

PUBLICATIONS

Sparse Matrix-Vector Multiply on the HICAMP Architecture 2012

J.P. Stevenson, A. Firoozshahian, A. Solomatnikov, M. Horowitz, and D. Cheriton, ICS 2012
Winner of Best Paper Award at International Conference on Supercomputing, 2012

HICAMP: Architectural Support for Efficient Concurrency-Safe Shared Structured Data Access 2012

D. Cheriton, A. Firoozshahian, A. Solomatnikov, J.P. Stevenson, and O. Azizi, ASPLOS 2012

CPU db: Recording Microprocessor History 2012

A. Danowitz, K. Kelley, J. Mao, J.P. Stevenson, and M. Horowitz, CACM 2012

Intermediate Representations for Controllers in Chip Generators 2011

K. Kelley, M. Wachs, A. Danowitz, J.P. Stevenson, S. Richardson, M. Horowitz, DATE 2011

An Integrated Framework for Co-Optimization of Architecture and Circuits 2010

O. Azizi, A. Mahesri, J.P. Stevenson, N. Zhou, S.J. Patel, and M. Horowitz, DATE 2010