JOHN PETER STEVENSON

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EDUCATION

Stanford University, Ph.D. Electrical Engineering 2008 – 2013

Thesis: *Fine-Grain In-Memory Deduplication for Large-Scale Workloads*.

Faculty advisors: Mark Horowitz and David Cheriton.

Stanford University, M.S. Electrical Engineering2008 – 2002
Focus Areas: Circuit Design and Semiconductor Physics.

U.S. Naval Academy, B.S. Control Systems Engineering1996 – 2000
Graduated 1st in academic standing, degree conferred with distinction. Recipient of Ward Prize for best undergraduate research on multi-aperture camera arrays.

EXPERIENCE

HICAMP Systems, Menlo Park, CA, Member of Technical Staff2009 – P
Implemented world's first deduplicated DRAM memory system in FPGA logic. Wrote Verilog RTL for high speed and high strength hash function. Wrote SystemC and C++ test infrastructure that automatically regenerates based on a high level graphical description of system protocol. Code generation implemented in Python and graphical description implemented in GraphViz.

U.S. Naval Academy, Annapolis, MD, Electrical Engineering Faculty20
As an officer faculty member, taught undergraduate engineering major and core curriculum classes for 4 semesters. Topics included circuit analysis, logic design, and wireless.

Lawrence Livermore National Laboratory, Livermore, CA, Photonics
As a summer intern, characterized wavelength shift properties of a multiple section edge emitting laser system proposed for use as an optical logic gate.

USS Los Angeles (SSN-688), Honolulu, HI, Officer2003 – 2006
As Officer of the Deck, responsible for all operations submerged, surfaced, and in port, in lieu of the ship's Captain. As Engineering Officer of the Watch, responsible for all nuclear power plant operations, in lieu of the ship's Engineer. As Communications Officer and Mechanical Division Officer, supervised a shipboard division (~25 personnel).

Honda Research, Mountain View, CA, Computer Vision Intern2002
Investigated algorithms for depth recovery in non-stereoscopic images.

Tensilica, Sunnyvale, CA, Design Verification Intern 2001
Wrote scripts to drive verification for customizable RTL code.

HONORS & AWARDS

Best Paper at International Conference on Supercomputing 2012

Best Student Project, Stanford MS&E-273: Punch Mobile 2011

David Cheriton Stanford Graduate Fellowship 2008

Stanford School of Engineering Fellowship 2000

Ward Prize: Best Undergraduate Research Project 2000

Phi Kappa Phi National Honor Society Graduate Study Fellowship 2000

Rhodes Scholarship State Finalist 1999

Eagle Scout 1996

PROJECTS

Zest – Memory Deduplicator for Linux 2012 – Present

Using LiME, zest counts duplicates in DRAM memory. Captures a snapshot of physical memory from a live instance of Linux. Performs post-mortem fine-grain deduplication to show the benefit of deduplicated memory systems. Shows that memory capacity is increased by over 2x in many common datacenter applications.
https://github.com/etep/zest

Hash-Stats – Overflow Statistics for Large Hash Tables 2014

Table utilization and table overflows are critical issues for large hash tables, but these topics receive scant attention on the Wikipedia and from introductory CS course material. This repository reduces theory to practice. Using published theoretical results, it provides simple matlab scripts to guide the practicing engineer when implementing a large hash table.
https://github.com/etep/hash-stats

The Stanford Circuit Optimization Tool (SCOT) 2008 – Present

Provides optimal digital circuit design using convex optimization. Integrates with industry standard tools such as SPICE.
http://github.com/etep/scot

Punch Mobile 2011

Electronic payment processing with integrated consumer loyalty. Provided significant cost savings by disintermediating the credit card payment network using a direct consumer-to-business (C2B) back-end. Voted as top project in MS&E-273 by VC panel.

Solar Boat Project at U.S. Naval Academy – Faculty Mentor 2006 – 2008

Mentored a multidisciplinary team of undergraduates competing in the world championship of solar electric boating.

SIMD Floating Point Adder Project – Stanford Independent Projects in VLSI 2001

Designed and taped out a fully functional 1x32 / 2x16 bit SIMD floating point adder (IEEE compliant math). Design was fabricated by TSMC in $0.5\mu\mathrm{m}$ technology.

PUBLICATIONS

SI-TM: Reducing Transactional Memory Abort Rates through Snapshot Isolation 2014

H. Litz, D. Cheriton, A. Firoozshahian, O. Azizi, J.P. Stevenson, ASPLOS 2014

Sparse Matrix-Vector Multiply on the HICAMP Architecture 2012

J.P. Stevenson, A. Firoozshahian, A. Solomatnikov, M. Horowitz, and D. Cheriton, ICS 2012
Winner of Best Paper Award at International Conference on Supercomputing, 2012

HICAMP: Architectural Support for Efficient Concurrency-Safe Shared Structured Data Access 2012

D. Cheriton, A. Firoozshahian, A. Solomatnikov, J.P. Stevenson, and O. Azizi, ASPLOS 2012

CPU db: Recording Microprocessor History 2012

A. Danowitz, K. Kelley, J. Mao, J.P. Stevenson, and M. Horowitz, CACM 2012

Intermediate Representations for Controllers in Chip Generators 2011

K. Kelley, M. Wachs, A. Danowitz, J.P. Stevenson, S. Richardson, M. Horowitz, DATE 2011

An Integrated Framework for Co-Optimization of Architecture and Circuits 2010

O. Azizi, A. Mahesri, J.P. Stevenson, N. Zhou, S.J. Patel, and M. Horowitz, DATE 2010