

# JOHN PETER STEVENSON

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## EDUCATION

**Stanford University** 2008 – 2014  
Ph.D. Electrical Engineering

Thesis: *Fine-Grain In-Memory Deduplication for Large-Scale Workloads*

**Stanford University** 2000 – 2002  
M.S. Electrical Engineering

Focus on circuit design and semiconductor physics

**U.S. Naval Academy** 1996 – 2000  
B.S. Control Systems Engineering

Graduated 1st in academic standing  
Degree conferred with distinction

## HONORS & AWARDS

**Best Paper** 2012  
Sparse Matrix-Vector Multiply on the HICAMP Architecture, International Conference on Supercomputing

**Best Startup Project** 2011  
Stanford MS&E-273: Punch Mobile

**David Cheriton Fellow** 2008 – 2014  
Stanford Graduate Fellowship

**SOE Fellow** 2000 – 2002  
Stanford School of Engineering Fellowship

**Ward Prize** 2000  
Best undergraduate research for a multi-aperture camera array

**PKP NHS Fellow** 2000  
Phi Kappa Phi National Honor Society Graduate Study Fellowship

**Rhodes Finalist** 1999  
State level interviewee

**Eagle Scout** 1996

## EXPERIENCE

**Intel** 2014 – Present  
Santa Clara, CA, Silicon Architect

Developed next generation memory technology as a member of the HICAMP team acquired in 2014. Wrote CPU cache performance simulator to validate key aspects of the technology. Contributed key micro-architectural optimizations. Developed rigorous methodology for testing strong low latency hardware hash functions. Led interviews and hired an intern.

**Palo Alto Central Condominiums** 2015 – Present  
Palo Alto, CA, Director

As member of the board of directors, fiduciary responsibility for \$1M annual budget and \$2M reserve fund.

**HICAMP Systems** 2009 – 2014  
Menlo Park, CA, Member of Technical Staff

As member of a seven person team, all engineers, contributed to FPGA implementation of next generation CPU memory. Technology acquired by Intel in 2014.

**U.S. Naval Academy** 2006 – 2008  
Annapolis, MD, Electrical Engineering Faculty

As an officer faculty member, taught undergraduate engineering major and core curriculum classes for 4 semesters. Topics included circuit analysis, logic design, and wireless.

**Lawrence Livermore National Laboratory** 2007  
Livermore, CA, Photonics Group Intern

As a summer intern, characterized wavelength shift properties of a multiple section edge emitting laser system proposed for use as an optical logic gate.

**USS Los Angeles (SSN-688)** 2003 – 2006  
Honolulu, HI, Officer

As Officer of the Deck, responsible for all operations submerged, surfaced, and in port, in lieu of the ship's Captain. As Engineering Officer of the Watch, responsible for all nuclear power plant operations, in lieu of the ship's Engineer. As Communications Officer and Mechanical Division Officer, supervised a shipboard division (~25 personnel).

**Honda Research** 2002  
Mountain View, CA, Computer Vision Intern

Investigated algorithms for depth recovery in non-stereoscopic images.

**Tensilica** 2001  
Sunnyvale, CA, Design Verification Intern

Wrote scripts to drive verification for customizable RTL code.

## PUBLICATIONS

### SITM 2014

*SI-TM: Reducing Transactional Memory Abort Rates through Snapshot Isolation*

H. Litz, D. Cheriton, A. Firoozshahian, O. Azizi, J.P. Stevenson, ASPLOS 2014

### SpMV on HICAMP 2012

*Sparse Matrix-Vector Multiply on the HICAMP Architecture*

J.P. Stevenson, A. Firoozshahian, A. Solomatnikov, M. Horowitz, and D. Cheriton, ICS 2012

Winner of Best Paper Award at International Conference on Supercomputing, 2012

### HICAMP 2012

*HICAMP: Architectural Support for Efficient Concurrency-Safe Shared Structured Data Access*

D. Cheriton, A. Firoozshahian, A. Solomatnikov, J.P. Stevenson, and O. Azizi, ASPLOS 2012

### CPU db 2012

*CPU db: Recording Microprocessor History*

A. Danowitz, K. Kelley, J. Mao, J.P. Stevenson, and M. Horowitz, CACM 2012

### IR for ChipGen 2011

*Intermediate Representations for Controllers in Chip Generators*

K. Kelley, M. Wachs, A. Danowitz, J.P. Stevenson, S. Richardson, M. Horowitz, DATE 2011

### CPU Co-Optimization 2010

*An Integrated Framework for Co-Optimization of Architecture and Circuits*

O. Azizi, A. Mahesri, J.P. Stevenson, N. Zhou, S.J. Patel, and M. Horowitz, DATE 2010

## PROJECTS

### Zest – Memory Deduplicator for Linux 2012 – Present

Using LiME, zest counts duplicates in DRAM memory. Captures a snapshot of physical memory from a live instance of Linux. Performs post-mortem fine-grain deduplication to show the benefit of deduplicated memory systems. Shows that memory capacity is increased by over 2x in many common datacenter applications.

### Hash-Stats 2014

Overflow Statistics for Large Hash Tables

Table utilization and table overflows are critical issues for large hash tables, but these topics receive scant attention on the Wikipedia and from introductory CS course material. This repository reduces theory to practice. Using published theoretical results, it provides simple matlab scripts to guide the practicing engineer when implementing a large hash table.

<https://github.com/etep/hash-stats>

### Stanford Circuit Optimization Tool 2008 – Present

Provides optimal digital circuit design using convex optimization. Integrates with industry standard tools such as SPICE.

<http://github.com/etep/scot>

### Punch Mobile 2011

Electronic payment processing with integrated consumer loyalty. Provided significant cost savings by disintermediating the credit card payment network using a direct consumer-to-business (C2B) back-end. Voted as top project in MS&E-273 by VC panel.

### Faculty Mentor for Solar Boat 2006 – 2008

As an officer faculty member at the U.S. Naval Academy, mentored a multidisciplinary team of undergraduates competing in the world championship of solar electric boating.

### SIMD Floating Point Adder 2001

Designed and taped out a fully functional 1x32 / 2x16 bit SIMD floating point adder with IEEE compliant rounding for Stanford independent projects in VLSI, EE-271. Silicon fabricated by TSMC in 0.5 $\mu$ m technology.