John Peter Stevenson

10 CANEPA CT.
REDWOOD CITY, CA 94062
(650) 906-9549 | jps@pax.markets

EDUCATION

Stanford University 2008 – 2014
Ph.D. Electrical Engineering

Thesis: *Fine-Grain In-Memory Deduplication for Large-Scale Workloads*

Stanford University 2000 – 2002
M.S. Electrical Engineering

Focus on circuit design and semiconductor physics

U.S. Naval Academy 1996 – 2000
B.S. Control Systems Engineering

Graduated 1st in academic standing

HONORS & AWARDS

Y-Combinator 2025
PAX Markets, Inc., YC W25 batch.

Best Paper 2012
Sparse Matrix-Vector Multiply on the HICAMP Architecture, International Conference on Supercomputing

Best Startup Project 2011
Stanford MS&E-273: Punch Mobile

David Cheriton Fellow 2008 – 2014
Stanford Graduate Fellowship

SOE Fellow 2000 – 2002
Stanford School of Engineering Fellowship

Ward Prize 2000
Best undergraduate research for a multi-aperture camera array

PKP NHS Fellow 2000
Phi Kappa Phi National Honor Society Graduate Study Fellowship

Rhodes Finalist 1999

Eagle Scout 1996

EXPERIENCE

PAX Markets 2025 – Present
CEO & Founder | Redwood City, CA

PAX is a new crypto exchange, on a chip. PAX provides unprecedented value to institutional trading participants: for HFT operators, PAX offers fee-based ultra-low latency exchange integrated order placement. All other market participants trade with zero-fees.

Jaguar Technologies 2024 – 2024
Lead Quantitative Researcher | Menlo Park, CA

Developed α models: short term price predictions for crypto markets. Developed low latency high frequency cyrpto trading platform.

Pixie Labs & New Relic 2020 – 2024
Founding & Principal Engineer | San Francisco, CA

Led development of eBPF performance profiler. Developed continuous performance regression testing framework.

Citadel Securities 2016 – 2020
Quantitative HW/SW Developer | Chicago, IL

Hardware software co-design for low latency trading. Implemented machine learning algorithms in FPGA. Wrote hardware emulator for model training.

Intel 2014 – 2016
Silicon Architect | Santa Clara, CA

Developed next generation memory technology as a member of the HICAMP team acquired in 2014. Wrote CPU cache performance simulator to validate key aspects of the technology. Contributed micro-architectural optimizations.

HICAMP Systems 2009 – 2014
Member of Technical Staff | Menlo Park, CA

Member of seven person engineering team, firm and technology acquired by Intel in 2014. Contributed to FPGA implementation of next generation CPU memory controller.

U.S. Naval Academy 2006 – 2008
Electrical Engineering Faculty | Annapolis, MD

As an officer faculty member, taught undergraduate engineering major and core curriculum classes on circuit analysis, logic design, and wireless.

USS Los Angeles (SSN-688) 2003 – 2006
Officer | Honolulu, HI

As Officer of the Deck, responsible for all operations submerged, surfaced, and in port, in lieu of the ship's Captain. As Engineering Officer of the Watch, responsible for all nuclear power plant operations, in lieu of the ship's Engineer. Supervised a shipboard division.

PUBLICATIONS

SITM 2014

SI-TM: Reducing Transactional Memory Abort Rates through Snapshot Isolation

H. Litz, D. Cheriton, A. Firoozshahian, O. Azizi, J.P. Stevenson, ASPLOS 2014

SpMV on HICAMP 2012

Sparse Matrix-Vector Multiply on the HICAMP Architecture

J.P. Stevenson, A. Firoozshahian, A. Solomatnikov, M. Horowitz, and D. Cheriton, ICS 2012

Winner of Best Paper Award at International Conference on Supercomputing, 2012

HICAMP 2012

HICAMP: Architectural Support for Efficient Concurrency-Safe Shared Structured Data Access

D. Cheriton, A. Firoozshahian, A. Solomatnikov, J.P. Stevenson, and O. Azizi, ASPLOS 2012

CPU db 2012

CPU db: Recording Microprocessor History

A. Danowitz, K. Kelley, J. Mao, J.P. Stevenson, and M. Horowitz, CACM 2012

IR for ChipGen 2011

Intermediate Representations for Controllers in Chip Generators

K. Kelley, M. Wachs, A. Danowitz, J.P. Stevenson, S. Richardson, M. Horowitz, DATE 2011

CPU Co-Optimization 2010

An Integrated Framework for Co-Optimization of Architecture and Circuits

O. Azizi, A. Mahesri, J.P. Stevenson, N. Zhou, S.J. Patel, and M. Horowitz, DATE 2010

PATENTS

Exchange Integrated Order Placement 2024

J.P. Stevenson

Customized Memory Deduplication 2018

C. Egbert, A. Firoozshahian, M. Maddury, J.P. Stevenson, H. Neefs, O. Azizi

Hardware-Assisted Paging Mechanisms 2018

A. Firoozshahian, O. Azizi, C. Egbert, D. Hansen, A. Kleen, M. Maddury, M. Madhav, A. Solomatnikov, J.P. Stevenson

Searchable Hot Content Cache 2016

Omid Azizi, A. Solomatnikov, A. Firoozshahian, J.P. Stevenson, M. Maddury

PROJECTS

Zest – Memory Deduplicator for Linux 2012 – 2016

Using LiME, zest counts duplicates in DRAM memory. Captures a snapshot of physical memory from a live instance of Linux. Performs post-mortem fine-grain deduplication to show the benefit of deduplicated memory systems. Shows that memory capacity is increased by over 2x in many common datacenter applications.

Hash-Stats 2014

Overflow Statistics for Large Hash Tables

Table utilization and table overflows are critical issues for large hash tables. Using published theoretical results, it provides simple scripts to guide the practicing engineer when implementing a large hash table.

https://github.com/etep/hash-stats

Stanford Circuit Optimization Tool 2008 – 2012

Using convex optimization, opimizes digital circuit design for latency and power. Integrates with industry standard tools such as SPICE.

http://github.com/etep/scot

Punch Mobile 2011

Electronic payment processing with integrated consumer loyalty. Provided significant cost savings by disintermediating the credit card payment network using a direct consumer-to-business (C2B) back-end. Voted as top project by VC panel.

SIMD Floating Point Adder 2001

Designed and taped out a fully functional 1x32 / 2x16 bit SIMD floating point adder with IEEE compliant rounding for Stanford independent projects in VLSI, EE-271. Silicon fabricated by TSMC in 0.5μm technology.