(Edited Jan. 3, 2022)

Introduction

In this CAD, you will create the schematics, symbols, & layouts for an inverter, a 2-input NAND gate, & a 2:1 MUX. Then you will perform Design Rule Checks (DRC) & Layout Versus Schematic (LVS) checks on the layouts of all three gates. Finally you will get accurate propagation delays on the 2:1 MUX by extracting parasitic capacitances from the layout and simulating the circuit.

You probably will not use any of these cells in your final project, so don't be concerned about choosing optimal transistor sizes. Try to **minimize area** and use Metal 1, Metal 2, & Metal 3 for routing, but please do not use any higher-level metals. The first two CAD assignments are to be done on your own. You may discuss use of the CAD tools & basic layout concepts with other students, but your design – particularly your layout – should be created by yourself.

INV/NAND2/MUX21

1. Create a directory in your class account called CAD1. All of your files will need to be in this library in order to be graded.
2. Create a library in your CAD1 directory called "CAD1_LIB".
3. Create **schematics** (transistor-level) & **symbols** for the inverter & 2-input NAND
   - Name your inverter "**INV**".
   - Name your 2-input NAND "**NAND2**".
   - Be sure to use pfet/nfet transistors from the library "cmrf8sf".
   - Call the "INV" ports "**IN**" & "**OUT**".
   - Call the "NAND2" ports "**IN0**", "**IN1**", & "**OUT**".
4. Create a **schematic** and **symbol** for the 2:1 MUX by instantiating 3 "NAND2" gates and 1 "INV" (hierarchical design)
   - Name your 2:1 MUX "**MUX21**".
   - Call the "MUX21" ports "**IN0**", "**IN1**", "**SEL**", & "**OUT**".
5. Simulate "INV", "NAND2", and "MUX21" in NCVerilog & verify correct functionality. Test all possible inputs for all 3 gates. Create the input stimulus as you did in Tutorial 1 by editing the testfixture.verilog file to force inputs.
6. Follow the guidelines of Tutorial 1 to create **layouts** for "INV" & "NAND2". Make sure that you use the same names to label the inputs & outputs of the gates in the layout that are used in their symbols.
7. Create the **layout** for "MUX21" by instantiating the layouts of "NAND2" and "INV" gates. Some things to keep in mind:
   - How will you route between 4 cells?
   - How will you place the cells to create a "MUX21"?
   - Where will you place your input and output ports?

For example, you could place all of your cells in a straight line or in a square. **Choose a configuration that minimizes interconnect length. Because this is hierarchical design, the only structures that you may use in the "MUX21" are the cells created earlier in CAD1 ("INV" & "NAND2") & metal1, metal2, metal3, or polysilicon for routing. Try to minimize your use of upper metal layers.**

8. Perform a Design Rules Check (DRC) on each of the layouts of "INV", "NAND2", & "MUX21". DRC reports should be saved automatically under **Calibre/DRC/<component_name>.drc.summary**. If not, please save it.
9. Perform a Layout Versus Schematic (LVS) on each of the layouts of "INV", "NAND2", & "MUX21". LVS reports should be saved automatically under **Calibre/LVS/<component_name>.lvs.report**. If not, please save it.
10. Run PEX to extract the capacitance values for "MUX21" only.
11. Simulate the extracted "MUX21" circuit. Prior to doing this, set the output capacitance to 25fF to represent a realistic load on the output of "MUX21". Find the **propagation delay** (critical path(s) only) of "MUX21".

Requirements

- The layout height & width of any cell should be a multiple of 0.4um. Metals should always be on track, and in the correct orientation. These requirements apply to "INV", "NAND2", & "MUX21", and all future CADs. Please ask if you are unclear with this requirement.
- The schematic & layout for "MUX21" must be created using the hierarchical method.

Submission

Here are some important submission requirements that apply to all CAD assignments. Please read carefully to not lose points over trivial mistakes! Ask your GSI if you are unsure of a requirement.

- Your directory should be named **CAD1**, & you should create a **SUBMIT** directory in your CAD1 directory. Copy all your DRC reports, LVS reports, & simulation waveform files/pictures to the SUBMIT directory.
- Name your README file "README" (not readme, README.txt, etc); README should be in your CAD directory, not in your SUBMIT directory.
- Naming convention for DRC reports: <component_name>.drc.summary
- Naming convention for LVS reports: <component_name>.lvs.report
- Naming convention for SPICE waveforms: spice_<component_name>_<description>.png, where <description> is a brief description of the measurement (e.g. falltime, risetime, falldelay, risedelay)
- Naming convention for NCVerilog waveforms: nc_<component_name>.ps.

Make sure this waveform shows proper digital functionality of your design & explain in the README why this input set was sufficient (i.e. covered all possible input combinations exhaustively)
- In general please do not put any spaces in file names

For CAD1, you need to submit the following:
- "INV", "NAND2", & "MUX21" schematics and layouts in a library called CAD1_LIB.
- Waveform files for all NCVerilog simulations for all three gates.
- Wave .png for the critical path waveform(s) generated by Spectre or HSPICE for "MUX21".
- DRC & LVS reports for all three gates.
- Include a README file containing the full path names for all of the cells the grader is to look at, & any comments you wish to pass on to the grader. Include in the README the maximum rise & fall times for "MUX21". List the nodes between which the rise & fall delays were maximum, what those delays were, & explain why that path was the maximum. Provide a brief paragraph describing any relevant points in your design. Any comments will be taken into consideration when your assignments are graded.

CAD1 FAQs

Q. Recommendations on how to start the layout?
A. Up to you. One way is to start from VSS power line, then place the NMOS, NWELL with PMOSs and VDD. Connect the NWELL to VDD and substrate to VSS and then add the contacts, M1, and poly to route.
- Run DRC constantly so errors do not accumulate
- Don't forget BP on PMOS's and as the substrate contact on VSS
- Don't place BP on NWELL contact to VDD
- Make sure labels in the layout are using the proper metal layer and of the type "lbl"
- Make sure M2 and M3 are on track!

Q. How to define the OUTLINE properly?
A. The outline, as demonstrated in Tutorial 1, is meant to define the cell size. The top and bottom should end at the center of the VDD and VSS lines. On the sides, make sure no metal layers or active region exceed the OUTLINE.

Q. What are metal tracks?
A. All metal layers (except M1) need to be on their corresponding track.
M2, M4… must be centered about X coordinate 0.4um*n + 0.2um (vertical)
M3, M5… must be centered about Y coordinate 0.4um*n + 0.2um, n being an integer (horizontal)

Q. How to show the tracks?
In the bottom left corner of the Layout window, click on the "Grids" tab. Open Grids -> Routing Grids -> select which corresponding metal track you want to view (M2/M3).

Q. Discrepancy is 0 in LVS, but no smiley?
A. Check if VDD and VSS are labeled correctly in the layout.

Q. Getting DRC GR268b
A. Make sure you have put BP layer over your VSS contacts to make the substrate contacts.

Q. After PEX, analog simulation gives the same delay as pre-PEX
A. Make sure you have Calibre written first in Setup -> Environment

Q. Cadence takes a long time to open after typing 'virtuoso &'
A. Delete the *.lck files on the library manager in your home folder. Also delete any panic* files from your home directory.

Q. Running into some other weird error?
A. Could be **many** things, but here are some common trivial mistakes:
Setup issues: Did you use mkcaddir instead of mkdir? Did you create the library from the CIW, & not the Library Manager?
LVS/DRC issues: Do you have BP in all the correct places? Do you have a GRLOGIC box enclosing your entire design? Are your labels on the lbl layer?

Deadline

You must complete CAD1 by **January 12, 2022** by **11pm**.
Do not modify any files in your CAD directory after that time.