(Edited Jan. 4, 2022)

Introduction

In this CAD you will design schematics & layout for a flip-flop (1-bit register) & find its timing characteristics. Your full-custom datapath will require a couple of multi-bit registers & you should design this flip-flop as a bit-sliced component for this purpose. You probably won't use this cell in your final datapath, but this exercise will introduce you to complex leaf-cell design as well as datapath style layout concepts. Note that once again you must work on your own for this assignment.

Sequential Logic

In this CAD, you will design a flip-flop with an asynchronous reset. The ability to asynchronously reset the state of a flip-flop may be desirable for some certain applications, as it will give you faster datapath speed. However, nowadays in common digital designs it is better to avoid sequential logic with asynchronous resets as much as possible and only use synchronous resets, for reasons concerning DFT (design for test) and potential glitching.

Consider a typical gate implementation of a positive edge-triggered master-slave D flip-flop design composed of only NAND gates, shown in Figure 1. This design requires 32 transistors, which is very large. It would also have glitching behavior. Try to understand how this circuit works, even though we will not be using it for this CAD.

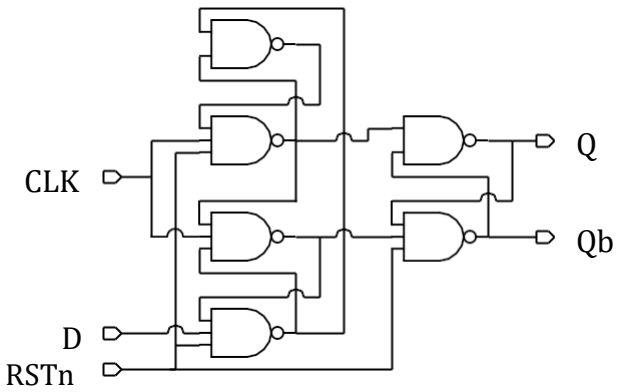

Figure 1: Positive Edge Triggered Flip-Flop Using Logic Gates

Using similar designs to Figure 1 that are more adapted to CMOS technology would result in many fewer transistors. A conceptually simple design to start with is a flip-flop composed of two latches connected in master-slave configuration show in Figure 2 (which is still not being held up as the best design).

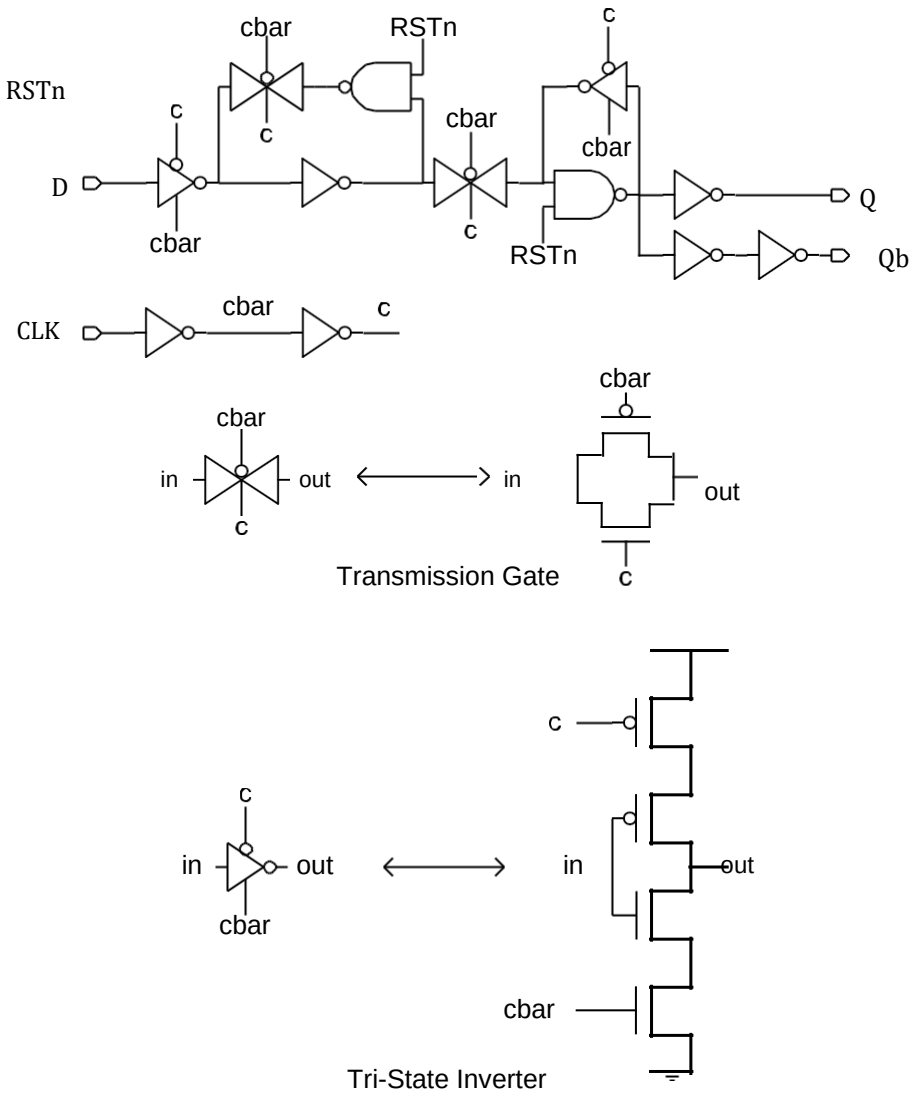

Figure 2: Example of a Static CMOS Transmission Gate Based Implementation D Flip-Flop

How could we improve the flip-flop design even more for performance? As we will see in lecture later on, dynamic or pseudo-dynamic styles with two-phase or single-phase clocking can drastically improve flip-flop speed, but we do not support dynamic design styles in EECS 427 CAD assignments (until the final project).

Layout Considerations

Compared to CAD1, you should pay more attention to the layout aspects of this design. Consider this a bit-sliced component with a target bit-slice width (pitch) of no less than 4um. Having bit-slice widths larger than 8um will likely result in odd aspect ratios for your complete datapath. If the bit-slice pitch is too small (e.g. 2um),

you may find in the future that you don't have enough space to route data buses over the top of the datapath. Your layout must be a flat layout (i.e. no hierarchy). This will result in a more compact layout. On this & all future CAD assignments, we will be looking more closely at your layout density. Note that the clock drivers are included in your cell design in this CAD.

DFF

Schematic Design

Make a directory called CAD2 and do all your work in that directory. Create a library called CAD2_LIB. Create the Flip-Flop shown in Figure 2 called "DFF". Be sure to include an asynchronous reset to zero. Use the following port names: D, Q, Qb, CLK, & RSTn (active low asynchronous reset).

Create a transistor level schematic of the "DFF". Size your gate taking speed, power, & area into consideration. There is no "correct" sizing. What is important is that you make an effort to design the logic & the sizing to optimize your register in some way & that you justify those choices in your README. In particular, please make it completely clear with minimal reading in the README what your design goals were.

Digital Simulation

Run NCVerilog on the "DFF" to exhaustively simulate the various input, state, & output combinations.

Layout & Verification

When implementing the layout of your "DFF", you should keep in mind various layout considerations. While doing DRC & LVS, follow the same procedures as CAD1. Be sure to match the ordering of the inputs in your schematic & layout. Save the DRC & LVS reports in the same format as CAD1.

Analog Simulation

Extract the parasitic capacitances & simulate the "DFF" & obtain the rise & fall CLK-Q delay times as well as the rise & fall setup & hold times. (Exactness is not required for the calculation of setup time, but you should try to get a relatively accurate estimate). Remember to add a 25fF capacitor to the output node to account for the load that the flip-flop may drive. Use the cursors to find your delay estimates. Save an image of your waveforms with the cursors in place that helped you calculate the delay.

Setup time/Hold time measurement

Setup

1. Store a 1 (0) to the flip-flop & allow to settle for one clock cycle.
2. Next clock cycle, change D input >= 0.25 clock cycle **before** rising edge & measure CLK-Q delay (50% CLK -> 50% Q)

3. Run parametric sweeps adjusting D transition later & later – closer to the rising edge of CLK. This will result to an increase in CLK-Q delay.
4. Setup constraint is the time in parametric sweep which causes [roughly] 5% increase in CLK-Q delay (calculated in 2nd step).

Hold

1. Store a 1 (0) to the flip-flop & allow to settle for one clock cycle.
2. Toggle the input at the falling edge of the clock.
3. Toggle D input again >= 0.25 clock cycle **after** rising edge & measure CLK-Q.
4. Run parametric sweep to make D transition (in step 3) earlier & earlier.
5. Hold constraint is the time in parametric sweep which causes [roughly] 5% increase in CLK-Q delay (calculated in 3rd step).

Requirements

- The layout height & width of any cell should be a multiple of 0.4um. Metals should always be on track, and in the correct orientation. These requirements apply to "INV", "NAND2", & "MUX21", and all future CADs. Please ask if you are unclear with this requirement.

Submission

Please refer to the submission guidelines mentioned in the CAD1 assignment, as they apply to all CAD assignments. Do not lose points over trivial mistakes like incorrect file names, etc!

For CAD2, you need to submit the following:

- Schematic and Layout of your "DFF", in the library called CAD2_LIB, in the directory called CAD2
- NCVerilog waveforms showing functional verification of your "DFF" without delay added & with delay added
- SPICE waveforms (post-PEX) for the following:
  - Rise & fall CLK-Q delays
  - Setup & hold times for each (rise & fall)

  Rise/fall delays are measured from the 50% point of CLK to 50% of the Q output transition. You do not have to be exact about the setup time – just get within a few picoseconds.
- DRC & LVS reports
- A README file with the names & paths of all the request files. Briefly describe each simulation in your README file, and discuss any results that are not what you expected. Include a few paragraphs describing your design

& verification rationale. Remember to copy all relevant reports & simulation waveforms to the SUBMIT directory.

CAD2 FAQs

Q. How do I make sure my transistors are in the correct orientation? What is the correct orientation?
A. In your schematic, the convention is your signal should always flow from source to drain. This means for transmission gates, the source of the PMOS should be connected to the source of the NMOS, and the same for the drains. To see the orientation of your transistors, click on the small yellow circle on the terminal you are interested in. On the bottom left hand side of the window, the description for what you selected will show S for source, D for drain, G for gate, or B for body.

Q. Why are all of my simulations wrong even though my schematic looks correct?
A. Make sure all of your transistors are in the correct orientation.

Q. Why is my setup time zero or negative?
A. Make sure you let the stored values settle for one complete clock cycle before running your sweep to find setup time.

Q. Why is my hold time negative?
A. This is actually possible, but just double check to see if you let the stored values settle for one complete clock cycle before running parametric sweep.

Q. Can I have the same label on multiple nodes?
A. No, this is not allowed (unless VSS or VDD). All nodes must be connected physically.

Q. How can I do the layout for a W=160nm transistor given the DRC rules for contacts?
A. Make your transistors dumbbell-shaped, with the active region of the channel area thinner than the active region surrounding your contacts.

Deadline

You must complete CAD2 by **January 19, 2022** by **11pm**.
Do not modify any files in your CAD directory after that time.