# DSD Final Project Scores(MIPS)

**1. Baseline**

(1) Area: 279585.542478 ($um^2$)

```
Number of ports:                          1525
Number of nets:                          22569
Number of cells:                         21588
Number of combinational cells:           17476
Number of sequential cells:               4109
Number of macros/black boxes:                0
Number of buf/inv:                        4045
Number of references:                      145

Combinational area:             167726.883701
Buf/Inv area:                    27781.345869
Noncombinational area:          111858.658777
Macro/Black Box area:                0.000000
Net Interconnect area:         2466159.281036

Total cell area:                 279585.542478
Total area:                     2745744.823515
1
dc_shell>
```

(2) Total Simulation Timeofgiven hasHazard testbench: 5187.65 (ns)

```
ncsim> run
-----------------------------------------------------

START!!! Simulation Start .....

-----------------------------------------------------

FSDB Dumper for IUS, Release Verdi_N-2017.12, Linux, 11/12/2017
(C) 1996 - 2017 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file
*Verdi* : Create FSDB file 'Final.fsdb'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 5187650 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
```

(3) Area*Total Simulation Time: $1.4504\times 10^9$ ($um^2$* ns)

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): 2.3 (ns)

**2. BrPred**

(1) Total execution cycles of given I_mem_BrPred: 385.5

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 385500 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
[b05016@cad29 ~]$
```

(simulation cycle is set to 1 ns)

(2) Total execution cycles of given I_mem_hasHazard: 2462.5

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 2462500 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
```

(simulation cycle is set to 1 ns)

(3) Synthesis area of BPU(Total area of BrPred minus baseline design, two design clock cycle need to be same): 232143.213798 – 230520.499474 = 1622.7143 ($um^2$)

Baseline:

```
Total cell area:          230520.499474
Total area:              2766913.568779
```

BrPred:

```
Total cell area:          232143.213798
Total area:              2792943.078605
```

(both are synthesized with the cycle time of 3.5 ns)

**3. L2 Cache**

(1) Average memory access time: 2.92 (ns)

(2) Total execution time of given I_mem_L2Cache: 1139.75 (ns)

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 1139750 PS + 0
```

**4. MultDiv**

(1) Area of MultDiv (Total area of MultDiv minus baseline design, two design clock cycle need to be same): 296237.035458 – 279585.542478 = 16651.492 ($um^2$)

Baseline:

```
Total cell area:      279585.542478
Total area:          2745744.823515
```

Multdiv:

```
Total cell area:      296237.035458
Total area:          2866463.488674
```

(both are synthesized with the cycle time of 2.3 ns)

(2) Total execution time of given I_mem_MultDiv: 4654.49 (ns)

```
---------------------------- Simulation FINISH !!----------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 4654490 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
```

(3) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): 4.27 (ns)