Hardware Roadmap for QEC-C Implementation

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1 ASIC-Based Hardware Plan

The QEC-C protocol targets a custom ASIC for low-power quantum control.

1.1 Architecture

- **Core Unit**: Feedback loop processor with 5–20 qubit channels. - **Power Consumption**: 3–5× lower than surface code (target 50 W for 20 qubits). - **Latency**: <10 ns per correction cycle.

1.2 Roadmap

- **Phase 1 (2025)**: Design and simulate ASIC layout. - **Phase 2 (2026)**: Fabricate prototype with 5-qubit support. - **Phase 3 (2027)**: Scale to 20 qubits with full QEC-C integration.

2 Performance Metrics

- Qubit efficiency: 9–25× reduction. - Control fidelity: >99.99% with active feedback.