Name

HOMEWORK 2A / EE 201L

FALL 2012

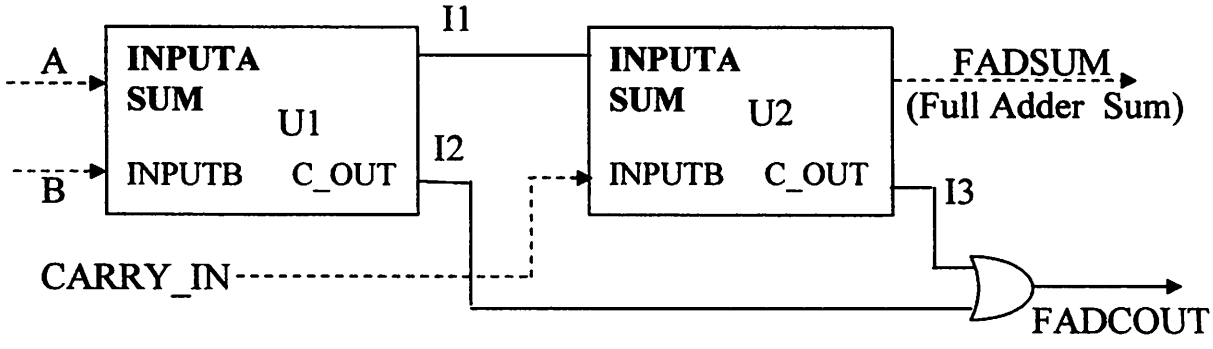
Verilog Fundamentals

Morning	
Afternoon	

1) Assume that you already wrote the module

HALFADDER (INPUTA, INPUTB, SUM, C_OUT)

Now write a FULLADDER Verilog module corresponding to the circuit below, instantiating HALFADDER module. Include plenty of comments to earn full credits and also all necessary declarations.



2) What is the value of reg [15:0] VarX , when VarX is assigned the following :

16'H7A becomes :

8'Bx10 becomes :

'O71 becomes :

9'Oz5 becomes :

3) →The declaration below sets up an array consisting of . . . . . members, each member is . . . . –bit long. Within each member bit # . . . is MSB.

reg [0:7] mem8x256 [0 :255]

→ What us a ***Reduction operator*** ? List at one application . . . . . .

. . . . . .

. . . . . .

→ Show your work / ~^ 1 1 0 0 1 1 1 0 becomes :

→ Given **a** = 4'B1z0x and **b** = 4'B1z0x

a == **b** evaluates to :

a != **b** evaluates to :

→ Given the following codes:

```
reg [ 15:0 ]  VarX ;
wire [15:0] Z ;
VarX  =  – 4'D12 ;
   ————————
   ————————
assign  Z =  VarX / 3
```

What value (in decimal) does **Z** evaluate to ? Show your work, step by step.