The Voting Machine

1. Synopsis:

In this lab we will build a simple logic circuit of a voting machine using TTL gates using integrated circuits that contain one or more gates packaged inside. The objective of the lab is to familiarize ourselves with the electrical characteristics of TTL chips and proper ways to connect inputs and outputs to these gates.

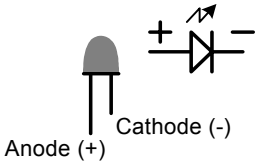
2. Terminology:

2.1 Floating inputs:

One of the terms used for describing unconnected inputs is *floating* inputs. Other terms frequently used are *hanging* inputs and *dangling* inputs.

2.2 Light Emitting Diode:

A light emitting diode (or, LED for short) requires approximately 0.7V of potential difference and 10mA of current across its terminals to glow properly. Also, the LED will only glow only if the potential at the anode (positive terminal) is higher (by at least 0.7V, usually about 1V) than the potential at the cathode (negative terminal). Usually the longer leg of an LED is the positive terminal. Also, if you look carefully at the two terminals in the plastic packing, the fatter terminal is the cathode. (Prelab Q 4. 1:)



3. Theory:

3.1 Floating inputs in TTL circuits:

In most TTL devices, a floating input is treated as HIGH or logic 1. Hence, the common notion that a floating input is a logic 0, is wrong (Prelab Q 4. 2:). In digital systems, a floating input can not be treated as a zero. It is either a HIGH, as in the case of most TTL devices, or UNDEFINED (ambiguous) as in the case of CMOS devices (and TTL devices of some families). Further, in the case of CMOS devices, floating inputs can actually damage the circuit due to electrostatic voltage on the floating input. Therefore, it is always desirable (and more or less required) to connect the unused inputs to an appropriate level, GND or 5V. (Prelab Q 4. 3:)

3.2 Current requirements for TTL gates:

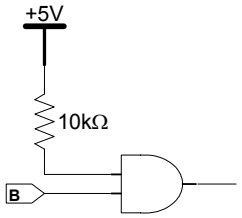
In digital circuit design, we need to be careful about the electrical characteristics, and the current specifications in particular, of the gates being used. For example, if a TTL gate is being used to drive an LED, we have to make sure that the current driving capabilities of the TTL gate exceed the current requirements of LED. Similarly, if a switch or another gate is driving the inputs of a TTL gate, then the switch (or the driver, in general) shall be connected in such a way as to satisfy the current requirements at the input of the TTL gate. These two issues will govern the way we connect LEDs and switches to TTL gates in this experiment.

3.3 Connecting inputs:

Recall from Ohm's law:

$$I = \frac{V}{R}$$

where, V = Voltage (in volts), I = Current (in amperes), and R = Resistance (in Ohms)



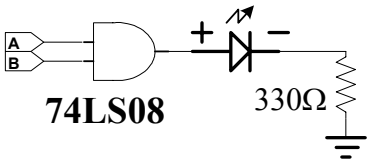
If we need to connect one of the inputs of a TTL gate (let's say, a 2-input AND gate) permanently to logic 1, we should connect it to a +5V power supply through a 10kΩ resistor, as shown in the figure to the right. This resistor limits the amount of current flowing into the TTL gate to about 0.5mA.

3.4 Connecting outputs:

When a gate is producing a HIGH output (logic 1), it can *source* (send out) certain amount of current. It is called its *sourcing* current capability (I_{OHmax}). Similarly, when a gate is producing a LOW output (logic 0), it can *sink* (suck in) certain amount of current. This is called its *sinking* current capability (I_{OLmax}). It is common for us to assume that all devices operate in a symmetric way but in reality, among bipolar TTL gates (say 74LS series), I_{OH} is far lower than the I_{OL}. For example, the snapshot of the datasheet provided in Appendix II of this handout shows I_{OH} for 74LS10 as 0.4mA and I_{OL} as 8mA. Hence, to drive an LED, instead of using the meager sourcing capability of a TTL gate, we use its much higher sinking capability. Please note that some gates are described as "buffers" which have 3 times the current drive capability of an ordinary gate. However, the sourcing current of even a buffer (for example, 74LS37 2-input NAND) is only about 1.2mA which is far lower than the 8mA sinking current of an ordinary gate.

Let us show how to connect an LED through an example.

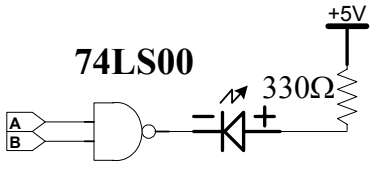
Suppose you wanted to make a simple circuit such that an LED glows when two inputs A and B are both HIGH. The circuit to the right is the intuitive way to implement this design.



In the circuit shown above, the AND gate is *sourcing* the current when it is in the ON state. We know that the amount of current needed by the LED to glow brightly is approximately 5 to 10mA. If the AND gate can not provide 10mA of current, the LED will not glow brightly. Also, this may burn the chip after a few hours. For these reasons, this design is not recommended.

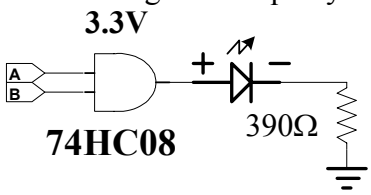
A better way to implement the same functionality is shown below:

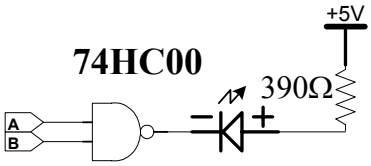
In this circuit, the LED still glows when both A and B are HIGH, but the TTL gate is serving as a *sink* of the current when the LED is glowing. The power supply is acting as a source, supplying the current to make the LED glow, through the 330Ω resistor. This (sinking method) is the preferred method of connecting LEDs to TTL circuits. The 330Ω resistor here is called a *current limiting series resistance* as limits the amount of current that sinks through the gate to near the I_{OL} range.



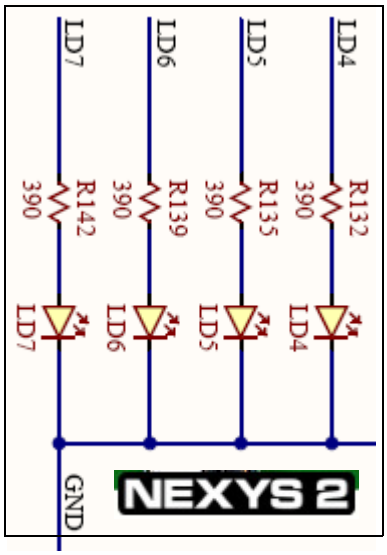
IOH is much smaller than IOL only in bipolar TTL gates such as 74LS series gates. In gates using CMOS logic (such as 74HC series gates) and in VLSI chip such as the Xilinx FPGA (Spartan 3E) on the Nexys 2 board, which is internally made using CMOS Logic, the IOH and IOL are symmetric.For example, the 74HC/74HCT gates have an Io of +4mA/-4mA.

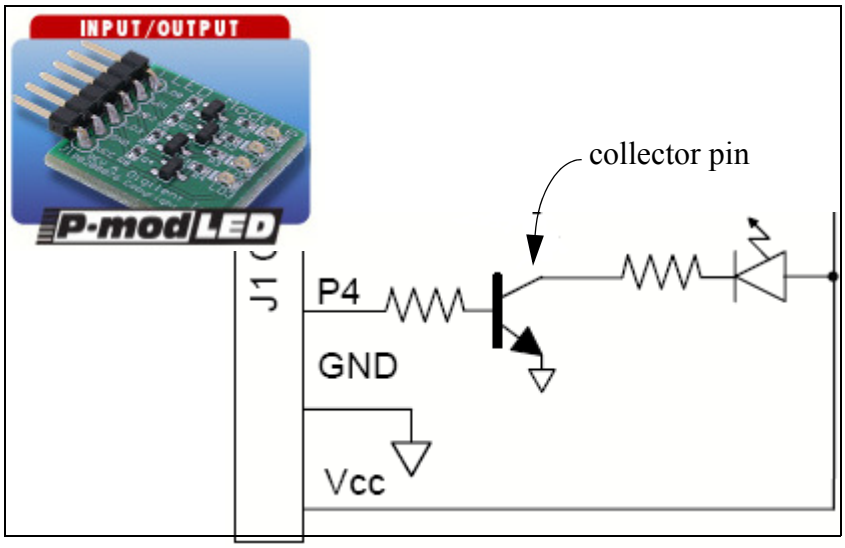
So, when it comes to driving load like a *small* LED requiring about 4 mA, one can use sourcing mode or sinking mode equally well.





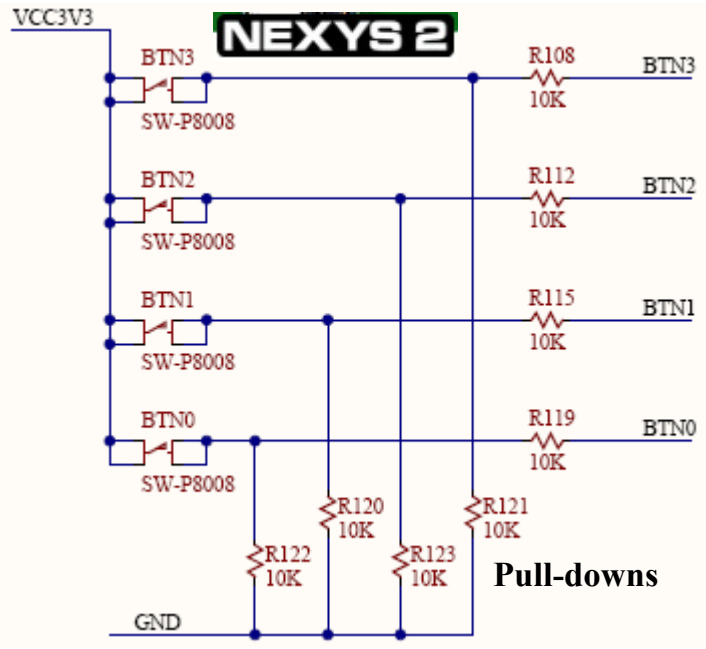
On the Nexys 2 board, sourcing mechanism is used to drive the small LEDs where as in the LED peripheral module Pmod-LED, they used an additional bipolar npn transistor to drive the LEDs in effectively sinking mode. The single transistor is in a way acting like a open-collector inverter.





The input currents in the case of CMOS circuits are called leakage currents and they are very small in magnitude compared to the input currents in TTL gates.They are also symmetric (example: I_I = +1uA/-1uA). Hence both pull-up and pull-down methods are possible in the CMOS unlike in TTL. Hence both method #1 and method #2 on the next page will work for CMOS gate inputs.

You see that the buttons on Nexys-2 board are connected to the Spartan FPGA using method #1 as shown on the side.

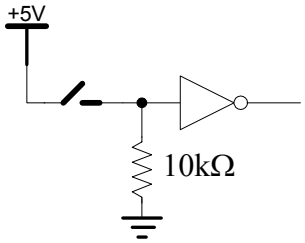


4. Prelab:

Q 4. 1: If you were given an LED whose both legs were cut equal, how would you determine which is the positive terminal? (5 points)

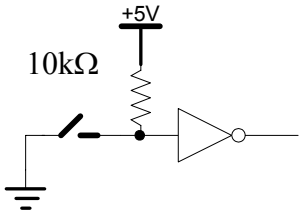
Q 4. 2: Which of the following four switch configurations can produce two distinct levels (HIGH and LOW) at the output corresponding to the two positions (Open and Close) of the switch if the inverter is 74LS04? Which method is preferable?
Answer the same questions if the inverter is 74HC04 or 74HCT.
Note: CMOS inputs shall never be left floating. (10 points)

Method 1



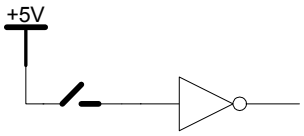
Is this configuration workable?
Is this configuration preferred?

Method 2



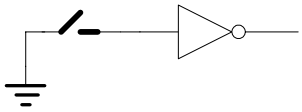
Is this configuration workable?
Is this configuration preferred?

Method 3



Is this configuration workable?
Is this configuration preferred?

Method 4



Is this configuration workable?
Is this configuration preferred?

Q 4. 3: Suppose you wanted a 2-input AND gate but only a 4-input AND gate was available. How could you use the available gate for your purpose? What if the required gates was a 2-input NOR gate and the available gate was a 4-input NOR gate? In either case, could you leave the remaining two inputs ***floating***? In the figure below connect the unused inputs of the available gates to appropriate voltage levels and explain if the unused inputs can/can not be left floating. (10 points)

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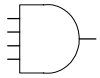
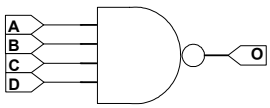
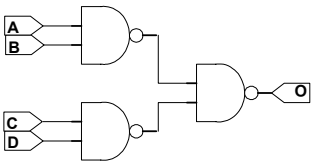
Required	Available	Explanation
		
		

Q 4. 4: Suppose in a certain circuit a 4-input NAND gate was needed but due to shortage of 4-input NAND gates in the lab, Mr. Bruin (a dumb character you will encounter throughout this lab manual) replaced this 4-input NAND gate with three 2-input NAND gates in the following manner. (15 points)

Original design



After Mr. Bruin's Modification



- ❑ Yes the original and the modified designs are functionally same.
- ❑ No, Mr. Bruin's design is not equivalent to the original circuit

(a) Proof using boolean algebra:
(Hint: Use De-Morgans laws to manipulate the expressions. Generate 2 obviously unequal statements.)

(b) Graphically perform the SAME calculation you did above using bubble-pushing:

5. Procedure:

Goal: To build a voting machine.

Four people are required to vote on an issue. Each of them has a switch which gives a HIGH signal if the person votes “yes”, and a LOW signal if the person votes “no”. An LED will light up if the majority of them are in favor of the measure (i.e., at least three out of four vote “yes”).

5.1 Experiment and learn connecting a switch to a TTL gate. Build each of the four circuits in Prelab Q 4. 2:, using 74LS04 and note the output voltages when the switch is turned ON and when the switch is turned OFF. Then build the first two circuits using 74HC04 or 74HCT. Fill out the form in report Q 6. 1:. Check your answer with the Prelab Q 4. 2:

5.2 Derive a simplified boolean expression (in the Sum of Products form) for the output of the voting machine. (Report Q 6. 2:)

5.3 Draw an implementation (circuit diagram) of the voting machine using AND gates and OR gates. (Report Q 6. 3:)

5.4 Draw an alternate implementation using only NAND gates (NAND-NAND implementation). (Report Q 6. 4:)

You perhaps have the following items in your lab kit #A (this lab kit will be used in this experiment and perhaps another):

74LS04 (1), 74HC04/74HCT04 (1), 74LS10/74HC10/74HCT10 (2),
330Ω resistor (1), LED (1), 4 Switches in DIP (Dual in-line package), 10kΩ resistors(4)

5.5 Notice that we did not give you a 4-input NAND gate. **Using 3-input NAND gates and inverters arrive at a multi-level (more than 2 levels) implementation for the voting machine**. Using the pin-out information for the 74xx10 NAND gate chips and 74xx04 inverters (available in the “component list” or at www.ti.com), label this circuit diagram with appropriate pin number for each input and output. Also, add the circuitry for the switches and the LED to have the complete schematics of the desired circuit. Note that for simplicity sake, we will first connect the LED in the sourcing mode. Also, **connect the switch using the preferred configuration from the prelab exercise**. (Report Q 6. 5:)

5.6 Now, we are ready to start wiring the circuit. Connect Vcc and GND pins of each of the chips to +5V and ground, respectively.

5.7 Connect the gates using the circuit diagram from step 5.5. Be sure to verify how the DIP switch is internally connected. Ideally, when the switch is open, the resistance between the two terminals should be infinitely high (or, very high) and when the switch is closed, it should be zero. Note down the observed values of these resistances in the report section. (Report Q 6. 6:)

5.8 Apply various input combinations to test your circuit and show it to your TA in the end.

5.9 Use the multimeter to determine the amount of current flowing through the LED and the potential difference across. (Report Q 6. 7:)

6. Lab Report:

Name:_____	Date: _____
Lab Session:_____	TA's Signature: _____

For TAs: Prelab (out of 40): _____ Hardware (out of 40): _____ Report (out of 20): _____
Comments:

Note: **DO NOT forget** to write **units** with the quantities measured.

Q 6. 1: Build the circuit in Prelab Q 4. 2: and fill in the form below.

	Voltage (V) (**74LS04**)		Voltage (V) (**74HC04**)	
	Switch is On	Switch is Off	Switch is On	Switch is Off
Method 1				
Method 2				
Method 3			XXXXXXXXX	XXXXXXXX
Method 4			XXXXXXXXX	XXXXXXXX

Q 6. 2: Simplified boolean expression for the Voting machine:

Q 6. 3: AND-OR implementation of the Voting machine design.

Q 6. 4: NAND-NAND implementation of the Voting machine design.

Q 6. 5: Draw the circuit using the chips provided in the lab kits, plus the connections with the switches and the LEDs. label the chips and add pin numbers.

Q 6. 6: Switch: Resistance when OPEN: _____

Resistance when CLOSED_____

Q 6. 7: LED: Exact Resistance of the 330Ω (nominal 330Ω) resistor measured on the multimeter: _____

Sourcing mode: Voltage drop across 330Ω resistors_____

Current (calculate by Ohm's law):_____

Voltage drop across LED:_____

Sinking mode: Voltage drop across 330Ω resistors_____

Current (calculate by Ohm's law):_____

Voltage drop across LED:_____

Appendix I: Datasheet 74LS10

Following is a portion of the datasheet of one of the ICs we will use in this experiment, 74LS10. To view the entire datasheet, please visit: www.datasheetarchive.com and search for 74LS10.

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DM74LS10

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			–0.4	mA
I_{OL}	LOW Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

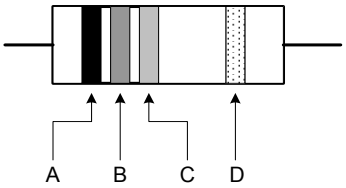
Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA			–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			–0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	–20		–100	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		0.6	1.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		1.8	3.3	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Appendix II: Color Coding of Resistors

In order to find the nominal resistance of a leaded resistor, hold the resistor as shown in the figure. Color band "D" is different from A, B and C, as it is typically either Silver or Gold in color. The nominal resistance is given by the equation:



$$\text{Resistance} = AB \times 10^{C}$$

The numerical value corresponding to each color in the band A, B and C is given in the table below:

Color	Number value
Black	0
Brown	1
Red	2
Orange	3
Yellow	4
Green	5
Blue	6
Violet	7
Grey	8
White	9

A Gold color band D represents 5% deviation (or tolerance) of the actual resistance value from the nominal value. A Silver band represents 10% tolerance. If there is no D band (gold or silver) then the tolerance is 20%.

Tip: Following web site has an interesting graphical tool that can be used to find the nominal resistance for leaded resistors: http://www.engplanet.com/content/resistorinfo.html

Since it is hard to remember the order of the colors, some people memorize the acronym **BBROYGBVGW** made up of the first letters of the ten colors and many others remember a mnemonic such as **"B**ig **B**oys **R**ace **O**ur **Y**oung **G**irls, **B**ut **V**iolet **G**enerally **W**ins".

Red Green Orange Gold

Resistance = _____