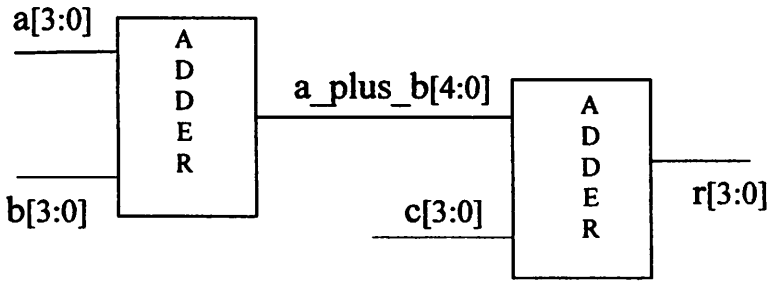
Name:

EE 201L - HOMEWORK IIB

FALL 2012

Morning
Afternoon



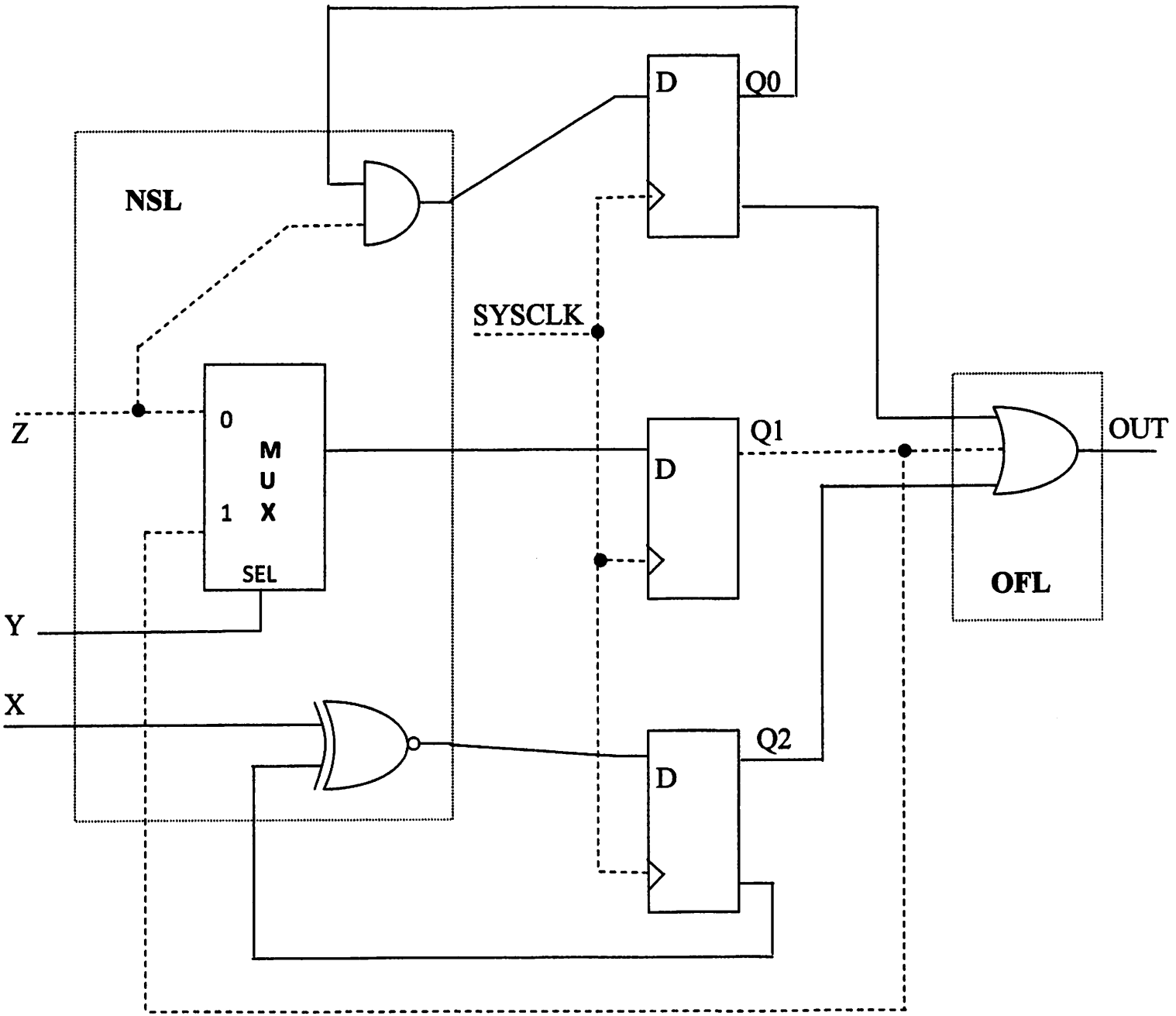
1) Does the following code correctly describe the circuit above? If not, find and correct at least ten mistakes.

```
module (a,b,c, r)
        Input   [3:0] a, b, c ;    output [4:0] r ;
        wire  [5:0] r ;
        reg  [4:0] a_plus_b ;

         always @ (a, b)
         begin ;
              a_plus_b <= a + b ;
              r <= a_plus_b + c ;
         end

endmodule ;
```

2) Write the Verilog codes corresponding to the circuit below. Stop at the end of compilation, because it represents nothing. Do not execute your program. This is an exercise in program writing. The dashed lines in the diagram facilitate your reading. They do not differ from the solid lines.


NSL
D
Q0
SYSCLK
Z
0
M
U
1
X
SEL
Q1
D
OUT
OFL
Y
X
Q2
D