Project 1 - CSCE 313

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1.0 – Nios II/f

Table 1.0	**Value**
Logical Elements:	3,038 / 114,480 (3%)
Total Registers:	1806
Total Pins:	2 / 529 (<1%)
Memory Bits:	604,672 / 3,981,312 (15%)

2.0 – Nios II/e

Table 2.0	**Value**
Logical Elements:	1,619 / 114,480 (1%)
Total Registers:	866
Total Pins:	2 / 529 (<1%)
Memory Bits:	535,552 / 3,981,312 (13%)

3.0 – Nios II/f: 4KB Instruction Cache, 16KB Data Cache

Table 3.0	**Value**
Logical Elements:	3,065 / 114,480 (3%)
Total Registers:	1804
Total Pins:	2 / 529 (<1%)
Memory Bits:	705,024 / 3,981,312 (18%)

4.0 – Comparison: Table 1.0 and Table 2.0

Table 1.0 displays information using the version Nios II/f of the Nios II processor and Table 2.0 displays information using the version Nios II/e of the Nios II processor. Table 1.0 has higher values for the variables Logical Elements, Total Registers, and Memory Bits. However, both tables have the same number of pins, 2. Changing the version of the processor to Nios II/e ultimately reduced the values as Table 2.0 has over 1000 fewer Registers and 2% fewer Logical Elements and Memory Bits.

5.0 – Comparison: Table 1.0 and Table 3.0

Table 1.0 displays information using the version Nios II/f of the Nios II processor and Table 3.0 displays information using version Nios II/f with the data cache set to 16KB and instruction cache set to 4KB. The tables have very similar values. Table 3.0 has only 27 more Logical Elements, 2 fewer Registers, and 100,352 more Memory Bits. Both tables also have the same number of pins, 2. Changing the Nios II Cache Configuration for data cache from 4KB to 16KB has the effect to increase the number of memory bits as Table 3.0 has 3% more memory bits.

6.0 – Adding a Welcoming Message