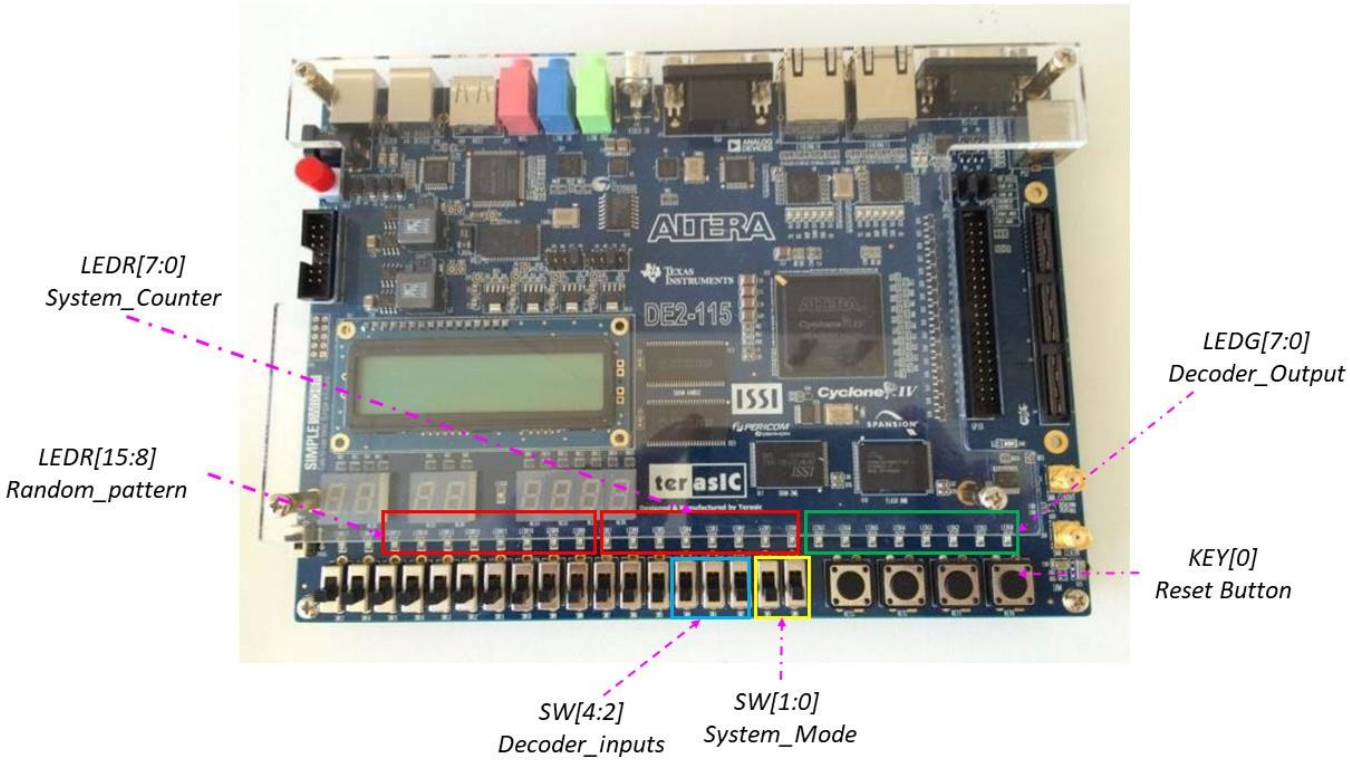
Project Objective

The main purpose of this project is to learn how to use the parallel I/O devices in embedded systems and how to use the PIO functions in your application software. The figure below shows the parallel I/O devices that you are required to add into your system.



Project Requirements

a. Make sure that both data and instruction cache of NIOS processor are set to **4KB** and Nios2 version is **Nios II/f.**

b. Add the five PIO components which are shown in the following table and specify their features as in the table. The first column shows that I/O pins that will be used in the Verilog code and connected with the exported signal of your nios system. The second and third columns show the PIO direction and width respectively that you need to specify when you select the component from IP

Catalog. The fourth column shows the name that you need to rename the component with when you add it to your nios system. The fifth column shows the signal name that will be exported in the conduit signal.

PIO board device	Direction	Width	name	Conduit name
SW[1:0]	Input	2-bit	System_modes	modes
SW[4:2]	Input	3-bit	decoder_input	dinput
LEDG[7:0]	Output	8-bit	decoder_output	doutput
LEDR[7:0]	Output	8-bit	System_counter	counter
LEDR[15:8]	Output	8-bit	random_pattern	pattern

c. Connect the new added components to nios processor and clock source as you connected JtagUart component in Project1.

d. The Verilog code with the update is attached with the assignment in blackboard. Keep in your mind, if you use different naming for your nios system (qsys) components, you must match the names in your Verilog code.

e. **Notes:**

1. Any time the mode value changes to another value, all the system LEDs turn OFF and then display the new values based on the new mode value.

2. A C template of the application code is attached with assignment in blackboard. You may use it as a reference when you write the software

f. You are required to write an application software that executes the following functions based on the values of the system mode as explained in the table below.

System Mode	SW [1:0]	Function
0	00	Both red and green LEDs light
1	01	A counter starts incrementing from 0 to 255, and the value is displayed on Red LED [7:0]. If the mode changes, the counter stops on latest number If the mode changes back to 1, the counter restarts.
2	10	A random pattern starts is displayed on Red LED [15:8]. If the mode changes, the pattern stops on latest value
3	11	Decoder is enabled. The decoder output is displayed on Green LED [7:0] based on the decoder input, SW [4:2].

Project Report (50%)

The project report will be graded out of 100, and the points will be distributed as following:

a. **Professional preparation** (10 points):

You are required to submit a typed document with text of the paragraphs in Times New Roman 11 pt font, clear and grammatically well-formed explanations, page numbering and document heading numbering (1.0, 2.0, 3.0, etc to identify the required sections listed below).

b. **Report Content** (90 points):

1.0 (*20 points total, each value is 5 points*) After you compiled and synthesized your system, read the summary report from Quartus, and fill out the below table with the numbers from the report.

Logical Elements	Registers	Total Pins	Memory Bits

2.0 (*30 points*) Briefly, compare the hardware results between the table above and Table.1 of project 1.

3.0 (*40 points, each picture is 10 points*) Run the application software on the four different mode values and include a picture that shows the output on the console for each case. You are required to submit only one picture per case.

Project Demo (50%)

- The main purpose of the demo is to test your project functionality and execution.
- Demos will be checked and graded by the TA
- Demos will be graded out of 100, but worth 50% of total project grade
- Both partners must show up in that day. If a member didn't show up, he/she receives 0 unless an excused absence was provided.
- Demos will be conducted during the lab time on the following dates:
  - **Section 001**: Wed. Feb 16 or Wed Feb. 23
  - **Section 002**: Fri Feb 18 or Fri Feb. 25
  - Demo dates will be decided by the groups
- Below are how the demo points will be distributed

Tasks	Point
LEDs lights when mode = 0	/20
Random pattern	/20
Counter	/20
Decoder	/20
Answering questions (students in a group might have different questions)	/20

Project Submission

1. Save the project report as **r2_username1_username2.pdf**, username of both students in the group.
2. Submit the entire project directory which includes quartus project, software folder and the report. For submission, you can watch video (**F**) in Module1/Labs.
3. Create a zip of the project working directory and name it as **p2_username1_username2**
4. **Only one attempt** is allowed
5. **Only one group member** submits the project
6. **Remember:** Any grade dispute must be raised within one week of the grade posting.