

Ethan Syed

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Portfolio: <https://ethansyed.github.io/portfolio/> | <https://github.com/ethansyed>

EDUCATION

University of Texas at Austin – Austin, TX

Bachelor of Engineering, Electrical and Computer Engineering | Minor - Entrepreneurship

May 2025

GPA: 3.17

Relevant Coursework: Computer Architecture, Digital Logic Design, Embedded Systems, Compilers, Algorithms, Software Design, Circuit Theory, Linear Systems & Signals

WORK EXPERIENCE

Stryker

Post-Market Quality Engineering Intern;

May 2023 - August 2023

Flower Mound, TX

- Measured and analyzed signal integrity of medical hardware with an oscilloscope and external power supplies
- Automated testing of display components using Python scripts, SNMP enabled devices, and IP cameras
- Increased testing throughput by 100%; doubling the number of components able to be tested simultaneously
- Created a full-stack web app to act as a local repository of historically addressed service cases

Mavencode

Software Engineering Intern;

June 2021 - August 2021

Southlake, TX

- Designed full-webpages, data entry components, search bars, and card arrays in React using Typescript
- Developed API methods to integrate with back-end with the use of JavaScript
- Integrated AWS and Google Cloud connections into server/team management within product
- Increased code throughput by approximately 20% and exceeded deadline expectations by one week

PROJECTS

Little Computer 3 Byte-Addressable Simulator

- Designed and created a pipelined byte-addressable computer in C given the LC3-b ISA
- Programmed microcode signals using state and dataflow diagrams to emulate data path components
- Created microarchitectural support for caches, virtual memory, interrupts, exceptions, and branch predictions

Zombie Invaders Microcontroller Game

- Utilized C and ASM to create a “Space Invader” game on a TM4C microcontroller
- Read from and wrote to register files to service input devices and interrupt service routines (ISRs)
- Programmed game features and textures in C and display firmware in ASM

FPGA Up and Down Timer/Stopwatch

- Programmed a Xilinx basys3 board in Verilog to function as an up and down counter
- Implemented switch input to load numbers and displayed status on seven-segment displays

EXTRACURRICULARS / AWARDS

Texas Crew – Novice rower on an eight-person team

August 2023 - Present

IEEE Member

August 2021 - Present

Machine Learning & Data Science Member

August 2021 - Present

Richard Greene Scholar – Recipient of \$10,00 Scholarship

February 2020 - Present

SKILLS -

Technical: RTL and Digital Logic Design, Vivado, LTSpice, Multisim, Linux/Unix

Languages: C, C++, C#, Python, Verilog, ARM ASM, SQL, MATLAB, Java, Typescript,

Frameworks: Node.js, PyTorch, Pandas, ReactJS