Document: AV-SIM-HW-V1.0

Title: Avionics Simulation System Hardware Configuration & Bus Architecture

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1. System Overview

The AV-SIM hardware layer uses a modular, distributed architecture connected via a primary data bus for command and telemetry exchange.

2. Communication Bus Architecture

The primary system communication is managed by the **MIL-STD-1553B** avionics data bus. This bus operates in a Command/Response structure.

Parameter	Value	Notes
Protocol	MIL-STD-1553B	Dual-redundant bus, 1MHz clock rate.
Message Size (Max)	32 Words (32 x 16-bit)	Used for FDM updates and Control Surface Commands.
Bandwidth Utilization	75%	Maximum utilization allocated for real-time traffic.
Calculated Bus Throughput (Maximum Effective Cycle Rate)	50 Hz	Achieved by scheduling 3 core data transfers per cycle.

3. Core Processing Units

3.1 Flight Control Processor (FCP) Module

The FCP is responsible for running the simulated flight control laws.

- **Architecture:** The FCP utilizes a **Dual-Channel Processor (DCP)** configuration where two identical processing nodes run the control laws in parallel and compare outputs before commanding the actuators.
- **Components:** Two ARM Cortex-A72 cores per node.
- **Function:** Accepts sensor inputs from the bus and calculates actuator outputs.