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CS M151B HW7

5.5 1) Offset is 5 bits

Cache block size = 2^5 bytes = 32 bytes

With word size as 4 bytes, the block size is **8 words**

2) Index is 5 bits

The cache has 2^5, or **32 entries**

3) Let's assume there is 1 valid bit for each tag

For each block (8 words) we have:

- (8 words) × (32 $\frac{\text{bits}}{\text{word}}$) = 256 data bits
- 22 tag bits
- 1 valid bit

Total bits for one block: 256 + 22 + 1 = 279 bits

$$\frac{\text{Total bits for implementation}}{\text{Data Storage Bits}} = \frac{279}{256} = 1.089$$

4)

Address	Index	Offset	Hit/Miss	Replace?	Final Value?
0	00000 ×	00000 ¹	M	N	N
4	00000 ×	00100 ²	H	N	N
16	00000 ×	10000 ³	H	N	N
132	00100 ⁴	00100 ⁵	M	N	N
232	00111	01000	M	N	Y
160	00101	00000	M	N	N
1024	00000 ×	00000 ¹	M	Y	N
30	00000 ×	11110 ³	M	Y	N
140	00100 ⁴	01100	H	N	N
3100	00000 ×	11100 ²	M	Y	Y
180	00101	10100	H	N	Y
2180	00100 ⁴	00100	M	Y	Y

5) There were 12 total references
There were 4 hits.
4/12 = 0.33 hit ratio

6) {00100, 0010, mem(2176)}
{00101, 0000, mem(160)}
{00000, 0011, mem(3072)}
{00111, 0000, mem(224)}

1157 5.10

Main Memory: 70ns 36% of instructions

	L1 Size	L1 Miss Rate	L1 Hit Time
P1	2KB	8%	0.66ns
P2	4KB	6%	0.90ns

1) P1: $\frac{1}{0.66}$ = **1.515 GHz**
P2: $\frac{1}{0.90}$ = **1.11 GHz**

2) AMAT = Hit Time + (Miss Rate × Miss Penalty)
P1: 0.66ns + (0.08 × 70ns) = **6.26ns**
P2: 0.90ns + (0.06 × 70ns) = **5.1ns**

3) TCPI = BCPI + $\left[\frac{\text{Memory Access Time} \times \text{Miss Rate}}{\text{Hit Time}}\right]$ × Percent of Memory Instructions
(the bracketed term = MCPI)

P1: $1.0 + \left[\frac{70 \times 0.08}{0.66}\right] \times 0.36$ = **4.05**
P2: $1.0 + \left[\frac{70 \times 0.06}{0.90}\right] \times 0.36$ = **2.68**

4) AMAT with L2: L1 hit time + L1 Miss Rate × [L2 Hit Time + (L2 Miss Rate × Miss Penalty)]
P1: 0.66ns + 0.08 × [5.62ns + (0.95 × 70ns)] = 6.43ns
The AMAT is slightly worse with the additional L2 cache

5) BCPI + (# of instructions) × $\left[\frac{\text{L1 Miss Rate} \times (\text{L2 Hit Time} + \text{L2 Miss Penalty})}{\text{L1 Hit Time}}\right]$

$1.0 + 0.36\left[\frac{0.08 \times (5.62 + 0.95 \times 70)}{0.66}\right]$

= 4.15

TCPI = 4.15

6) $1.0 + 0.36\left[\frac{0.08 \times (5.62 + x \cdot 70)}{0.66}\right] < 4.05$

$x < 0.918$ Miss rate would have to be less than 91.8%

7) $1.0 + 0.36\left[\frac{0.08 \times (5.62 + x \cdot 70)}{0.66}\right] < 2.68$

$x < 0.470$ Miss rate would have to be less than 47%

5.12.1) First Level Only

TCPI = BCPI + MCPI

= BCPI + (L1miss × main memory access)

= 1.5 + (0.07 × 100) × 2GHz

= 1.5 + (0.07 × 200) = 15.5

Main memory doubled

= 1.5 + (0.07 × 200) × 2GHz

= 1.5 + (0.07 × 400) = 29.5

Second Level Direct Mapped

TCPI = BCPI + MCPI

= BCPI + (L1miss × L2access + L2miss × Main memory access)

= 1.5 + [(0.07 × 6 ns) + (0.035 × 100ns × 2GHz)]

↑ 12 cycles, 2GHz

= 8.92

Main memory doubled

= 1.5 + [(0.07 × 6) + (0.035 × 200ns × 2GHz)] = 15.92

Second level 8-way set associative

TCPI = BCPI + MCPI

= BCPI + (L1miss × L2access + L2miss × main memory access)

= 1.5 + [(0.07 × 14ns) + (0.015 × 100ns × 2GHz)] =

↑ 28 cycles, 2GHz

= 5.48

main memory doubled

= 1.5 + [(0.07 × 14ns) + (0.015 × 200ns × 2GHz)] =

= 8.48

2) TCPI = BCPI + MCPI

= BCPI + (L1miss × L2miss × L3access + L3miss × main memory access)

= 1.5 + (0.07 × 0.035 × 25ns) + (0.13 × 100ns × 2GHz)

↑ 50 cycles, 2GHz

= 27.56 - this is slower! L3 has a high miss rate

advantage

- can be more efficient if implemented well, might lower CPI as there are fewer memory access

disadvantage

- complex cache structure
- more complicated hardware requirements
- increased cycle time

3) 512 KB 4% miss rate

additional 512KB lowers miss rate 0.7%.

50 cycle access time

Use equation from second level direct mapped

TCPI = 1.5 + [(0.07 × 25) + (x · 100 · 2) = 8.92

↑ 50 cycles, 2GHz

x = 0.0283

miss rate must be 2.8%

We need to increase by 512KB twice them, to decrease miss rate to 2.6%.

Thus the cache must be 1536 KB large