```
0
                                                                                                                                     M
                                                                                                                                     ×
                                                                                                          Add ALU result
          Add
                                                                                               Shift
                                                                                               left 2
                                                            RegDst
                                                            Branch
                                                            MemRead
                                                            MemtoReg
                              Instruction [31-26]
                                                   Control
                                                            ALUOp
                                                            MemWrite
                                                            ALUSTC
                                                            RegWrite
                                                                                                                                                                        00
                              Instruction [25-21]
                                                             Read
Read
                                                             register 1
                                                                              Read
address
                                                                            data 1
                              Instruction [20-16]
                                                             Read
                                                                                                                Zero
                                                             register 2
            Instruction
                                                                                                                      result[0
                                                   0
                                                                   Registers Read
                                                                                                          ALU
                                                                                                                ALU
               [31-0]
                                                                                                0
                                                                                                                                               Read
                                                   M
                                                             Write
                                                                            data 2
                                                                                                               result
                                                                                                                              Address
                                                                                                                                               data
                                                             register
Instruction
                                                                                                 M
                                                                                                                                                          M
 memory
                              Instruction [15-11]
                                                             Write
                                                                                                x
                                                                                                                                          Data
                                                                                                                                                          ×
                                                                                                     instruction[5]
                                                             data
                                                                                                                                         memory
                                                                                                                              Write
                                                                                                                              data
                                                                       16
                                                                                    32
                              Instruction [15-0]
                                                                             Sign
                                                                            extend
                                                                                                  ALU
                                                                                                  control
                                                           Instruction [5-0]
                                                                                                             fc
```

Main Controller

Input or Output	Signal Name	R-format	lw	sw	Beq
Inputs	Op5	0	1	1	0
	Op4	0	0	0	0
	Op3	0	0	1	0
	Op2	0	0	0	1
	Op1	0	1	1	0
	Op0	0	1	1	0
	RegDst	1	0	X	X
	ALUSrc	0	1	1	0
	MemtoReg	0	1	X	X
Outputs	RegWrite	1	1	0	0
	MemRead	0	1	0	0
	MemWrite	0	0	1	0
	Branch	0	0	0	1
	ALUOp1	1	0	0	0
	ALUOp0	0	0	0	1

> fc 0

ALII Controller

Opcode	ALUOp	instruction	function	ALU Action	ALUCtrl
Lw	00	load word	XXXXXX	add	010
Sw	00	store word	XXXXXX	add	010
Beq	01	branch equal	XXXXXX	subtract	110
R-type	10	add	100000	add	010
R-type	10	subtract	100010	subtract	110
R-type	10	AND	100100	AND	000
R-type	10	OR	100101	OR	001
R-type	10	SLT	101010	SLT	111

R-type 10 funky 001011 SLT 111