5.16 5.16.1

5.10.1			TLB						
	Virtual	TLB		Ta					
Address	Page	H/M	Valid	g	Physical Page				
		TLB miss PT hit PF	1	b	12				
4669	4		1	7	4				
0x123d	1		1	3	6				
		111(71	1 (last access 0)	1	13				
			1 (last access 1)	0	5				
2227	0	TLB	1	7	4				
0x08b	U	miss PT hit	1	3	6				
		1110	1 (last access 0)	1	13				
			1 (last access 1)	0	5				
13916	3	TLB hit PT hit	1	7	4				
0x365c			1 (last access 2)	3	6				
			1 (last access O)	1	13				
	8	TLB miss PT hit PF	1 (last access 1)	0	5				
34587			1 (last access 3)	8	14				
0x871b			1 (last access 2)	3	6				
			1 (last access 0)	1	13				
	b	- 1.0	1 (last access 1)	0	5				
48870		TLB miss PT	1 (last access 3)	8	14				
0xbee6		hit	1 (last access 2)	3	6				
			1 (last access 4)	11	12				
			1 (last access 1)	0	5				
12608	3	TLB hit	1 (last access 3)	8	14				
0x3140	3	PT hit	1 (last access 5)	3	6				
			1 (last access 4)	b	12				
		TID	1 (last access 6)	С	15				
49225	С	TLB miss PT	1 (last access 3)	8	14				
0xc040	С	hit PF	1 (last access 5)	3	6				
			1 (last access 4)	b	12				

5.16.2

Addres	Virtua	TLB		TLB				
S	l Page	H/M	Valid	Tag	Physical Page			
	4		1	11	12			
4669		TLB	1	7	4			
0x123d	1	miss PT hit	1	3	6			
		1110	1 (last access 0)	0	5			
		TLB miss PT hit	1	11	12			
2227	0		1	7	4			
0x08b	U		1	3	6			
		1110	1 (last access 1)	0	5			
			1	11	12			
13916	3	TLB hit PT hit	1	7	4			
0x365c			1	3	6			
			1 (last access 2)	0	5			
	8	TLB miss PT hit PF	1 (last access 3)	2	13			
34587			1	7	4			
0x871b			1	3	6			
			2	0	5			
		T I D	1 (last access 4)	2	13			
48870	11	TLB miss PT	1	7	4			
0xbee6	11	hit	1	3	6			
			1 (last access 2)	0	5			
			1 (last access 4)	2	13			
12608	3	TLB hit	1	7	4			
0x3140	3	PT hit	1	3	6			
			5	0	5			
		T1.5	1 (last access 4)	2	13			
49225	12	TLB ! miss PT	1	7	4			
0xc040	12	hit	1 (last access 6)	3	6			
			1 (last access 5)	0	5			

A larger page size reduces the TLB miss rate but can lead to higher fragmentation and lower utilization of the physical memory.

5.16.3 Two-way set associative

	Way 3				TLB						
Addres	dres Virtua Inde 🗔		TLB		Та		inde				
S	l Page	Tag	х	H/M	Valid	g	Physical Page	х			
			1	TLB miss PT	1	b	12	0			
4669	1	0			1	7	4	1			
0x123d	1	U		hit PF	1	3	6	0			
				111611	1 (last access 0)	0	13	1			
				- 1.0	1 (last access 1)	0	5	0			
2227	0	0	0	TLB miss PT	1	7	4	1			
0x08b	0	U	U	hit	1	3	6	0			
				1110	1 (last access 0)	0	13	1			
	3		1	TLB miss PT hit	1 (last access 1)	0	5	0			
13916		1			1 (last access 2)	1	6	1			
0x365c					1	3	6	0			
					1 (last access 0)	1	13	1			
	8		0	TLB miss PT hit PF	1 (last access 1)	0	5	0			
34587		4			1 (last access 2)	1	6	1			
0x871b					1 (last access 3)	4	14	0			
					1 (last access 0)	1	13	1			
				TLB miss PT hit	1 (last access 1)	0	5	0			
48870	h	5	1		1 (last access 2)	1	6	1			
0xbee6	b	3			1 (last access 3)	4	14	0			
				1110	1 (last access 4)	5	12	1			
					1 (last access 1)	0	5	0			
12608	3		1	TLB hit	1 (last access 5)	1	6	1			
0x3140	3	1		PT hit	1 (last access 3)	4	14	0			
					1 (last access 4)	5	12	1			
			0	- 1.0	1 (last access 6)	6	15	0			
49225	6	6		TLB miss PT miss PF	1 (last access 5)	1	6	1			
0xc040	С	0			1 (last access 3)	4	14	0			
					1 (last access 4)	5	12	1			

5.16.4 Direct mapped

					TLB						
Addres	Virtua		Inde TLB		Vali	Та		inde			
S	l Page	Tag	х	H/M	d	g	Physical Page	х			
	1			TLB miss PT	1	b	12	0			
4669		0	1		1	0	13	1			
0x123d	1	U		hit PF	1	3	6	2			
					0	4	9	3			
					1	0	5	0			
2227	0	0	0	TLB miss PT	1	0	13	1			
0x08b	U	U	0	hit	1	3	6	2			
				1	0	4	9	3			
13916 0x365c			3	TLB miss PT hit	1	0	5	0			
	3	0			1	0	13	1			
					1	3	6	2			
					1	0	6	3			
34587 0x871b	8	2	0	TLB miss PT hit PF	1	2	14	0			
					1	0	13	1			
					1	3	6	2			
					1	0	6	3			
			3	TLB miss PT hit	1	2	14	0			
48870	L	2			1	0	13	1			
0xbee6	b				1	3	6	2			
				1110	1	2	6	3			
					1	2	14	0			
12608	3		3	TLB hit	1	0	13	1			
0x3140	3	0	3	PT hit	1	3	6	2			
					1	0	6	3			
					1	3	15	0			
49225		2		TLB miss PT miss PF	1	0	13	1			
0xc040	С	3	0		1	3	6	2			
				111133 1 1	1	0	6	3			

5.16.5 Without a TLB, almost every memory access would require two accesses to RAM: An access to the page table, followed by an access to the requested data.

5.20

- 5.20.1 There are no hits
- 5.20.2 Direct mapped

0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
М	М	М	М	М	М	М	М	Н	Н	М	М	М	М	Н	Н	М

- 5.20.3 Answers varies.
- 5.20.4 MRU is an optimal policy.
- 5.20.5 The best block to evict is the one that will cause the fewest misses in the future. Unfortunately, a cache controller cannot know the future! Our best alternative is to make a good prediction.
- 5.20.6 If you knew that an address had limited temporal locality and would conflict with another block in the cache, choosing not to cache it could improve the miss rate. On the other hand, you could worsen the miss rate by choosing poorly which addresses to cache.