

4.31.5

(Assuming load/store are resolved in MEM stage)

beqz IF ID EX MEM WB

li IF ID EX MEM WB

slti IF ID EX MEM WB

add IF ID EX MEM WB

ld IF ID EX MEM WB

add IF ID EX MEM WB

ld IF ID EX MEM WB

addi IF ID EX MEM WB

sub IF ID EX MEM WB

sd IF ID EX MEM WB

bne IF ID EX MEM WB

slti IF ID EX MEM WB

add IF ID EX MEM WB

ld IF ID EX MEM WB

add IF ID EX MEM WB

ld IF ID EX MEM WB

addi IF ID EX MEM WB

sub IF ID EX MEM WB

sd IF ID EX MEM WB

bne IF ID EX MEM WB

Ethan Wang
2/17/22

CS MISI B HW

819 4.31.6. For 4.31.3 Single Issue

12 instructions

For 4.31.4 two-issue

9 "instructions"

$$12 \div 9 = 1.33$$

There is a $1.33 \times$ speedup when going from single issue to two-issue.

4.31.7 beqz x13, DONE

li x12, 0

jal ENT

Top:

slli x5, x12, 3

add x6, x10, x5

ld x7, 0(x6)

ld x29, 8(x6)

addi x12, x12, 2

sub x30, x7, x29

add x31, x11, x5

sd x30, 0(x31)

slli x5, x12, 3

add x6, x10, x5

ld x7, 0(x6)

ld x29, 8(x6)

addi x12, x12, 2

sub x30, x7, x29

add x31, x11, x5

sd x30, 0(x31)

This loop has been unrolled so that 2 iterations run each time, and it has been optimized to run on the single-issue processor.