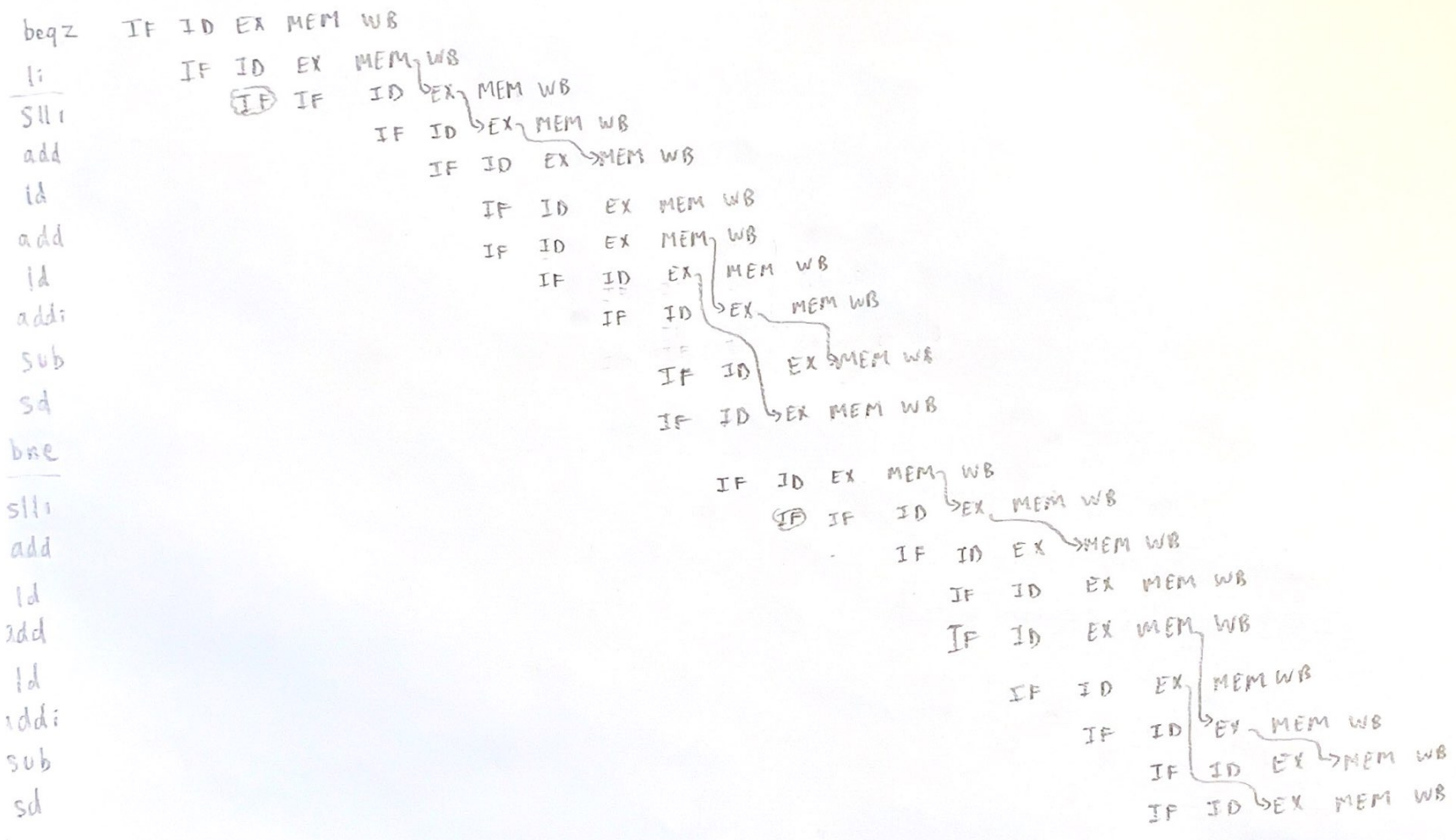
4.31.5 (I'm assuming load/store are resolved in MEM stage)



Ethan Wong
2/17/22

CS M151B HW

829 4.31.6. For 4.31.3 single issue
12 instructions
For 4.31.4 two-issue
9 "instructions"
12 ÷ 9 = 1.33
There is a 1.33 x speedup when going from single issue to two-issue.

4.31.7

```
beqz x13 , DONE
li   x12 , 0
jal  ENT
Top:
slli x5, x12, 3
add  x6, x10, x5
ld   x7, 0(x6)
ld   x29, 8(x6)
addi x12, x12, 2
sub  x30, x7, x29
add  x31, x11, x5
sd   x30, 0(x31)

slli x5, x12, 3
add  x6, x10, x5
ld   x7, 0(x6)
ld   x29, 8(x6)
addi x12, x12, 2
sub  x30, x7, x29
add  x31, x11, x5
sd   x30, 0(x31)
```

This loop has been unrolled so that 2 iterations run each time, and it has been optimized to run on the single-issue processor.