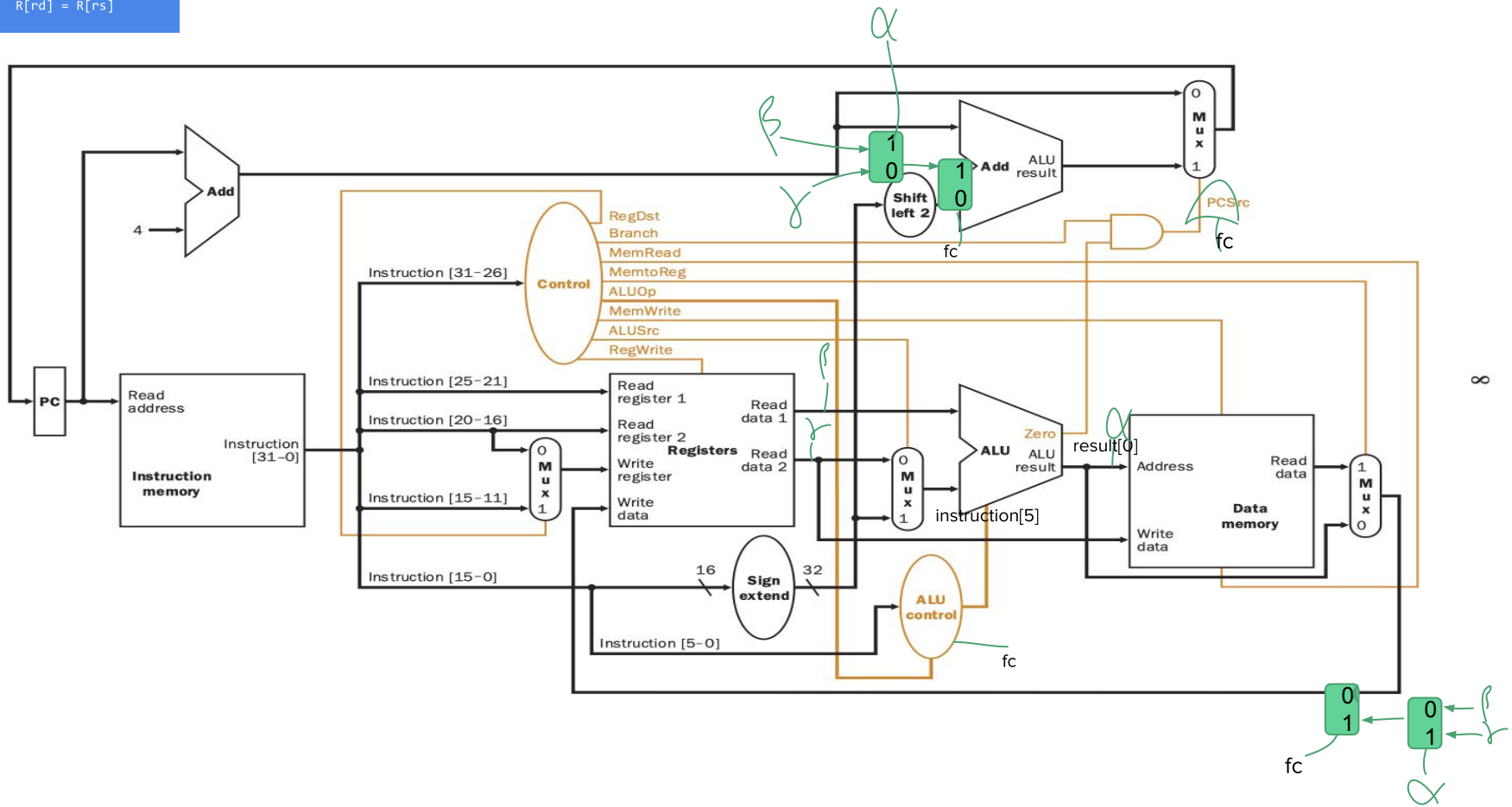
```
If ( R[rs] < R[rt] ):
        PC = PC+4+R[rs]
        R[rd] = R[rt]
Else:
        PC =  PC+4+R[rt]
        R[rd] = R[rs]
```



Main Controller

Input or Output	Signal Name	R-format	lw	sw	Beq
Inputs	Op5	0	1	1	0
	Op4	0	0	0	0
	Op3	0	0	1	0
	Op2	0	0	0	1
	Op1	0	1	1	0
	Op0	0	1	1	0
Outputs	RegDst	1	0	X	X
	ALUSrc	0	1	1	0
	MemtoReg	0	1	X	X
	RegWrite	1	1	0	0
	MemRead	0	1	0	0
	MemWrite	0	0	1	0
	Branch	0	0	0	1
	ALUOp1	1	0	0	0
	ALUOp0	0	0	0	1

```
If ( R[rs] < R[rt] ):
          PC = PC+4+R[rs]
          R[rd] = R[rt]
Else:
          PC =  PC+4+R[rt]
          R[rd] = R[rs]
```

ALU Controller

Opcode	ALUOp	instruction	function	ALU Action	ALUCtrl
Lw	00	load word	XXXXXX	add	010
Sw	00	store word	XXXXXX	add	010
Beq	01	branch equal	XXXXXX	subtract	110
R-type	10	add	100000	add	010
R-type	10	subtract	100010	subtract	110
R-type	10	AND	100100	AND	000
R-type	10	OR	100101	OR	001
R-type	10	SLT	101010	SLT	111

R-type 10 funky 001011 SLT 111

fc
0
0
0
0
0
0
0
0
1