CS151B/EE116C – Solutions to Sample Problem 1

Given a gate with an output signal O and k input signals I0, I1, I2, …, Ik:
DELAY(O) = MAX(DELAY(I0), DELAY(I1),…,DELAY(Ik)) + DELAY(k-input gate).

Given a multiplexer with an output signal O, k input signals I0, I1, I2, …, Ik, and selector S:
DELAY(O) = MAX(DELAY(S), DELAY(I0), DELAY(I1),…,DELAY(Ik)) + DELAY(multiplexer).

The sum of a 1-bit full adder is implemented as two cascaded 2-input XOR gates:
Sn= (An ^ Bn) ^ Cn

*: AND
+: OR
^: XOR

1.
G0 = A0*B0
- Delay(G0) = 2T

2.
P0 = A0^B0
- Delay(P0) = 2T

3.
G3 = A3*B3
- Delay(G3) = 2T

4.
P3 = A3^B3
- Delay(P3) = 2T
- All Gn and Pn that govern a 1-bit adder have delay 2T.

5.
C3 = G2 + G1*P2 + G0*P1*P2 + C0*P0*P1*P2
- Delay(C3) = 2T (P0/P1/P2) + 7T (4-input AND) + 7T (4-input OR) = 16T

6.
C4 = G3 + G2*P3 + G1*P2*P3 + G0*P1*P2*P3 + C0*P0*P1*P2*P3
- Delay(C4) = 2T (P0/P1/P2/P3) + 9T (5-input AND) + 9T (5-input OR) = 20T

7.
S3 = (A3^B3)^C3
- Delay(S3) = 16T (C3) + 2T (2-input XOR) = 18T

8.

Gα = G3 + G2*P3 + G1*P2*P3 + G0*P1*P2*P3

- Delay(Gα) = 2T (G0/P1/P2/P3) + 7T (4-input AND) + 7T (4-input OR) = 16T
- All Gx that govern a 4-bit CLA have delay 16T

9.

Pα = P0*P1*P2*P3

- Delay(Pα) = 2T (P0/P1/P2/P3) + 7T (4-input AND) = 9T
- All Px that govern a 4-bit CLA have delay 9T.

10.

C12 = Gβ + Gα*Pβ + "C4"*Pα*Pβ

- "C4" is ready at time 0 due to the Carry Select technique. As a result, the product with "C4" has latency 9T (Pα/Pβ) + 4T (3-input AND) = 13T while the Gα*Pβ term has delay 16T (Gα) + 2T (2-input AND) = 18T. As a result the latter term is the product with the highest latency.
- Delay(C12) = 16T (Gα) + 2T (2-input AND) + 4T (3-input OR) = 22T

11.

C16 = Gγ + Gβ*Pγ + Gα*Pβ*Pγ + "C4"*Pα*Pβ*Pγ

- Delay(C16) = 16T (Gα) + 4T (3-input AND) + 7T (4-input OR) = 27T

12.

S15 = (A15^B15)^C15

- To get the delay of S15, we need to find C15 which is a function of the 4-bit CLA with label γ.

C15 = G14 + G13*P14 + G12*P13*P14 + C12*P12*P13*P14

- The formula for C15 is comparable to the formula for C3. However, while C3 dealt with C0 which was ready at time 0, C15 deals with the carry in to the 4-bit CLA which is C12.
- Delay(C15) = 22T (C12) + 7T (4-input AND) + 7T (4-input OR) = 36T
- Delay(S15) = 36T (C15) + 2T (2-input XOR) = 38T

13.

Delay(Gω) = 16T

14.

Delay(Pω) = 9T

15.

C28 = Gψ + Gχ*Pψ + Gφ*Pχ*Pψ + "C16"*Pφ*Pχ*Pψ

- The formula for C28 is comparable to the formula for C16. C16 dealt with carry-in "C4" which was ready at time 0 while C28 deals with the carry-in "C16" which is also ready at time 0 due to the Carry Select technique. As a result, the latencies are identical.
- Delay(C28) = 16T (Gφ) + 4T (3-input AND) + 7T (4-input OR) = 27T

16.

C32 = Gω + Gψ*Pω + Gχ*Pψ*Pω + Gφ*Pχ*Pψ*Pω + "C16"*Pφ*Pχ*Pψ*Pω

- Delay(C32) = 16T (Gφ) + 7T (4-input AND) + 9T (5-input OR) = 32T

17.

S31 = (A31^B31)^C31

- This process of determining S31 is comparable to determining the delay of S15 and requires C31.

C31 = G30 + G29*P30 + G28*P29*P30 + C28*P28*P29*P30

- Delay(C31) = 27T (C28) + 7T (4-input AND) + 7T (4-input OR) = 41T
- Delay(S31) = 41T (C31) + 2T (2-input XOR) = 43T

18.

C16(after) has inputs C16(before) (ready at 27T) and selector C4 (ready at 20T)

- Delay(C16(after)) = 27T (C16(before)) + 4T (latency of multiplexer) = 31T

19.

C32(after) has inputs C32(before) (ready at 32T) and selector C16(after) (ready at 31T)

- Delay(C32(after)) = 32T (C32) + 4T (latency of multiplexer) = 36T

The maximal delay is the maximum latency of the output signals:

- Delay(S3) = 20T
- Delay(S4-S15(after)) = 38T (S15) + 4T (latency of multiplexer) = 42T
- Delay(S16-S31(after)) = 43T (S31) + 4T (latency of multiplexer) = 47T
- Delay(C32(after)) = 36T

Maximal Delay: 47T