| | | (SMISIB HWZ |
|------|----|---|
| 2.16 | | Expand MIPS register to 128 registers |
| | | 4 times as many instructions |
| | 1) | Each of the register fields (is, it, id) would need to be |
| | | movensed to 7 bils as 2 = 128. The finet field may |
| | | need to increase as well to encapsulate the new instructions |
| | | However, this depends on how many instructions there |
| | | were to begin with. The instruction no longer fits m 32 bits. |
| | 2) | Each of the register fields (15, 11) would need to be increased |
| | | to 7 bits as well. This would increase the total number |
| | | of bits needed to 36, unless some are taken from. |
| | | the mondate. |
| | 3) | Decrease - now that there are more instructions, its possible |
| | | that multiple small instructions could have been combined |
| | | into one. This would decrease the size of the program. |
| | | Larger registers can combat spilling, which decreases |
| | | overall piogram size. |
| | | Increase - Now that the instructions themsolves are larger |
| | | (no longer 32 bits), this may morease the size of a 'word', |
| | | effectively increasing programsize. |
| | | |
| 7.39 | | CPI: Arith: 1 Load/Store: 10 Branch: 3 3800 |
| | | 500M 300M 100M |
| | 1) | Arith: 400 Load/Store: (300 × 11) = 3300 Branch: (100 × 3.3) = 330 4020 |
| | | This is not a good design choice. Reducing arithmetic instructions |
| | | is nice, but they required few cycles to begin with. Increasing |
| | | the clock cycle time adversely affects the other more costly |
| | | instructions to a greater degree. The new design will actually |
| | | cause the program to take longer to execute. |
| | 2) | Original: (1×500) + (10×300) + (3×100) = 3800 |
| | | New # 1: (0.5 x 500) + (10 x 300) - (3 x 100) = 3550 1.07 x speedup |
| | | New = 2: (0.1 × 500) + (10 × 300) + (3×100) = 3350 1.13 × speedup |
| | | |

| 10 2 | .40 | 70% anthometre 10%. Load Store 20 branch |
|------|-----|--|
| | 1) | ZCPI 6 CPI 3CPI |
| | | $(0.7 \times 2) + (0.1 \times 6) + (0.2 \times 3) = 2.6$ average CPI |
| | 2) | 75x improvement in overall performance |
| | | Performance can be defined by IPC (instructions per cycle) |
| | | IPC = CP1 IPC = 2.6 = 0.3846 |
| | | If we increase this by 25 x> 0.3846 x 1.25 = 0.481 IPC |
| | | $CPI = \frac{1}{1PC}$ $CPI = \frac{1}{0.481} = 2.08$ |
| | | We are aiming for a CPI of 7.08. |
| | | $(0.7 \times ?) \cdot (0.(\times 6) \cdot (0.2 \times 3) = 2.08$ |
| | | $(0.7 \times ?) = 0.88$ |
| | | ? = 1.257 |
| | | Arithmetre instructions should take, on average, 1.257 CPI. |
| | 3) | 50". Improvement in overall performance |
| | | IPC = 0,3846 |
| | | Increase this by 50x> 0.3846 x 1.5 = 0.577 IPC |
| | | CPI = 0.517 = 1.733 |
| | | We are aiming for a CPI of 1.733 |
| | | $(0.7 \times ?) + (0.1 \times 6) + (0.2 \times 3) = 1.733$ |
| | | $(0.7 \times ?) = 0.533$ |
| | | ? = 0.7614 |
| | | Arithmetic instructions should take, on average, 0.7614 CPI. |
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