I completed this assignment entirely on my own, except for discussions with Jiaming Xu

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Assignment #4

1.

Half-Subtracter

X	Y	C	Diff.
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

Carry

	x'	x
y'	0	0
y	1	0

SoP $C = x' \cdot y$

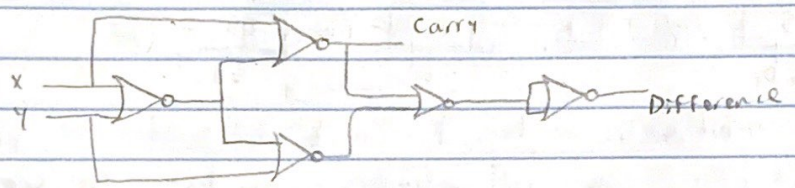
PoS $C = (x') \cdot (y)$

Difference

	x'	x
y'	0	1
y	1	0

SoP $D = (x \cdot y') + (x' \cdot y)$

PoS $D = (x + y) \cdot (x' + y')$



Full-Subtracter

X	Y	C_i	C_o	Diff
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	1	0
1	0	0	0	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

x \ yCi	00	01	11	10
0	0	1	0	1
1	1	0	1	0

Difference

SoP: $D = (x' \cdot y' \cdot C_i) + (x' \cdot y \cdot C_i') + (x \cdot y' \cdot C') + (x \cdot y \cdot C)$

PoS: $D = (x + y + C) \cdot (x + y' + C') \cdot (x' + y + C') \cdot (x' + y' + C)$

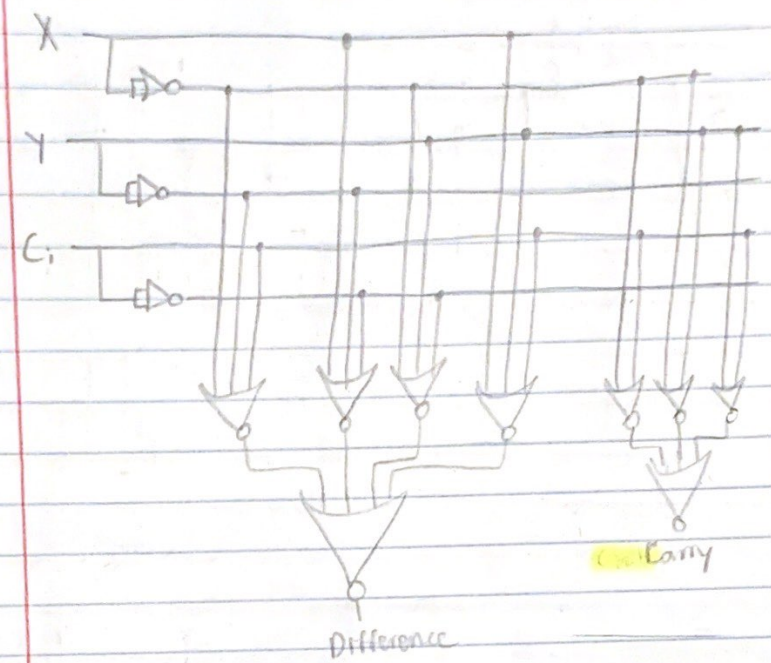
x \ yCi	00	01	11	10
0	0	1	1	1
1	0	0	1	0

Carry

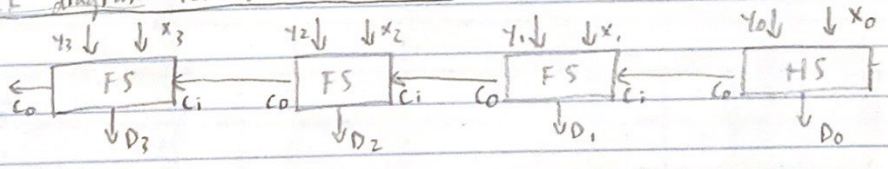
SoP: $(x' \cdot C) + (x' \cdot y) + (y \cdot C)$

PoS: $(y + C) \cdot (x' + y) \cdot (x' + C)$

Full subtractor Circuit Diagram



Block diagram for 4-bit subtractor



HS : Half Subtracter

FS : Full Subtracter

Gate Delay for 32-bit subtractor

31 FS : 31 × (3 gate delays for C_{out}) = 93 gate delays

1 HS : 2 gate delays

93 + 2 = 95 gate delays

2. Half - comparator

x	y	G	L
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

	y'	y
x'	0	0
x	1	0

G

SoP : $G = x \cdot y'$

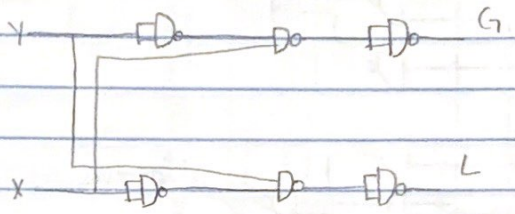
PoS : $G = x \cdot y'$

	y'	y
x'	0	1
x	0	0

L

SoP : $L = x' \cdot y$

PoS : $L = x' \cdot y$



Full comparator

x	y	Gin	Lin	Gout	Lout
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	X	X
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	0	1
0	1	1	1	X	X
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	X	X
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	X	X

Gout

xy \ Gin Lin	00	01	11	10
00	0	0	X	1
01	0	0	X	0
11	0	0	X	1
10	1	1	X	1

* SoP : $(y' \cdot Gin) + (x \cdot y') + (x \cdot Gin)$

PoS : $(x + Gin) \cdot (x + y') + (y' + Gin)$

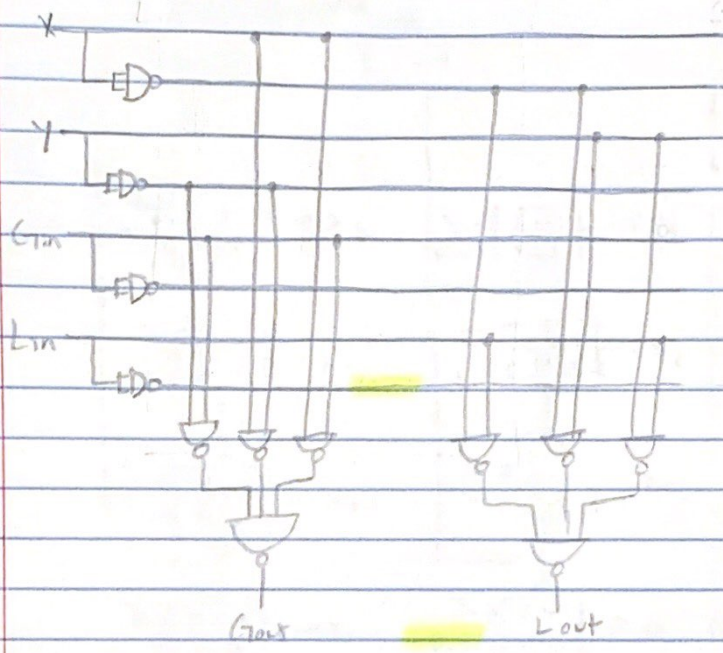
Lout

xy \ Gin Lin	00	01	11	10
00	0	1	X	0
01	1	1	X	1
11	0	1	X	0
10	0	0	X	0

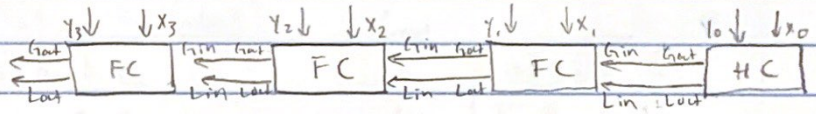
* SoP : $(x' \cdot Lin) + (x' \cdot y) + (y \cdot Lin)$

PoS : $(y + Lin) \cdot (x' + y) \cdot (x' + Lin)$

Full comparator diagram



Block diagram for Full 4-bit comparator



96 Gate delays:

31 FC : 31 × (3 gate delays) = 93 gate delays

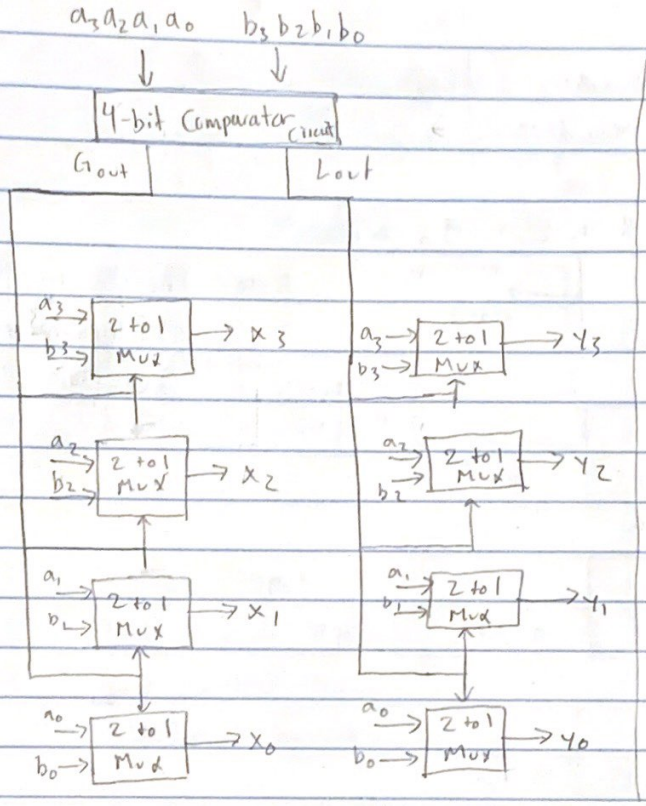
1 HC : 3 gate delays

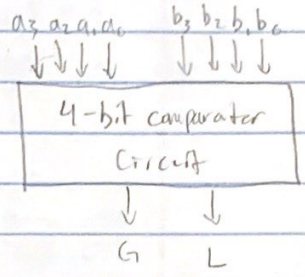
93 + 3 = 96 gate delays

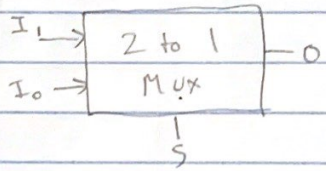
* I had a bit of trouble understanding how a full comparator would work — I implemented it to the best of my understanding. I hope it makes sense. Also, sorry the circuit diagram is a little messy.

This is a diagram for a Vector Mux created out of scalar Muxes.

3.





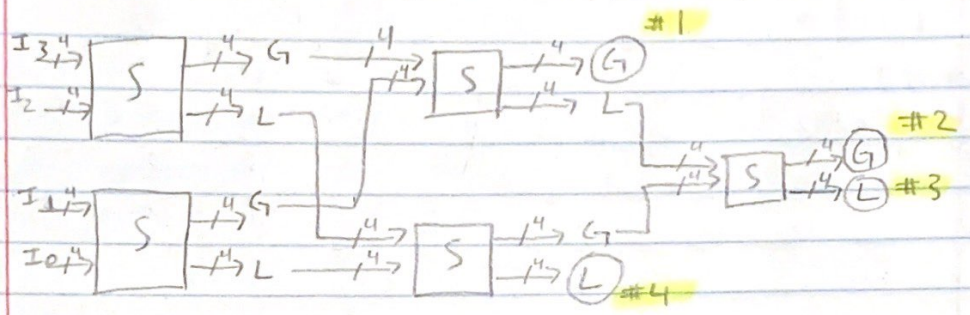


Gout	X3 X2 X1 X0 (output)	Lout	Y3 Y2 Y1 Y0 (output)
0	b3 b2 b1 b0	0	a3 a2 a1 a0
1	a3 a2 a1 a0	1	b3 b2 b1 b0

This circuit diagram is for a Vector Mux, it shows how the vector Mux is created from numerous 2 to 1 scalar Muxes.

4. [S] : This is the sorting circuit from #3.

I_0, I_1, I_2, I_3 are supposed to represent separate 4-bit inputs.



#1 : Largest input
#2 : 2nd largest input
#3 : 3rd Largest input
#4 : Smallest input

#1 ≥ #2 ≥ #3 ≥ #4