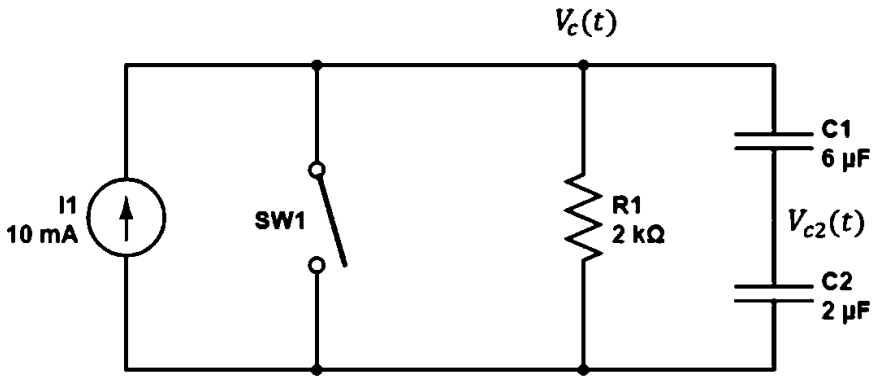
ECE100 Midterm 2 Solutions Spring 2022

Q1: The switch is closed well before $t = 0$ and the switch is opened at $t = 0$. (The lowest node of the graph is treated as ground.)



(a) What is the initial condition ($t = 0$) and steady condition ($t \to \infty$) of V_C?

Solution:

$$V_C(0) = 0V$$

$$V_C(\infty) = 20V$$

(b) What is the initial condition ($t = 0$) and steady condition ($t \to \infty$) of V_{C_2} (voltage across C_2)?

Solution:

$$V_{C_2}(0) = 0V$$

Using the equation for a Capacitor voltage divider:

$$V_{C_2}(\infty) = 15V$$

(c) Write down the equation for $V_c(t)$.

Solution:

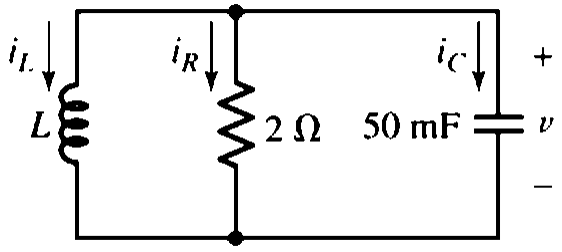
Using the general form $V_c(t) = V_\infty + (V_0 - V_\infty)e^{-\frac{t}{\tau}}$

The time constant $\tau = RC_{eq}$ where $C_{eq} = \frac{(6\times10^{-6})(2\times10^{-6})}{(6\times10^{-6})+(2\times10^{-6})} = \frac{3}{2}\times 10^{-6}F$

$$\tau = (2 \times 10^3)\left(\frac{3}{2}\times 10^{-6}\right) = 0.003s$$

This means $V_c(t) = 20 + (-20)e^{-\frac{t}{0.003}} = 20\left(1 - e^{-\frac{t}{0.003}}\right)$

Q2: For the circuit below, the value of the inductance is $L = 1250mH$. Determine $v(t)$ if it is known that the capacitor initially stores 390 J of energy and the inductor initially stores zero energy.



Solution:

Initial Conditions:

The problem gives the energy initially stored in the capacitor. This allows us to find the initial voltage.

$$E_c = \frac{1}{2}Cv^2$$

$$E_c(0) = 390 = \frac{1}{2}(0.05)v(0)^2$$

$$15{,}600 = v(0)^2$$

$$v(0) = \sqrt{15{,}600} = 124.9V$$

Note that since $E_L = \frac{1}{2}Li_L^2$, the initial current through the inductor must be equal to 0.

Also $i_R = \frac{v}{2} = 62.4A$

KCL:

I write the KCL in terms of v:

$$0 = i_L + i_R + i_C = \frac{1}{L}\int v\,dt + \frac{v}{R} + C\frac{dv}{dt}$$

$$0 = C\frac{d^2v}{dt^2} + \frac{1}{R}\frac{dv}{dt} + \frac{1}{L}v$$

$$0 = \frac{d^2v}{dt^2} + \frac{1}{RC}\frac{dv}{dt} + \frac{1}{LC}v$$

$$0 = \frac{d^2v}{dt^2} + 10\frac{dv}{dt} + 16v$$

Solving using the characteristic equation:

$$s^2 + 10s + 16 = 0$$

$$s = \frac{-10 \pm \sqrt{100 - 64}}{2}$$

$$s = -5 \pm 3$$

$$s_1 = -2, s_2 = -8$$

We plug this into our expected solution form for the overdamped case:

$$v(t) = K_1 e^{-2t} + K_2 e^{-8t}$$

Using the initial conditions to solve for the constants:

$$v(0) = 124.9 = K_1 + K_2$$

$$K_1 = 124.9 - K_2$$

We need one more equation so I will take the derivative:

$$\frac{dv(0)}{dt} = -2K_1 - 8K_2$$

Note that the equation for capacitor current is $i_C = C\frac{dv}{dt}$ and we can use KCL with the initial conditions to solve for this.

$$0 = C\frac{dv}{dt} + i_L + i_R = C\frac{dv}{dt} + 0 + \frac{v}{R}$$

$$\frac{dv}{dt} = -\frac{v}{RC} = -10(124.9)$$

$$-10(124.9) = -2K_1 - 8K_2 = -2(124.9 - K_2) - 8K_2$$

$$-8(124.9) = -6K_2$$

$$K_2 = 166.5$$

$$K_1 = -41.6$$

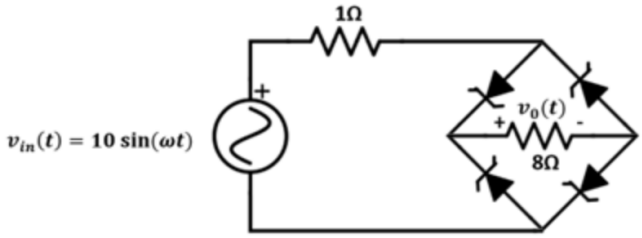
Then

$$v(t) = -41.6e^{-2t} + 166.5e^{-8t}$$

Q3: In the following circuit, the forward ON voltage for all diodes is 00.5V and the reverse breakdown voltage for Zener diodes is 5V.

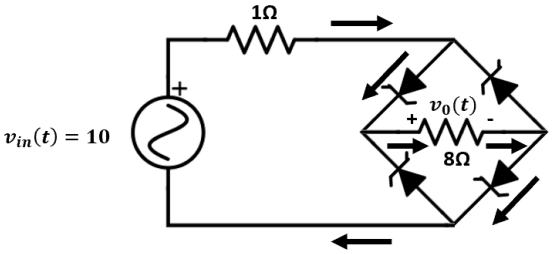
(a) Sketch $v_0(t)$ for one cycle of v_{in} treating the diodes as basic diodes, not Zener diodes. Mark important voltage levels on the sketch.

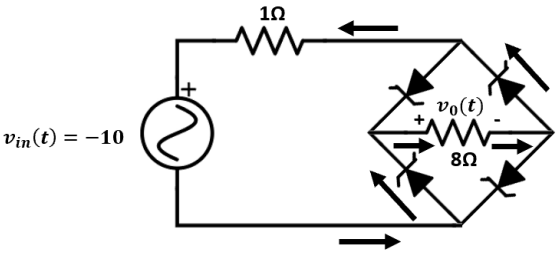
(b) Sketch $v_0(t)$ for one cycle of v_{in} treating the diodes as Zener diodes. Mark important voltage levels on the sketch.



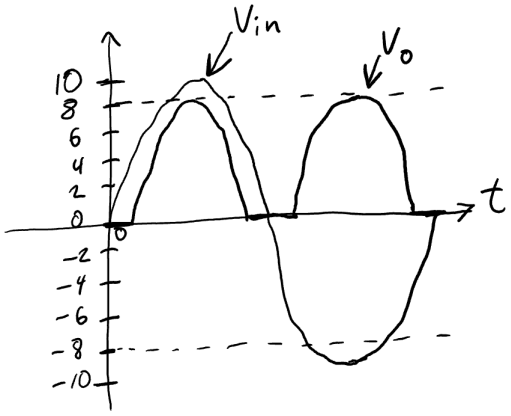
Solution:

(a) This is nearly the same as the full wave rectifier circuit we looked at in class. To find the peak voltage, we consider $v_{in} = \pm 10V$.

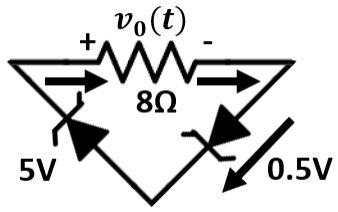




In each case, there will be 0.5V drop across each forward biased diode. Since there are two forward biased diodes in the path of the current, this will be a total of 1V drop due to the diodes. The remaining 9V will drop 1V across the 1Ω resistor and 8V across the 8Ω resistor. Since $v_0(t)$ is across the 8Ω resistor and will always be positive with the polarity marked, we see the following output with a peak voltage of 8V.



(b) The only difference between this and part (a) is that the diodes are now treated as Zener diodes. This means the reverse bias voltage across the Zeners will be capped at 5V.



Looking at this portion of the circuit shown above in isolation where $v_{in} = 10$, we can write a KVL loop.

$$5 \geq v_0 + 0.5$$

Thus:

$$v_0 \leq 4.5V$$

There is symmetry in this circuit, and the same condition holds for analyzing the top side of the rectifier and for analyzing for $v_{in} < 0$.