HW5 Solutions

Part 2 (Graded)

Q1. Textbook Problem 9.40

The circuit shown in Figure P9.40(a) is a type of logic gate. Assume that the diodes are ideal. The voltages V_A and V_B independently have values of either 0V (for logic 0, or low) or 5V (for logic 1, or high). For which of the four combinations of input voltages is the output high (i.e., $V_0 = 5V$)? What type of logic gate is this? Repeat for the circuit of Figure P9.40(b).

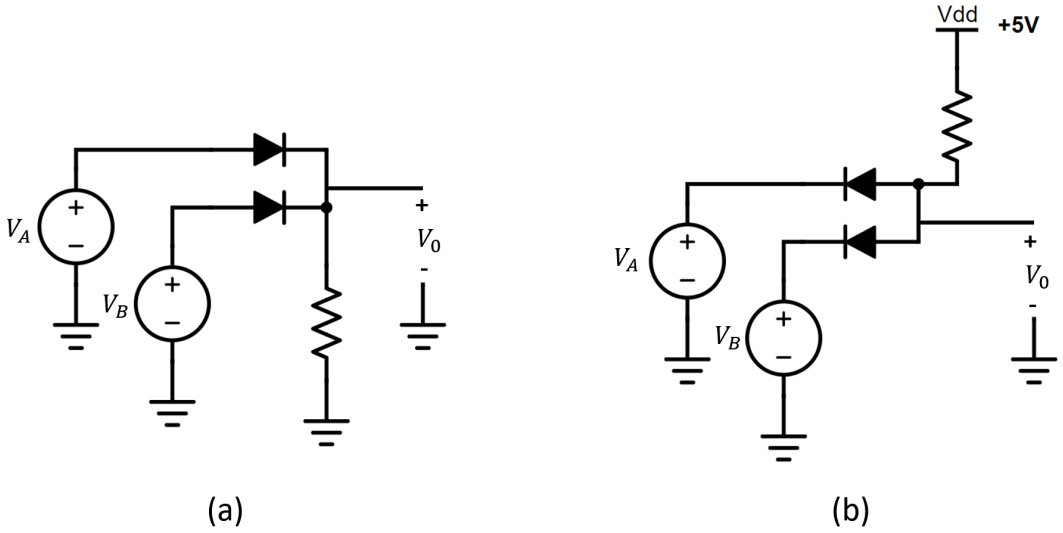


Figure 9.40

V_A	V_B	(a) V_0	(b) V_0
Low	Low	Low	Low
Low	High	High	Low
High	Low	High	Low
High	High	High	High

Logic Gate	(a) OR	(b) AND

Q2. Textbook Problem 9.66

Sketch the transfer characteristic (v_0 versus v_{in}) to scale for the circuit shown in Figure P9.66. Allow v_{in} to range from -5V to +5V and assume that the diodes are ideal.

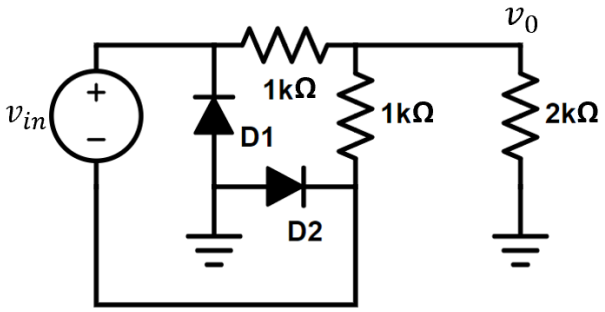


Figure P9.66

Solution:
When v_{in} is nonzero, one of the two diodes will be on. For a positive voltage, D2 will be on. For a negative voltage, D1 will be on.

If D2 is on, the node connected to the negative terminal of the voltage source will be connected to ground and have a value of 0V. The positive side will have a value of v_{in} since v_{in} is greater than 0 in this case.
If D1 is on, the node connected to the positive terminal of the voltage source will be connected to ground and have a value of 0V. The negative side will have a value of $-v_{in}$ since v_{in} is less than 0 in this case.

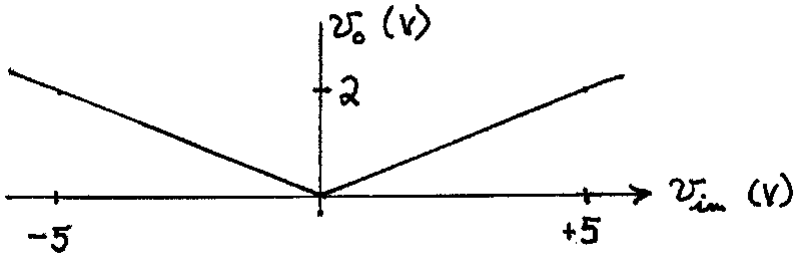
In both cases, v_0 will be the result of a voltage divider.
For the case where $v_{in} > 0$:

$$v_0 = v_{in}\left(\frac{\left(\frac{1k(2k)}{1k+2k}\right)}{1k+\left(\frac{1k(2k)}{1k+2k}\right)}\right) = v_{in}\left(\frac{2}{5}\right)$$

For the case where $v_{in} < 0$:

$$v_0 = -v_{in}\left(\frac{2}{5}\right)$$

Add your sketch here:



Q3. Textbook Problem 9.70

Sketch to scale the steady-state output waveform for the circuit shown in Figure P9.70. Assume that *RC* is much larger than the period of the input voltage and that the diodes are ideal.

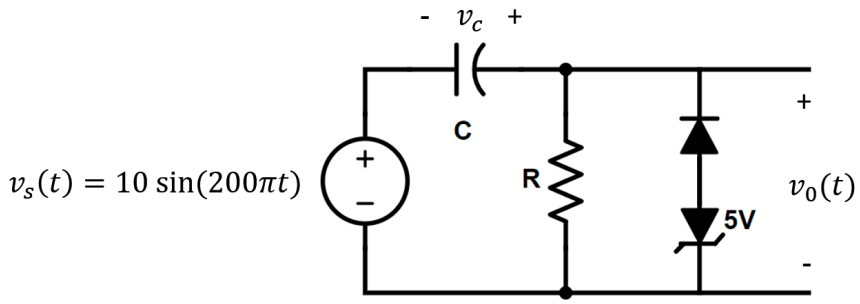
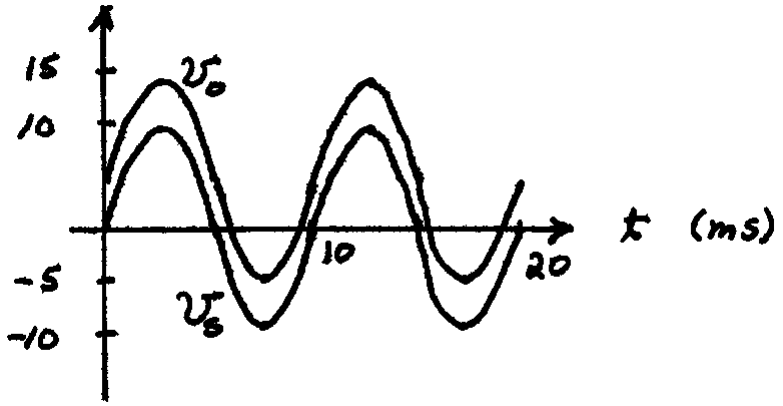


Figure P9.70

Solution:
Since RC is much larger than the period, the capacitor will not have time to discharge between cycles of v_s. The capacitor will end up taking a somewhat constant voltage level. To find this level, consider what will happen at the extremes of v_s if the capacitor is uncharged. If $v_s = 10V$, then the diode-Zener branch will not be conducting current since the basic diode will be reverse biased. If $v_s = -10V$, then the basic diode will be on and the Zener diode will be conducting in the reverse direction with a constant voltage drop of 5V. This will force the capacitor to charge to $v_c = 5V$ to satisfy KVL. This voltage will stay relatively constant, so $v_0 = v_s + v_c$ and the waveform of v_0 will effectively be shifted up by 5V relative to v_{in}.

Add your sketch here:



Q4. Textbook Problem 9.72

Design a clipper circuit to clip off the portions of an input voltage that fall above 3V or below -5V. Assume that diodes having a constant forward drop of 0.7V are available. Ideal Zener diodes of any breakdown voltage required are available. DC voltage sources of any value are available.

Solution:
There are multiple possible correct solutions.
One possible circuit is shown below. By using basic diodes in series with the Zener diodes, but with opposite polarity, we prevent the Zener diodes from conducting in the forward biased direction. Then the Zener diode should be set to 0.7V less than the desired maximum magnitude for v_0 in that direction to account for the forward voltage drop of the basic diode.

Answer: