`

HW6

Due Thursday 6/2 at 3:00PM on Gradescope

You are not required to submit the solutions to Part 1, but you still should solve these questions since op amps will be on the final.

Part 1 (Practice Problems):

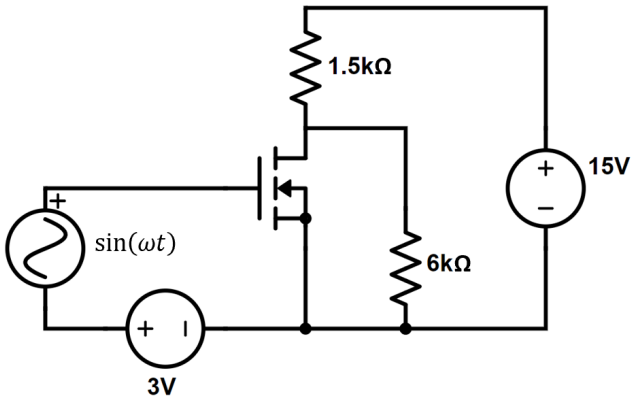
Q1. Problem 11.3

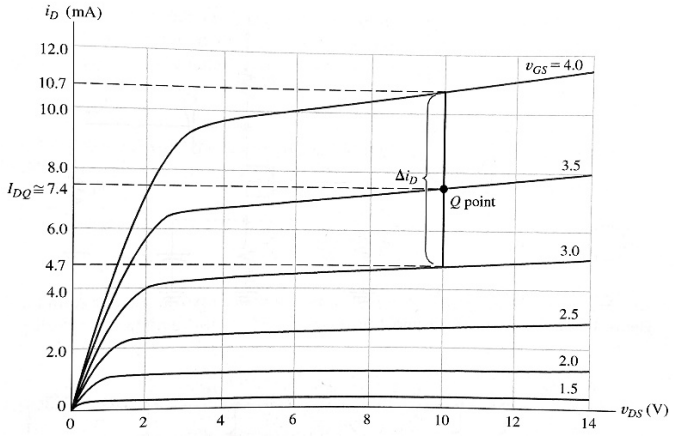
A certain NMOS transistor has $V_{t0} = 1V$, $KP = 50\mu A/V^2$, $L = 5\mu m$, and $W = 50\mu m$. For each set of voltages, state the region of operation and compute the drain current.

- **a.** $v_{GS} = 4V$ and $v_{DS} = 10V$
- **b.** $v_{GS} = 4V$ and $v_{DS} = 2V$
- **c.** $v_{GS} = 0V$ and $v_{DS} = 10V$

Q2. Problem 11.22

Use a load-line analysis of the circuit shown in the figure below to determine the values of V_{DSQ}, V_{DSmin}, and V_{DSmax}. The characteristics of the FET are shown in the plot on the right. Note that the labelled I_{DQ} is for a different textbook example, not for this problem. [Hint: First, replace the 15V source and the resistances by their Thevenin equivalent circuit.]

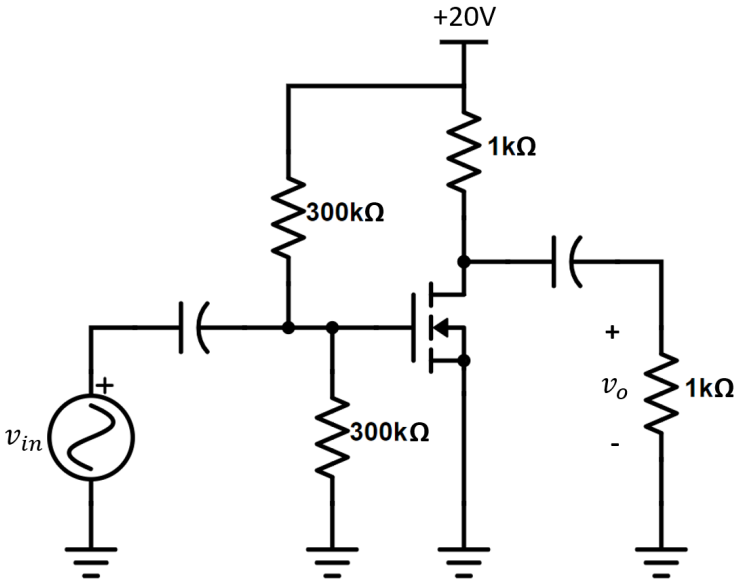




Q3. Problem 11.50

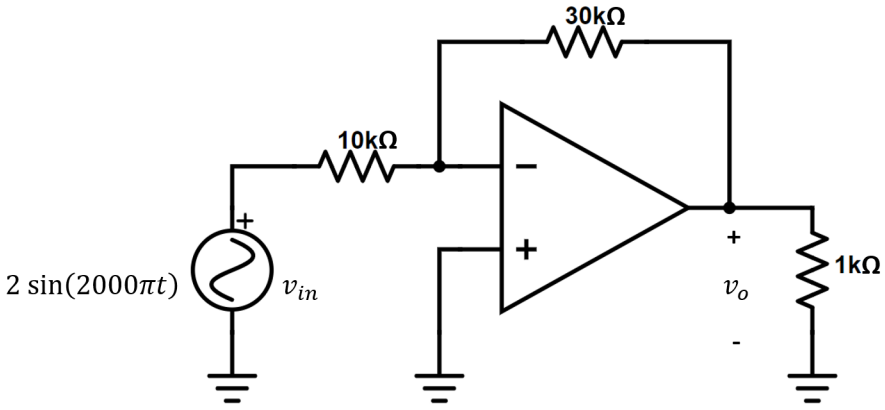
Consider the common-source amplifier shown in the figure below. The NMOS transistor has $KP = 50\mu A/V^2$, $L = 5\mu m$, $W = 500\mu m$, $V_{to} = 1V$, and $r_d = \infty$.

- **a.** Determine the values of I_{DQ}, V_{DSQ}, and g_m.
- **b.** Compute the voltage gain, input resistance, and the output resistance, assuming that the coupling capacitors are short circuits for the ac signal.



Q4. Problem 13.9

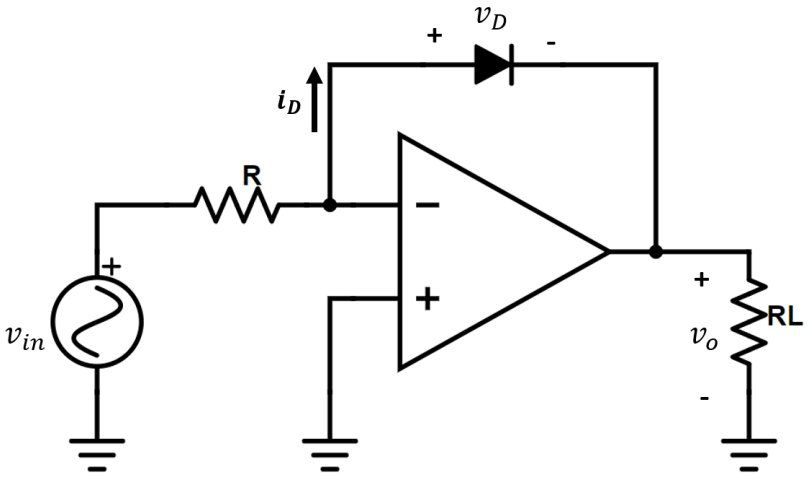
Consider the circuit shown in the figure below. Sketch $v_{in}(t)$ and $v_o(t)$ to scale versus time. The op amp is ideal.



`

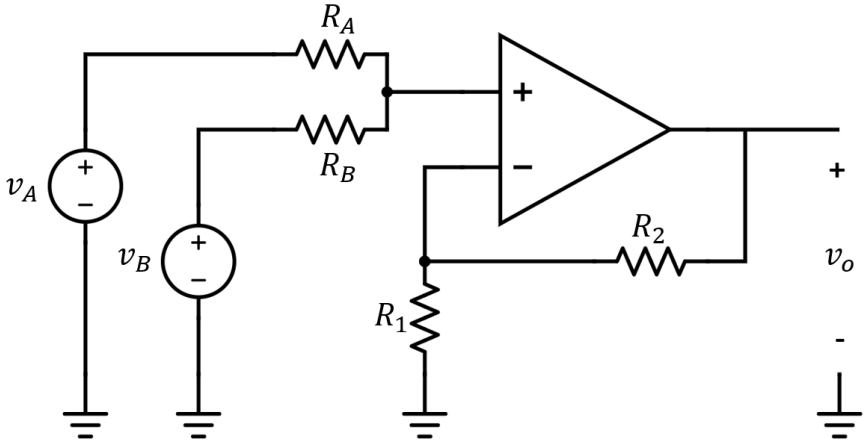
Q5. Problem 13.12

Consider the inverting amplifier shown in the figure below, in which one of the resistors has been replaced with a diode. Assume an ideal op amp, v_{in} positive, and a diode current given by $i_D = I_s \exp(v_D/nV_T)$. Derive an expression for v_o in terms of v_{in}, R, I_s, n, and V_T.



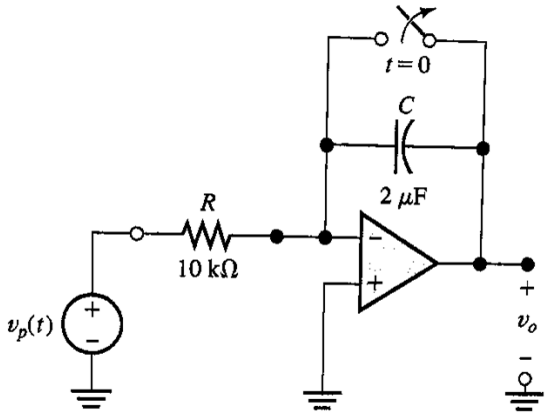
Q6. Problem 13.21

Analyze the ideal-op-amp circuit shown in the figure below to find an expression for v_o in terms of v_A, v_B, and the resistance values.

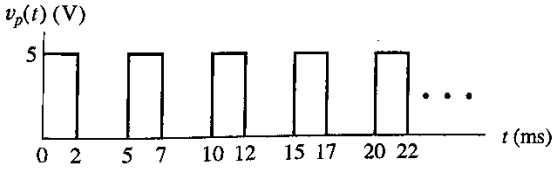


Q7. Problem 13.74

Sketch the output voltage of the idea-op-amp circuit shown in the figure below to scale versus time. The circuit is shown in (a) and the input voltage $v_p(t)$ is shown in (b).



(a)



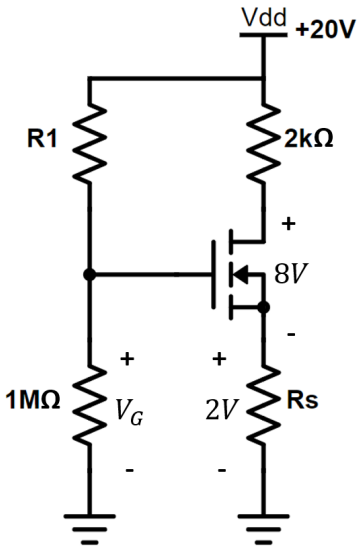
(b)

`

Part 2 (Graded):

Q1. Problem 11.29

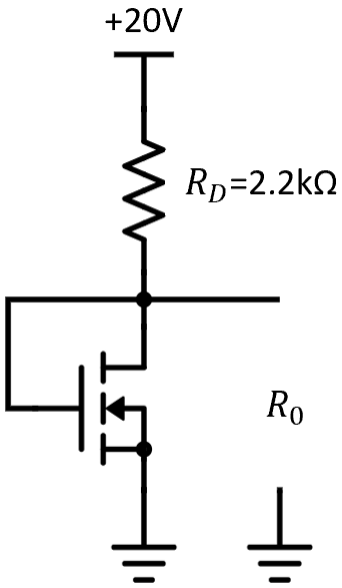
The transistor in the figure below has $KP = 50\mu A/V^2$, $W = 600\mu m$, $L = 20\mu m$, and $V_{t0} = 1V$. Determine the values of R_1 and R_s.



`

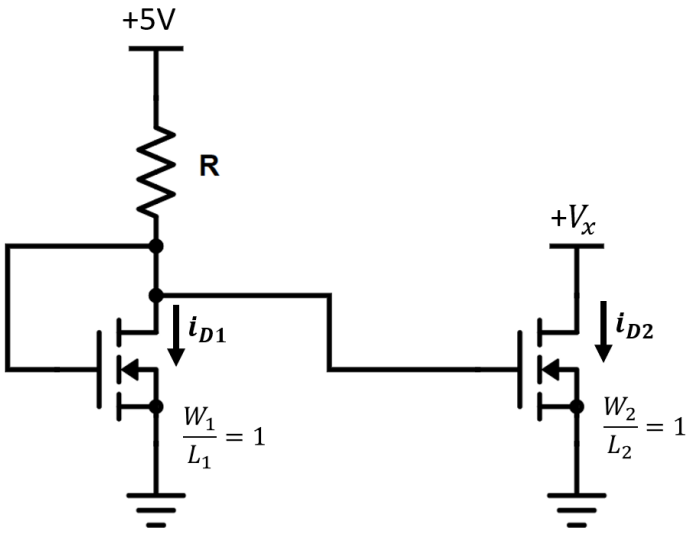
Q2. Problem 11.53

Find V_{DSQ} and I_{DQ} for the FET shown in the figure below, given $V_{t0} = 3V$ and $K = 0.5mA/V^2$. Find the value of g_m at the operating point. Draw the small-signal equivalent circuit, assuming that $r_d = \infty$ (r_d is the resistance in the small signal model due to channel length modulation, not the same as the R_D marked in the circuit). Derive an expression for the resistance R_0 in terms of R_D and g_m. Evaluate the expression for the values given.



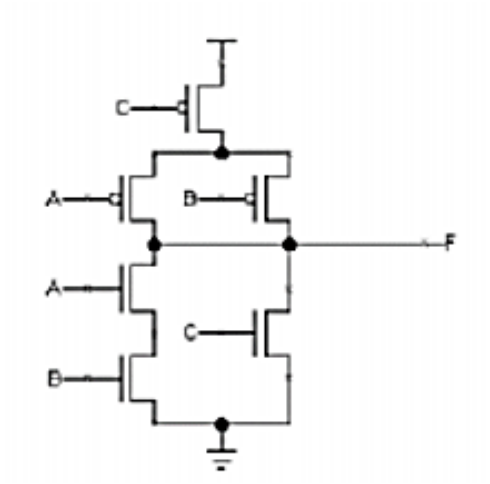
Q3. Problem 11.35

Both transistors shown in the figure below have $KP = 100\mu A/V^2$ and $V_{t0} = 0.5V$. Determine the value of R needed so that $i_{D1} = 0.2mA$. For what range of V_x is the second transistor operating in the saturation region? What is the resulting value of i_{D2}? Provided that V_x is large enough so that the second transistor operates in saturation, to what ideal circuit element is the transistor equivalent?



`

Q4. Analyze the CMOS circuit below (triode region equivalent) and fill out the "truth table" for it.



A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	