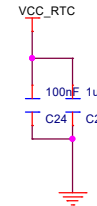
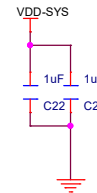
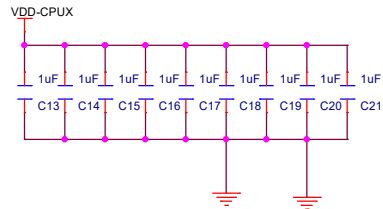
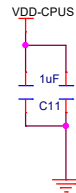
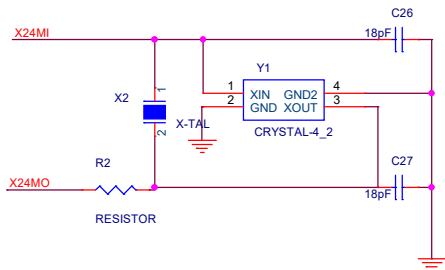
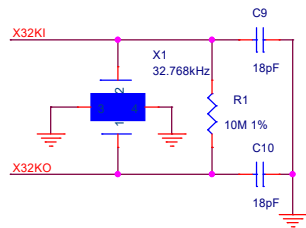
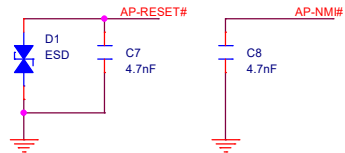
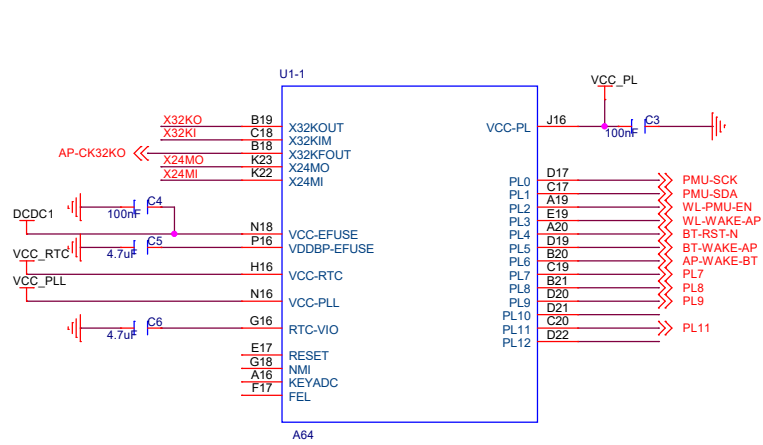
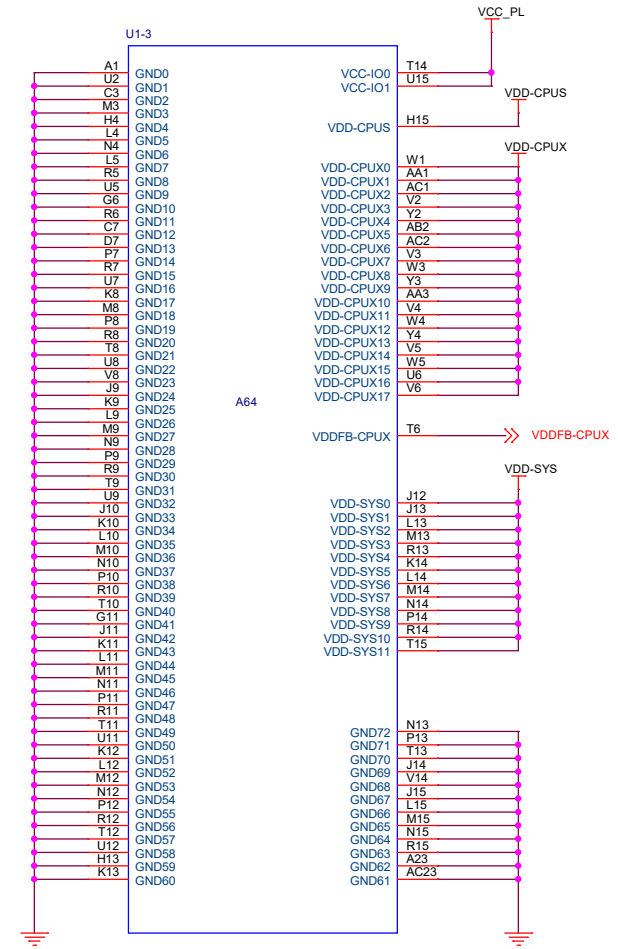
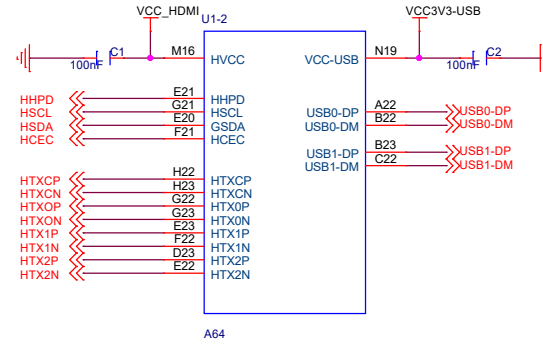


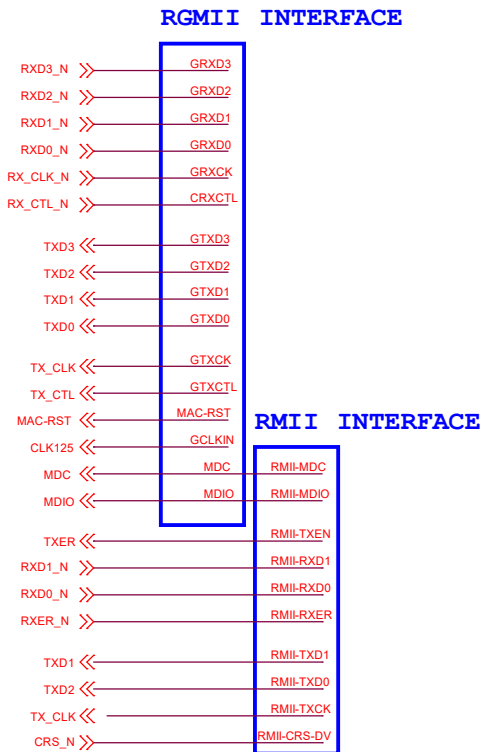
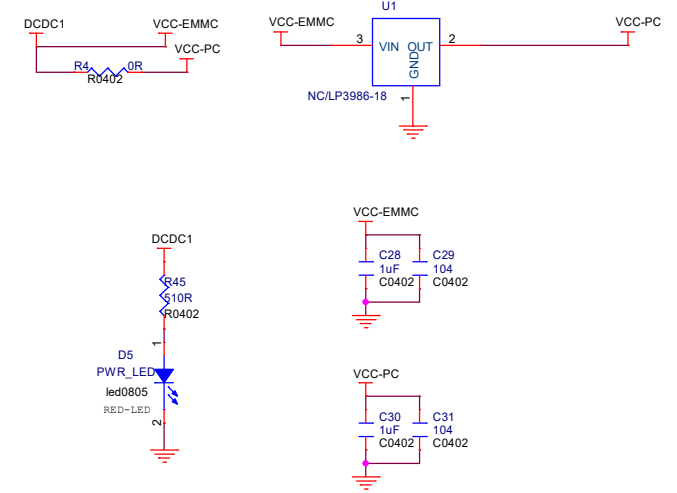
# CPU



## interface block summary

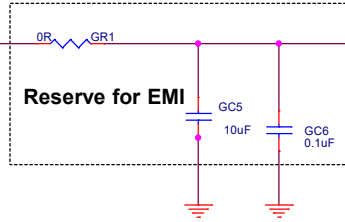


# ETHERNET

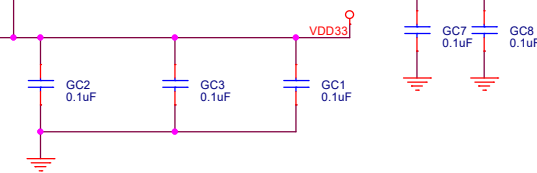


# Ethernet Magnetic / RJ45

GMAC-3V

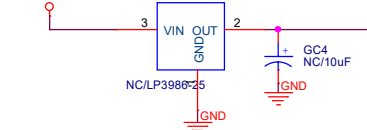


PHY\_VDD33



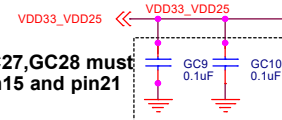
PHY\_VDD33

PHY\_VDD25



Reserve for 2.5V RGMII power (If MAC support 2.5V RGMII)

R80 for 3.3V RGMII  
R81 for 2.5V RGMII (From 3.3-2.5V LDO)  
R82 for 2.5VRGMII (From ACR 2.5V)  
RTL8201FN/EN:GR81(NC) GR82(NC)



For EMI GC27,GC28 must close to pin15 and pin21

PHY\_VDD33

PHY\_VDD25

VDD25

PHY\_AVDD10

C44 close to pin40

PHY\_VDD10

C39 close to pin28

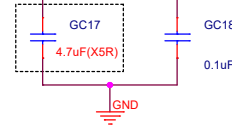
RTL8201FN/EN :  
C40,C41,GL1 is NC  
GC33,GC38,GC35,GC37 is NC

Reserve for EMI

Note 1: The Trace length between GL1 and Pin 48 must be within 0.5 cm. GC40 and GC41 to G L1 must be within 0.5cm.

RTL8211D/8211CN:GC40 22uF(X5R)  
RTL8211E: GC40 4.7uF(X5R)

C40 close to L1



VDDREG

RTL8211D/8211CN: L1=4.7uH  
RTL8211E: L1= 2.2uH

Note 2: The Trace length from C56, C57 to Pin 44,45 must be within 1 cm. The trace width from PHY\_AVDD33 to Pin 44,45 should>40mils

PHY\_AVDD33

Isolation VDDREG and AVDD33  
RTL8201FN/EN:GC56(NC),GC57(NC),GR146(NC)  
RTL8211CN/8211D: GC56 22uF(X5R)  
RTL8211E: GC56 4.7uF(X5R)

External Power Source

U10,GC69,GC68, GR122,GR120 and GR121 are only used by 8211CN/8211D/8211E application when switching regulator is disabled. For other applications, please remove them.

RESERVE

LED1\_AD1  
LED0\_AD0



100 ohm



ChipHD to Pine64

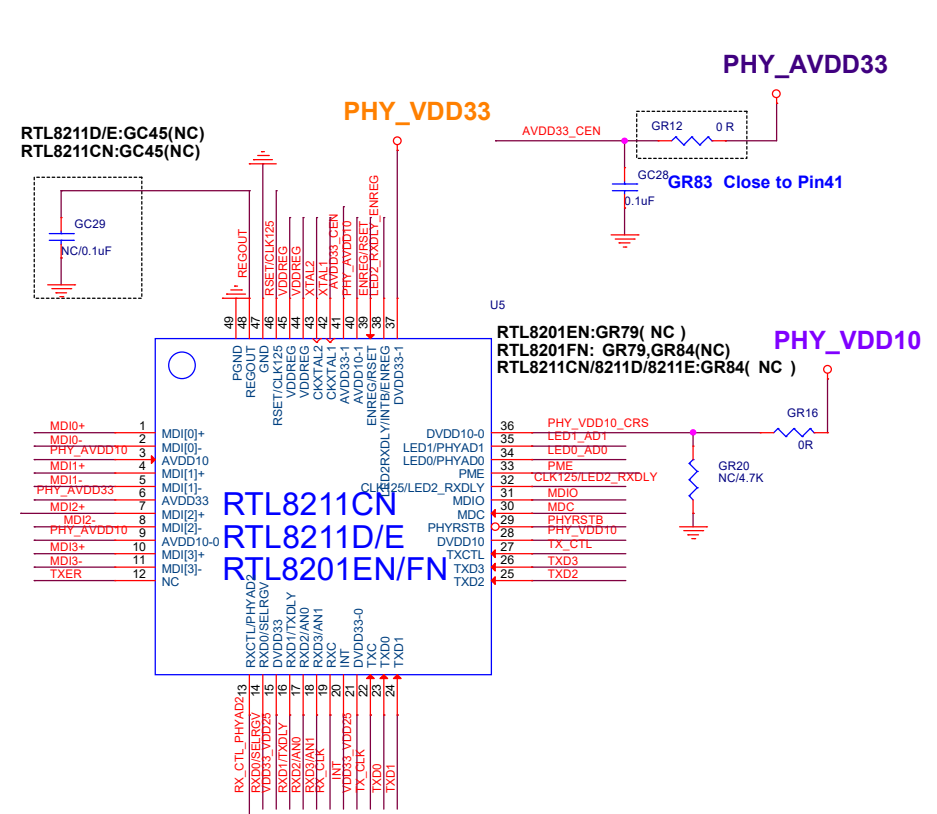
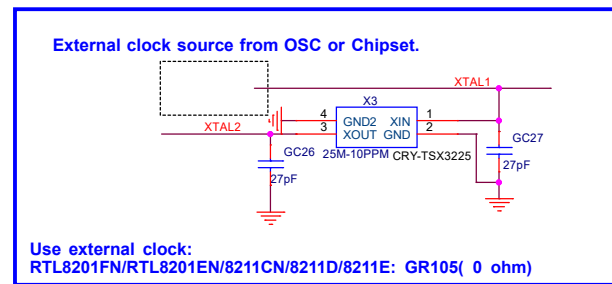
5  
ETHERNET PHY

#### 4 External clock and Crvstal

---

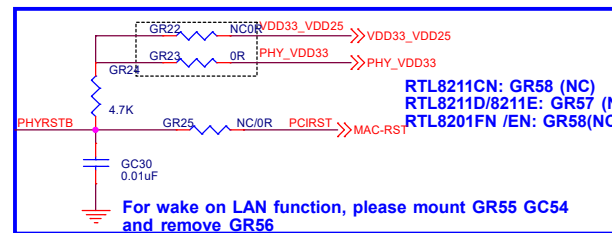
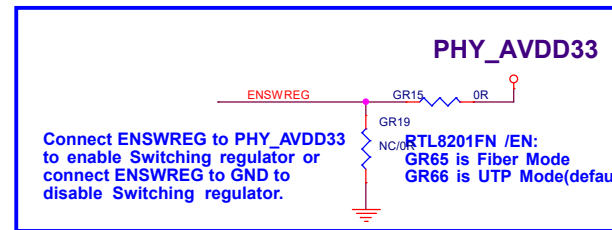
## 2

## 1



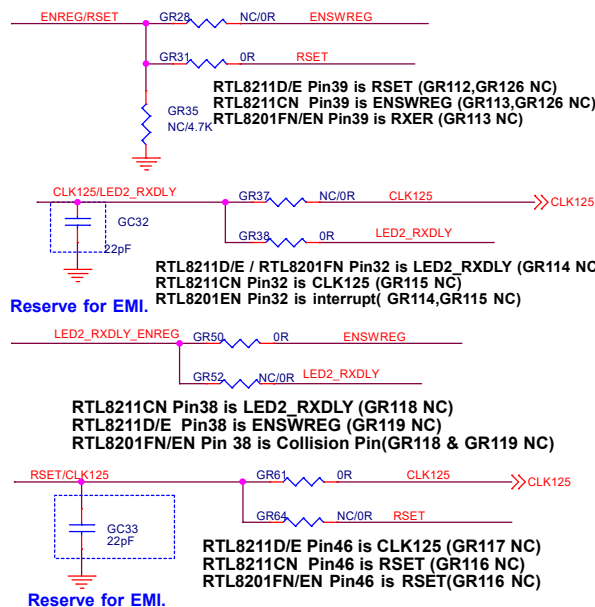
# ETHERNET PHY

## Enable/Disable SWREG

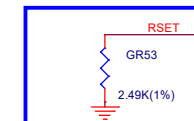


## PHY Reset

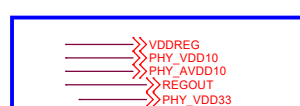
## RSET/ENSWREG/CLK125 Co-layout



**RSET**

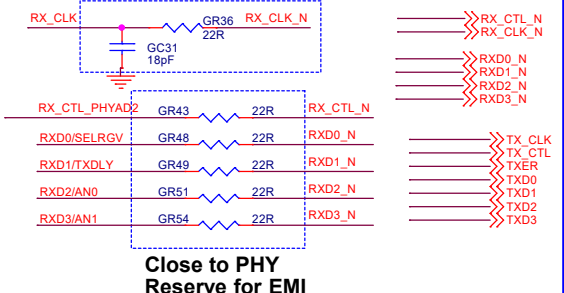


## Others

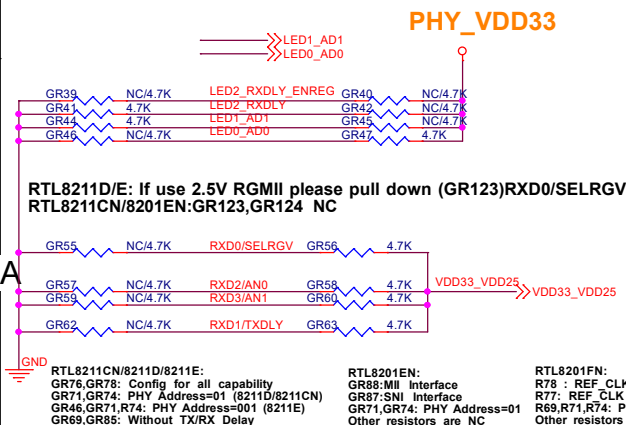


## RGMII/RMII

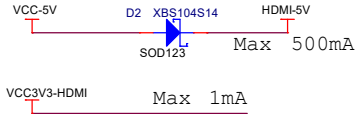
**Place filter network close to RX\_CLK.  
Reserved for EMI**



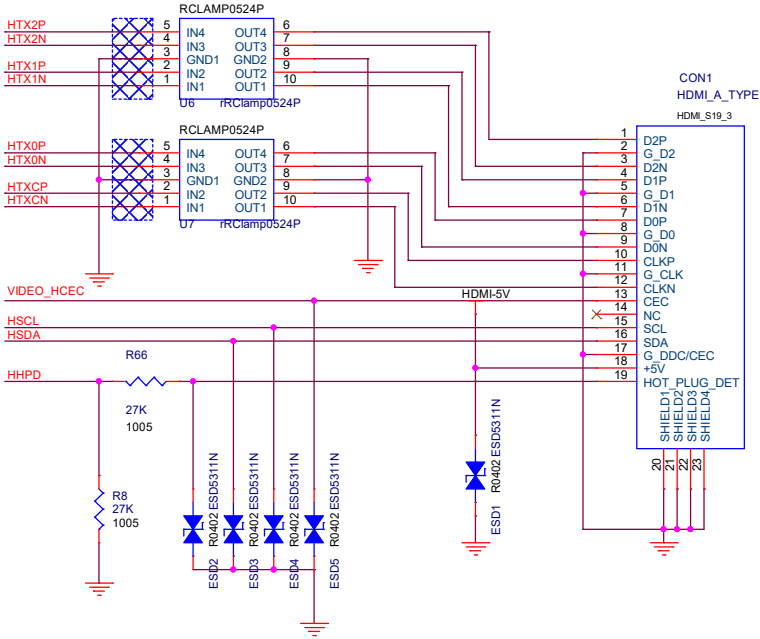
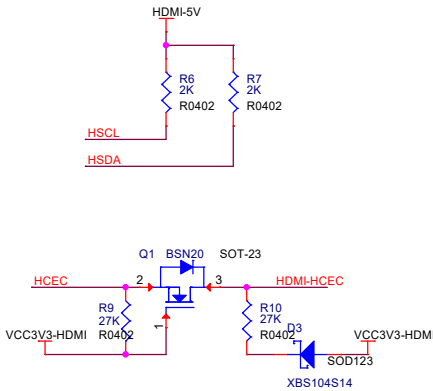
## Configuration Setting



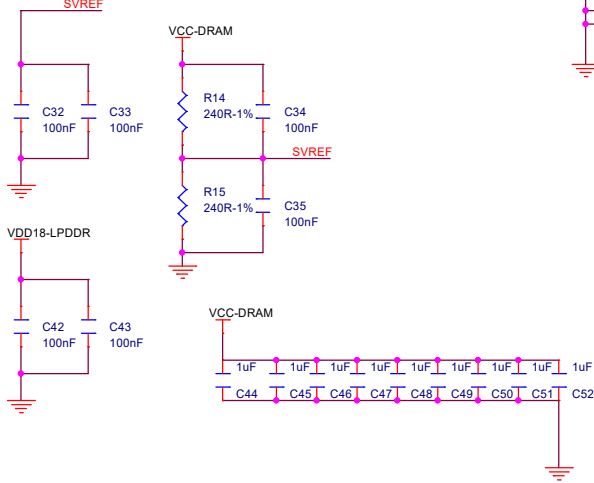
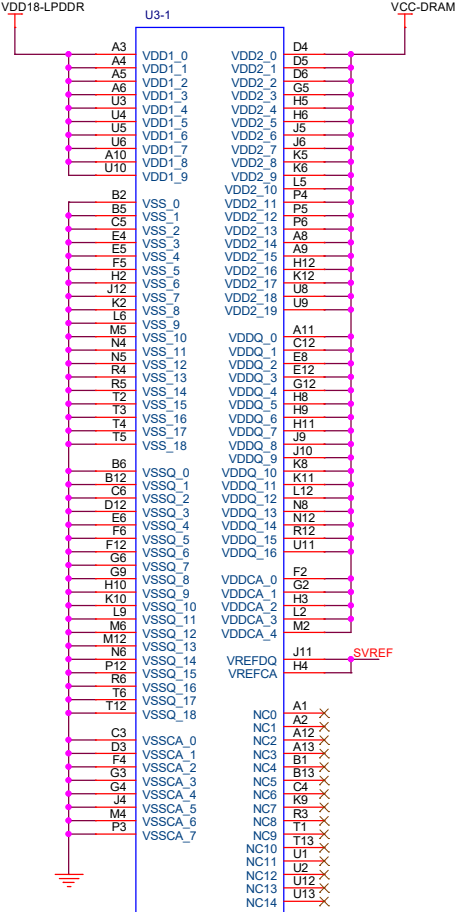
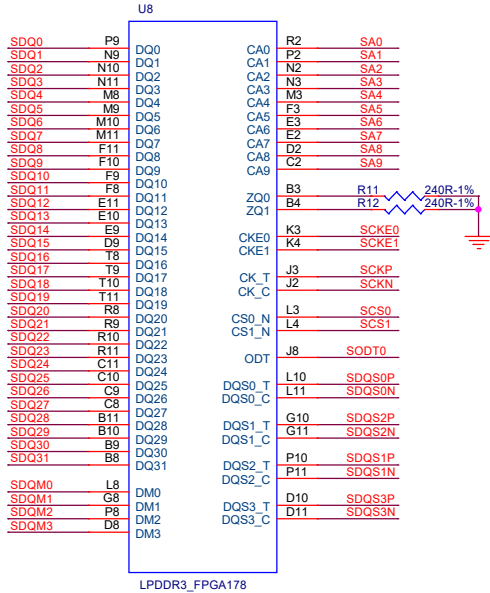
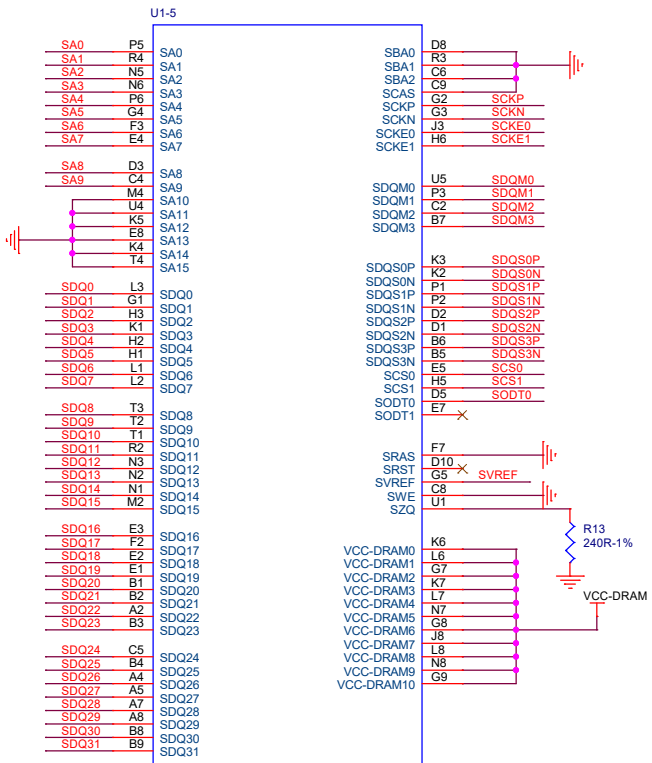
HDMI



Differential pairs  
Z0= 100 ohm

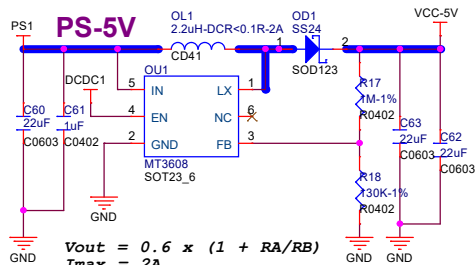
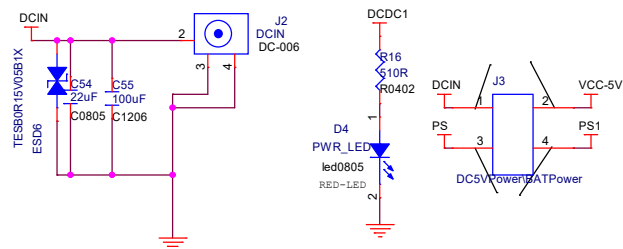


LPDDR3 32X1



# Power

# DC JACK SIZE : (Diameter) 1.3 mm

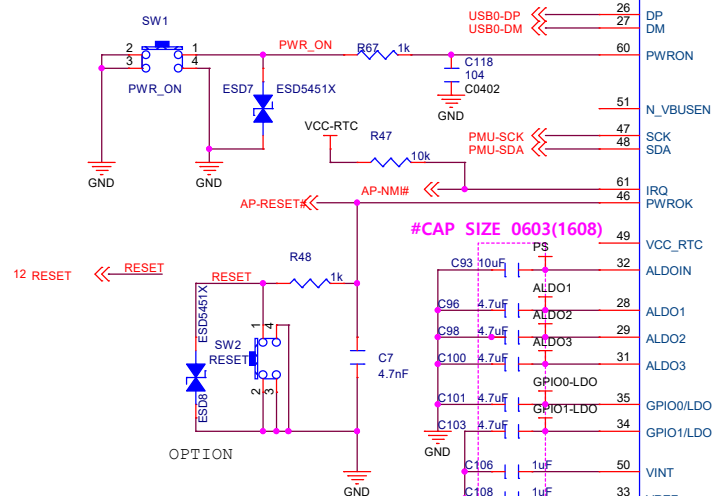


$$V_{out} = 0.6 \times (1 + R_A/R_B)$$

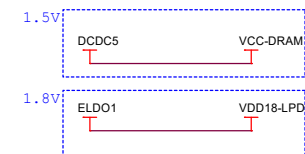
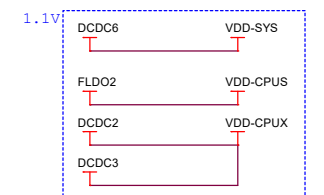
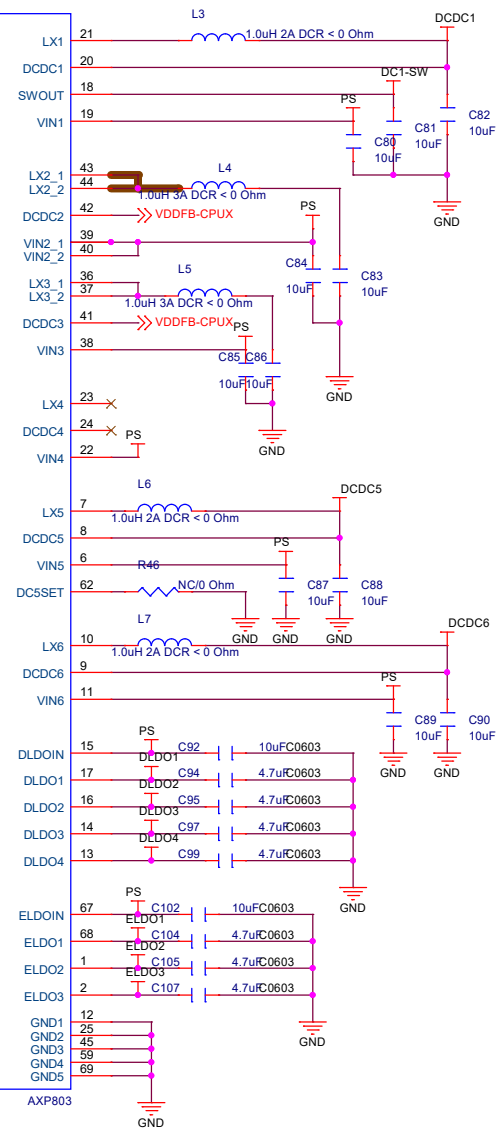
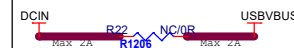
$$I_{max} = 2A$$

PWR\_ON << PWR\_ON

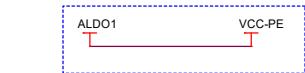
## # BATTERY BLOCK WAS REMOVED



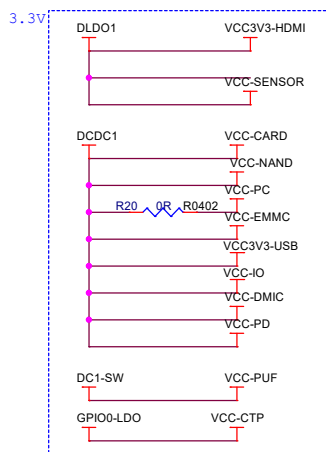
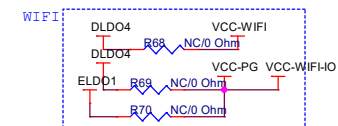
**DCIN**



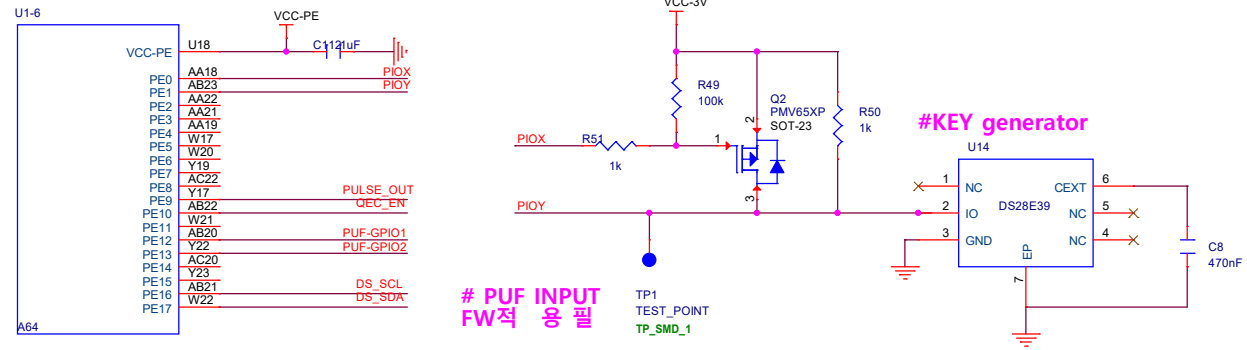
PUF/QEC/HSM



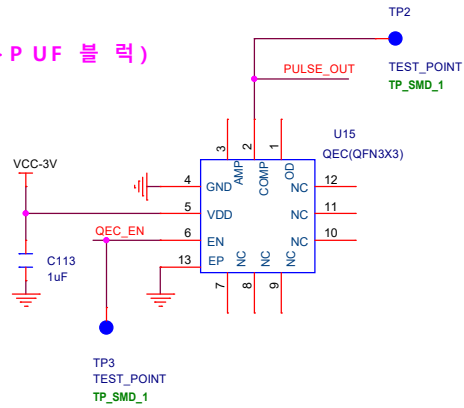
WIFI



# PUF/QEC/HSM

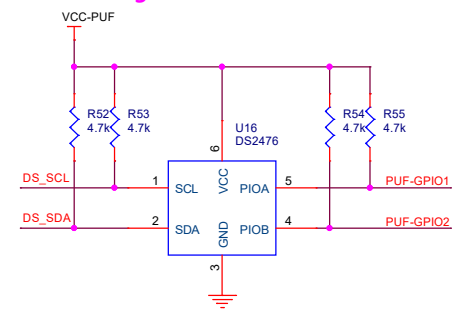


# (CAMERA 블럭 >> PUF 블럭)  
블럭 변경



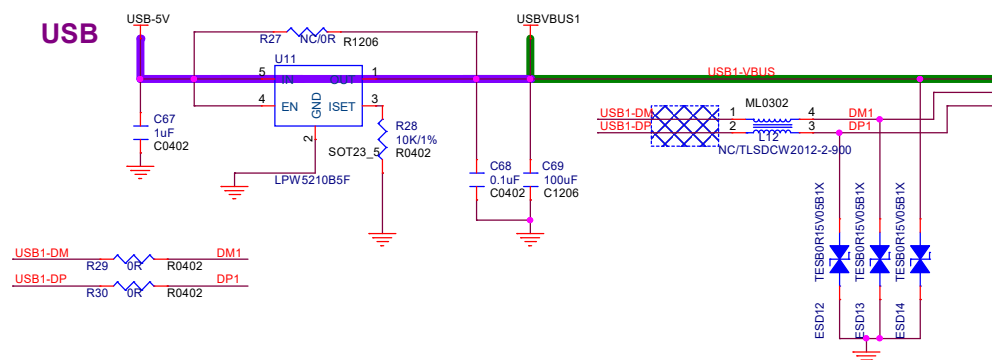
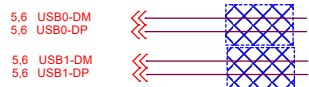
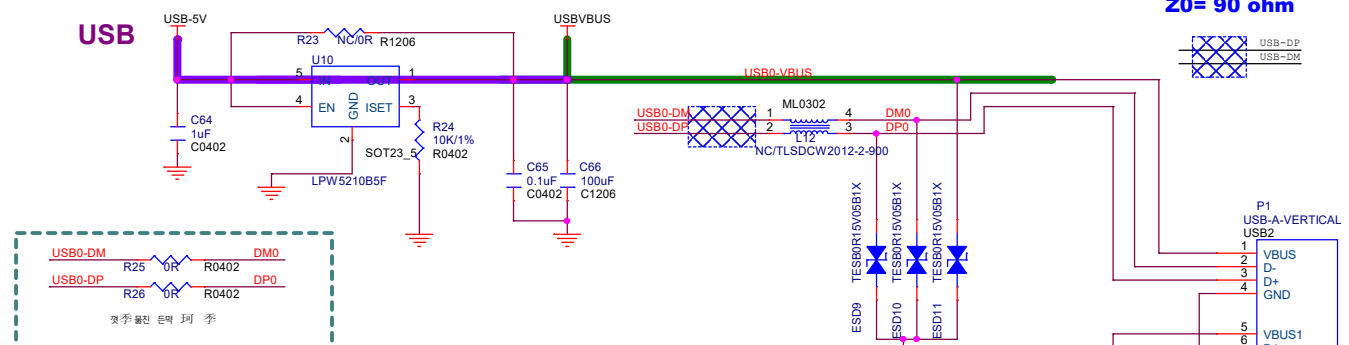
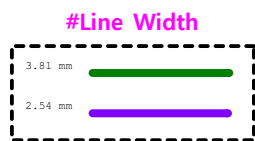
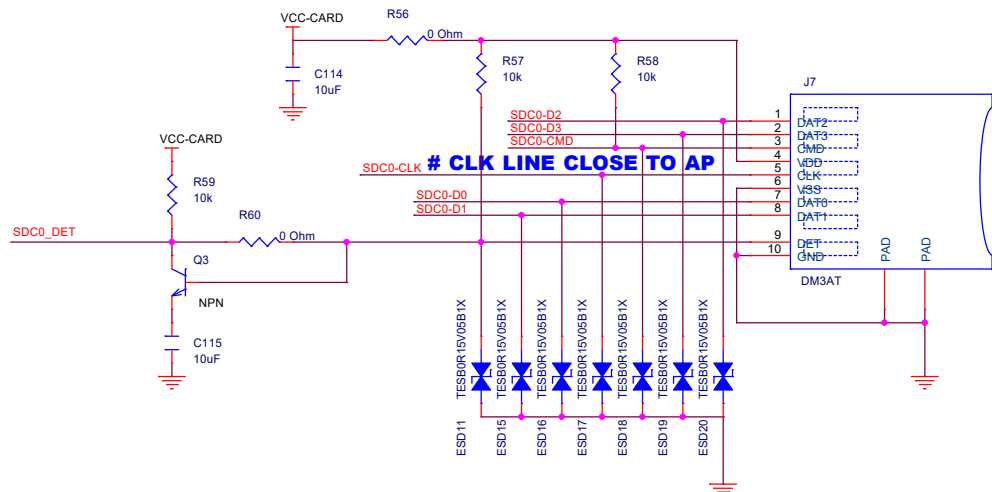
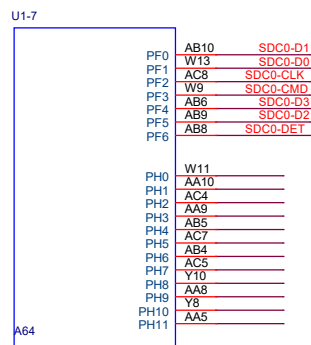
#Quantum Entropy nonce generator

# KEY storage and secure host controller



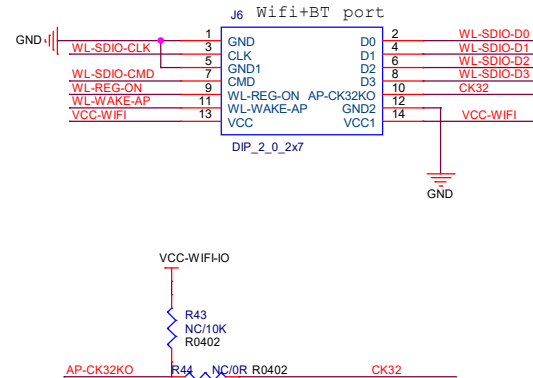
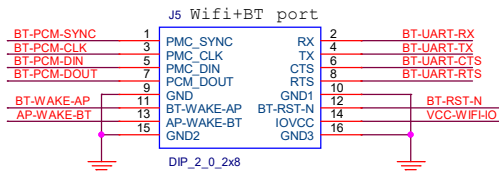
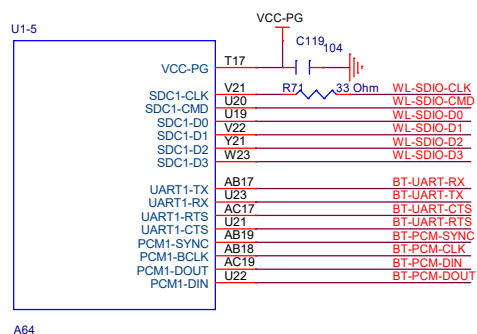


## USB / SD-CARD



The ESD part's parasitic capacitance  $< 5\text{pF}$ .

## WiFi/BT



## WiFi/BT - MODULE

