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A high-efficiency full-wave CMOS rectifying charge pump for RF energy harvesting applications

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ABSTRACT

A high-efficiency integrated full-wave CMOS rectifying charge pump for radio-frequency (RF) energy harvesting was designed. By using the commercially available 40 nm CMOS process, low-voltage operation as low as 0.4 V was achieved by adopting body-connected PMOS diodes as the rectifying diodes and as switches for capacitor charging pump. A full-wave rectifying configuration was used to enhance the power conversion efficiency (PCE) of the converter. Simulation results indicate that the circuit can achieve a power efficiency of over 50.0% for an input voltage larger than 0.4 V of a single narrow band 900 MHz RF signal. Although the loading characteristics of the primitive charge pump, especially for 0.4 V input which is just above the specific threshold voltage of the PMOS, is rather poor, and a large voltage drop due to the conduction loss was found when the load current increases, it may still be acceptable for battery charging applications. A regulation circuit based on the charge pump switching control was then proposed to improve the loading characteristics.

1. Introduction

Radio frequency (RF) energy harvesting has recently attracted much attention because of the need for powering some distribution sensor networks or some remote electronic setups [1–4]. These devices, were powered by conventional batteries have limited lifetimes. In addition, the cost of battery replacement for such large number of remote sensor nodes could be very high. A cost effective solution for this issue is to power the devices with sustainable power sources such as RF signals [1–4]. A device could operate for whole life if it is powered with an RF energy harvesting system. RF energy harvesting has been quite successful for RFID applications [5–8] and now it becomes feasible as a regular source for low-power devices such as remote controllers for home appliances, wearable components, body area networks, and remote sensor networks, etc. Indeed the realization ambient for RF powered systems is better ever because of the widely available and almost non-stop RF sources around the city, offices and domestics. These readily available sources include TV, radio, mobile phone signals, and most importantly the widely installed WLAN routers in recent years. Although RF sources are ubiquitous now, the energy levels of these sources are quite low in general. Unlike the RFID applications where the devices are powered instantaneously by a high-power RF generator instead of taking from ambient continuously, the power level of the RF products we used such as WiFi routers and mobile communication systems is usually less than 0.1 W because of safety considerations as governed by FCC [9]. The power attenuates when it transports over the air and passes through some obstacles. The available energy for the harvesting system is usually in the range of some tens to hundred microwatts [10]. Hence, the power efficiencies of every segments of the system design are always important considerations.

An RF energy harvesting system consists of an antenna, matching network, RF-to-DC rectifier, and energy storage and management system (see Fig. 1) [1]. An efficient collection of the RF power requires a high performance antenna. However, a big and comprehensive antenna is not realistic in most applications. Patch antennas, being compact and low cost, are good options for most applications. However, patch antennas have the disadvantages of narrow bandwidth, low efficiency, and low gain. The available incident power is even lower in that case. Thus, the power efficiency of the converter circuit is critical in obtaining sufficient power while maintaining the antenna small and inexpensive. As shown in Fig. 1, the main part of the circuit is the rectifying and voltage step-up circuit. The convention implementation is to use a simple half-wave rectifying using Schottky diode and to step up the voltage with a Villard voltage multiplier which is constituted by capacitors and Schottky diodes also. Schottky diode has the advantages of low turn-on voltage ($\sim$ 0.2 V) and fast speed. The major disadvantage is that it is difficult to be integrated

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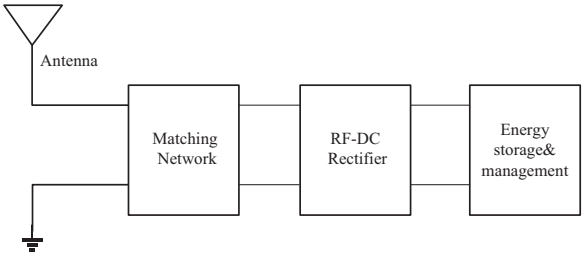

Fig. 1. Schematic of a typical RF energy harvesting system.

with the mainstream CMOS circuits. In addition, the power conversion efficiency drops dramatically when the rectifiers are cascaded using the Villard structure. The power conversion efficiency is typically less than 40% for this kind of converters. To reduce the costs and to make use of the standard CMOS compatible process so as to keep the harvesting system compact and inexpensive, fully CMOS based systems are preferred. The major difficulty for standard CMOS realization of the RF signal detection is the "high" threshold voltages which are governed by the noise margins of digital circuits. An RF energy harvesting circuit based on a Dickson charge pump configuration was developed and realized using the 90 nm CMOS technology [2]. In this structure, the low-voltage operation was achieved by using a threshold voltage compensation technique. Using a half-wave rectifying configuration, a rectifying efficiency of 11% was obtained [2]. This work also aims at the developing of an integrated RF harvesting system based on the standard CMOS process. In this paper, we use the low threshold voltage PMOS as the rectifying devices. To further reduce the operation voltage, instead of using threshold voltage compensation through the gate terminal, we adopt a bulk or body connection structure, which can turn the diode-connected MOS transistors on at lower voltages. To achieve higher power conversion efficiency, a complementary full-wave configuration that converts RF signal both at positive and negative cycles is proposed. Section 2 presents the details of this design and the simulation validation based on a commercial 40-nm CMOS process will be shown in Section 3.

2. Circuit configuration and design methodologies

In order to integrate with other circuits, diode-connected MOS transistors were used as rectifying devices. In a typical CMOS process for logic circuits, a PMOS transistor has a slightly smaller magnitude of threshold voltage, $|V_{TH}|$, than that of the NMOS ones, thus we use the diode-connected PMOS for RF signal rectifying applications. In the present work, the turn-on voltage of this diode, equal to V_{TH}, is about -0.39 V for the given CMOS process. Assuming the RF power being collected from antenna is 0.4 mW, the antenna being perfectly matched with the converter, and the characteristic impedance be 50 Ω, the voltage at the input of converter is about 0.4 V which is just above the threshold voltage of the PMOS diode. Under this situation, the diode current is very small and the charge pump will be very inefficient. To reduce the turn-on voltage of the diode, many schemes were proposed [11–14]. An internal threshold voltage cancellation, by biasing the diode with output voltage, was proposed [11]. This method is able to enhance the input impedance matching also. A double chain rectifier scheme using an auxiliary rectifier chain to bias the diode was also attempted [12]. Self V_{TH} cancellation technique was also proposed [13]. In this work, we use body bias to lower the turn-on voltage and that was done simply by connecting the body to the drain. This simple method can reduce the threshold voltage by about 20 mV. Fig. 2 compares the current–voltage characteristics

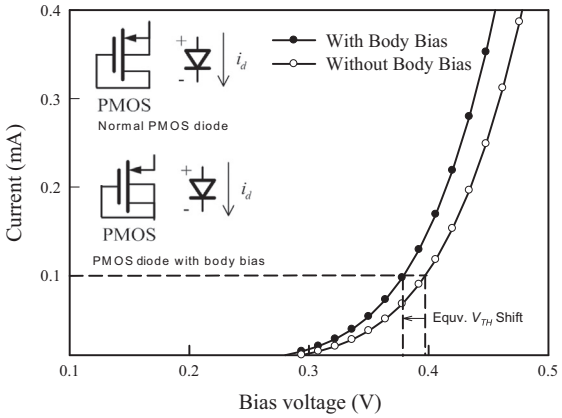

Fig. 2. Comparison of forward current–voltage characteristics of a normal diode-connected PMOS and a body-biased PMOS diode.

of the normal diode-connected (with body connected to source) PMOS transistor and with body bias (body connected to drain). The aspect ratio for both cases are the same which is $W/L=20$ μm/60 nm. As shown in Fig. 2, the same current level at the defined threshold voltage (0.39 V) can be achieved at 0.37 if the body-connection is employed.

In this work, the voltage multiplication is done by using Dickson charge pump configuration [15–17]. Depending on the number of stages and coupling capacitance, the output voltage of a Dickson charge pump can be modeled by

$$V_{OUT}=V_{IN}+N\left[\left(\frac{C}{C+C_S}\right)V_\phi-V_D\right]-V_D-\frac{NI_{OUT}}{(C+C_S)f} \quad (1)$$

where V_{IN} is the input voltage amplitude, $V\phi$, N are the output voltage and the number of stage of charge pump, respectively; C is coupling capacitance, C_S is stray capacitance of the MOS switches, V_D is the forward bias diode voltage, I_{OUT} is the output current and f is the clock frequency.

The Dickson charge pump needs a clock to control the capacitor charging alternately [15]. In this work, the clock signal was replaced with an RF signal. The circuit configuration is depicted in Fig. 3(a). The high-frequency operation can enhance the conversion efficiency and the loading characteristic. Note that we used diode-connected PMOS transistors as the rectifying diode and switches for capacitor charging control. The transistors are switched on during positive input phases and switched off during negative input phases. Assuming the transistors are operated at saturation region when they are turned on, the DC output voltage V_{OUT+} can be expressed as:

$$V_{OUT+}=N\left(V_{IN}-|V_{TH}|-\sqrt{\frac{2I_D}{\mu C_{OX}(W/L)}}\right) \quad (2)$$

where I_D is the current of MOS transistor in saturation region. Similarly, we can also design a complementary Dickson charge pump that is operated at negative input voltages (see Fig. 3(b)). By combining both positive and negative rectifying charge pumps together, we have the push–pull structure, as shown in Fig. 4, that operates at both positive and negative phases of input signal. In this design all the PMOS transistors were set in same size and all the capacitance values were also the same. This circuit functions well at input peak value of 0.4 V where the threshold voltage of the PMOS transistors is -0.39 V.

The circuit operation is explained as follows. For positive signal cycle, transistor MP_{1+} is on, and the current (through MP_{1+}) charges up capacitor C_{1+} to a value equal to $V_M-|V_{TH}|$, here V_M is the peak voltage of the RF input. At negative cycle, transistor MP_{2+}

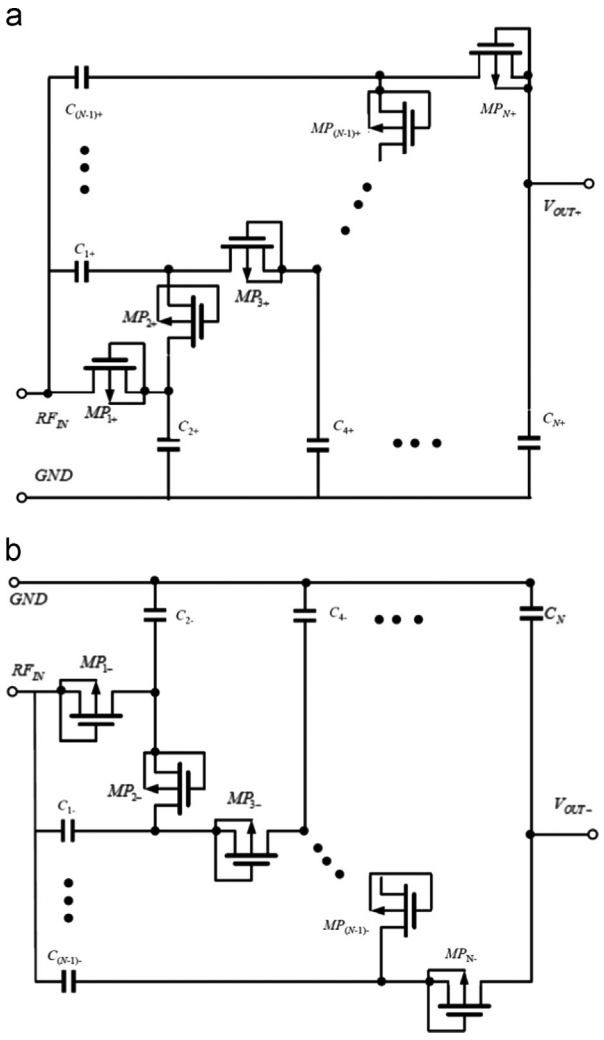

Fig. 3. A Dickson charge pump/rectifier realized with body-connected PMOS transistors: (a) positive input; and (b) negative input.

turns on and the current, I_{MP2+}, flows from C_{2+} to C_{1+}. The voltage across C_{1+} will then be $2(V_M-|V_{TH}|)$. Since the negative portion of the circuit operates in the complementary way, the voltage across C_{1-} will be $-2(V_M-|V_{TH}|)$. The subsequence stages further step the DC voltage in C_{1+} and C_{1-}. For an N-stage circuit, the final output can be approximated by $V_{OUT}=2N(V_M-|V_{TH}|)$ if the losses are negligible. Yet the output voltage can modeled more precisely, after considering the approximation given in (2), by

$$V_{OUT}=V_{OUT+}-V_{OUT-}$$
$$=2N\left(V_{IN}-|V_{TH}|-\sqrt{\frac{2I_D}{\mu C_{OX}(W/L)}}\right) \quad (3)$$

when taking the conduction loss into account.

3. Simulation results and discussion

The operation of the proposed full-wave CMOS RF-DC rectifying voltage stepper was confirmed with Spectre simulation using a commercial 40 nm CMOS process. All transistors are in same size with $W/L=20\ \mu m/60$ nm. The input signal was a narrow band 900 MHz RF signal with amplitude from 0.4 to 0.55 V. To achieve a reasonable DC voltage for biasing the mainstream digital circuits or for battery charging applications, the preferable output voltage

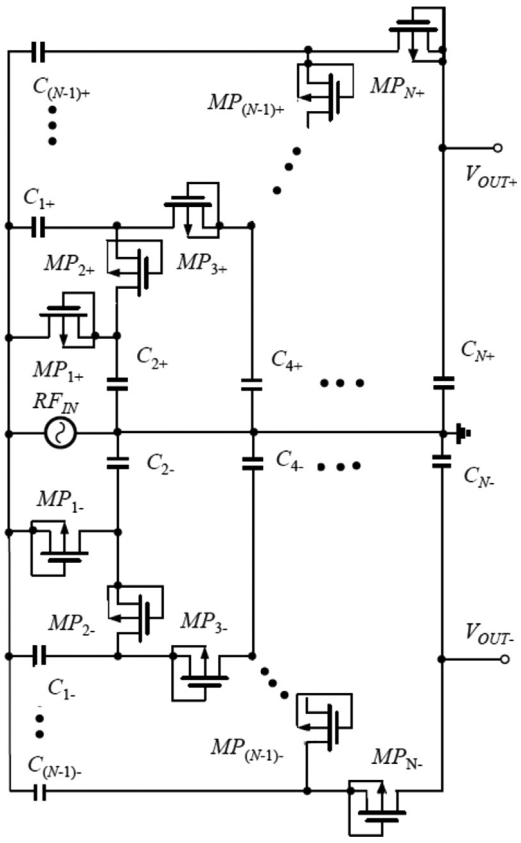

Fig. 4. Proposed high-efficiency full-wave CMOS RF-DC rectifying charge pump developed in this work.

of the system should be above 1.3 V. The threshold voltages are 0.45 V and −0.39 V for NMOS and PMOS, respectively, for the 40 nm process we used, it imposes great difficulty in realizing the system. For the case of 0.4 V input, we need seven stages (*both positive and negative half cycles*) to achieve this voltage level as the input voltage is slightly lower than the threshold voltage of the MOS transistor. Under normal bias, the input voltage is so close to the threshold voltage of the CMOS transistor that the power conversion efficiency will be very low. In this work, we adopted the body biasing scheme to turn on the transistor at a voltage lower than the threshold. Under this condition, the transistors MP_{1+} and MP_{1-} (see Fig. 4) were in fact operated in weak linear region. The dynamic resistance of MP_{1+} and MP_{1-} were quite large and that produced a larger power loss. However, our circuit is still able to function well regardless the poor conversion ratio. Fig. 5 shows the transient response of the circuit for the case of 0.4 V input. The circuit was able to settle at a final DC voltage of 1.34 V, a double of both the –ve output and the +ve output of the circuit, within 3.5 μs.

Fig. 6(a) shows the loading characteristics of the proposed converter at four signal levels of 0.4 V, 0.45 V, 0.5 V and 0.55 V. According to the figures, the output and loading characteristics were improved greatly when the input signal level increases. Alternatively, if a smaller threshold voltage is availbale, the characteristics can be significantly improved. Fig. 6(b) shows some simulation results using a low-voltage process where the threshold voltage for PMOS is −0.37 V. The circuit functions well for input voltage as low as 0.37 V. As shown in Fig. 6(a), the output voltage drops to about 0.8 V when the loading current increases to 19 μA when the input voltage is 0.4 V. For higher input voltages, a great improvement on the output voltage and the loading characteristics. For 0.55 V input, for example, the output voltage

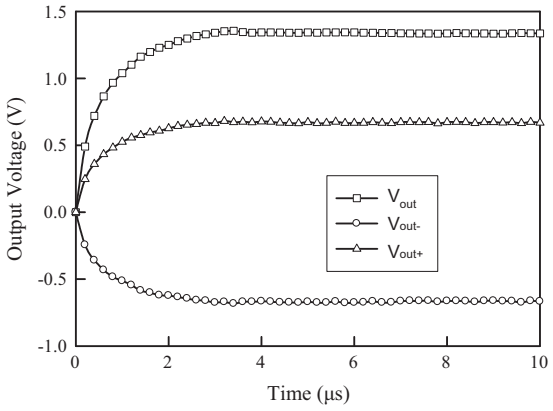

Fig. 5. Transient response of the RF-DC converter showing the output of the circuit reaches final steady voltage of 1.34 V within 3.5 μs.

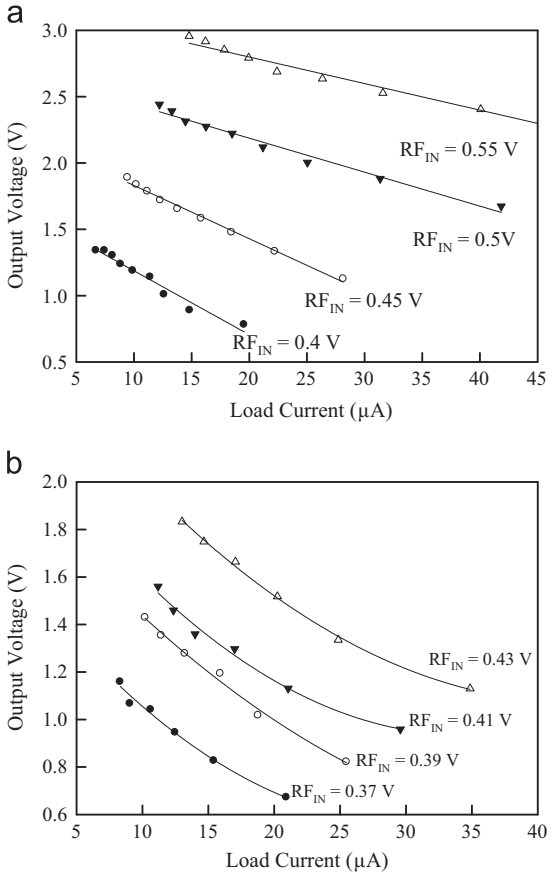

Fig. 6. Loading characteristics of the converters for a 900 MHz RF input signal with different amplitudes simulated using: (a) the standard logic process with PMOS threshold voltage of 0.39 V; and (b) a low-voltage process with PMOS threshold voltage of 0.36 V.

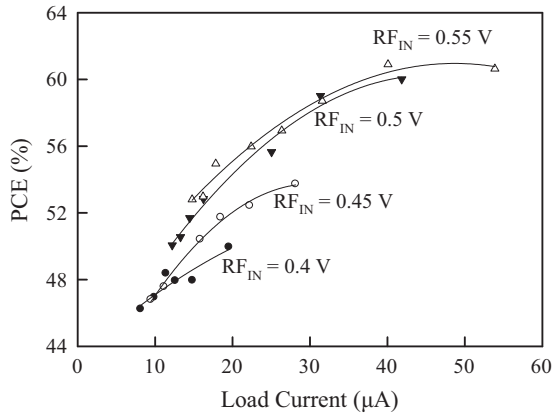

Fig. 7. Plot of power conversion efficiency as a function of load current for the 0.4 V, 0.45 V, 0.5 V and 0.55 V input cases.

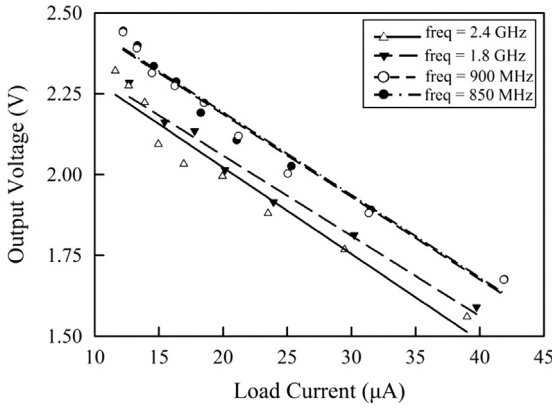

Fig. 8. Loading characteristics of the converter for 850 MHz, 900 MHz, 1.8 GHz and 2.4 GHz RF input signal with amplitude equals to 0.5 V.

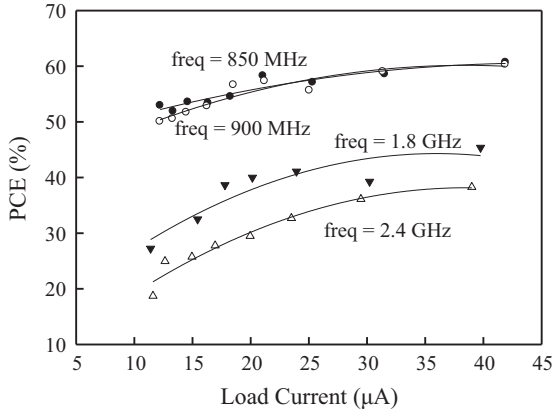

Fig. 9. Plot of power conversion efficiency as a function of load current for RF signals with frequency of 850 MHz, 900 MHz, 1.8 GHz and 2.4 GHz. The singal amplitude is 0.5 V.

reaches 2.96 V for load current of 14.8 μA and drops by 15% when the load current is doubled. Note that these figures are only used to demonstrate the step up capability of the proposed circuit under different input voltages. It is noted that the output varies so large for a small variation on the input that it is not practical without a regulating circuit. In fact, for input voltages larger than 0.5 V, the output voltage is much larger than the desirable output voltage and is larger than the supply voltage of 40 nm CMOS technology we used and will cause both drain and gate oxide to break down. Thus, if the input voltage is higher than 0.5 V, the number of stages should be reduced. Meanwhile, it is noted that the loading characteristic is still not good enough for most applications. Both issues mentioned above can be solved by introducing an output regulating stage [17, 18], such as the pulse-skipping modulation technique. At small loading currents, a feedback signal, through the clock control, will shut some stages of the converter down. That is, the average power delivering to the load can be adjusted so that the output voltage will remain unchanged at different load currents. In addition, a wider range

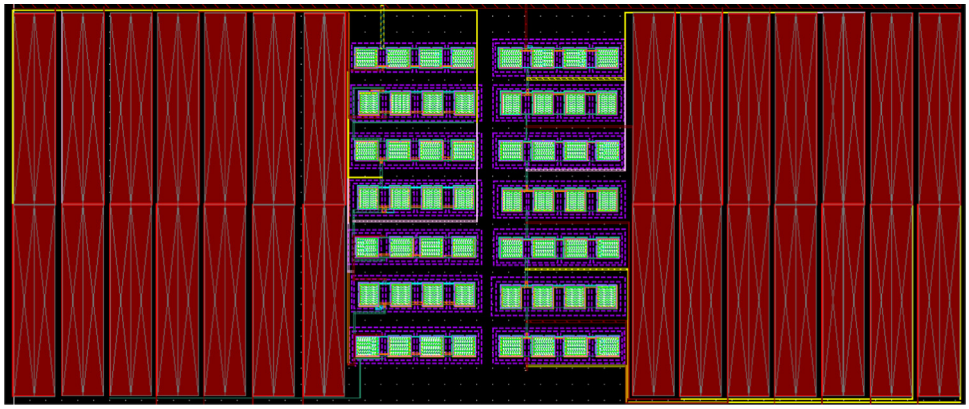

Fig. 10. Layout of the designed full-wave CMOS rectifying charge pump.

of input power range will be allowable in this kind of configuration. The switching loss can also be reduced and the power efficiency at small load current can be also improved [18].

Fig. 7 shows the PCE as a function of load current. The power efficiency maintains at over 48% for load current over 13 μA for 0.4 V input. The efficiency is low because the input voltage is very close to the threshold voltage of PMOS transistors we used. The transistors are biased at very close to the threshold voltage and a large conduction loss of the MOS diode/switch in the input rectifying stages were encountered. The PCE can be greatly improved if the RF source voltage is higher or the threshold voltage of the transistor can be reduced. For instant, the efficiency was significantly improved for 0.55 V input. As shown in Fig. 7, the power efficiency increases to over 56% for 20 μA loading current for 0.55 V input. Again, power efficiency can be further improved by incorporating the active regulator at the output of the charge pump which is under development. On the other hand, since the number of stages is large, it may be more power and area efficient by adopting an exponential topology for stepping up the voltages [19].

Fig. 8 shows the loading characteristics of the proposed converter at four signal frequencies of 850 MHz, 900 MHz, 1.8 GHz and 2.4 GHz. According to this figure, the loading characteristics deteriorate for higher operation frequency because of the losses of parasitic capacitances of the MOS switches. For input frequencies in the range of 850–900 MHz, the output voltage drops about 0.12 V when the loading current increases to about 21 μA. However, for input frequency at 1.8 and 2.4 GHz, the loading characteristics become worse. The output voltage drops to about 2 V when the loading current increases to about 20 μA. Fig. 9 shows the PCE as a function of load current with different signal frequencies. The power efficiency maintains at over 50% for load current over 12 μA for 850 and 900 MHz inputs. For 1.8 GHz input, the efficiency can maintains at over about 44% at large load current of 40 μA. For 2.4 GHz, it is even poor.

The layout of the proposed full-wave CMOS rectifying charge pump is shown in Fig. 10. The active area, which is mainly occupied by MOM capacitors, is about 0.0408 mm^2 (298 μm × 137 μm). The layout was designed using the design rules as given in a commercial 40 nm CMOS process. The specified supply voltage is 1.2 V. Actual measurements on transistors fabricated using the same technology indicate that the transistors can still function well for gate and drain voltage of 1.35 V. However, to avoid possible drain punchthrough at an output voltage that is larger than the specified supply voltage, we choose a slightly longer channel length of 60 nm for the design. A post-layout simulation for 900 MHz 0.4 V input yielded output voltage of 1.26 V and PCE of 44.75%.

4. Conclusions

RF energy harvesting has become an attractive and viable power source for low-power electronic devices. One of the major challenges is the system integration with the available CMOS technology. In this work, a high-efficiency integrated full-wave CMOS DC rectifying charge pump for radio-frequency (RF) energy harvesting was designed. By using the commercially available 40 nm CMOS process, low-voltage operation (~ 0.4 V) was achieved by adopting body-connected PMOS diodes as the rectifying diodes and as the switches for the charge pump. A full-wave rectifying configuration was used to enhance the power conversion efficiency of the converter. Simulation results indicate that the circuit can be operated at 0.4 V input and perform quite well with power efficiency of over 72% at 0.5 V input from a narrow band 900 MHz RF source. This circuit can be used as a sustainable voltage source for charging a battery in some low-power electronic products.

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References

[1] M. Arrawatia, V. Diddi, H. Kochar, M.S. Baghini, and G. Kumar, An integrated CMOS RF energy harvester with differential microstrip antenna and on-chip charger, in: Proceedings of the 25th International Conference on VLSI Design, 2012, pp. 209–214.
[2] G. Papotto, F. Carrara, G. Palmisano, A 90-nm CMOS threshold-compensated RF energy harvester, IEEE J. Solid-State Circuits 46 (2011) 1985–1997.
[3] P.C.P. Chao, C.-T. Chiang, T.-C. Huang, and C.-K. Chang, Achieving maximum power efficiency of a novel rectifier charge pump by impedance matching in an energy harvester suited for self-powered sensors, in: Proceedings of the IEEE Sensors, 2013, pp. 1–4.
[4] T. Le, K. Mayaram, T.S. Fiez, Efficient far-field radio frequency energy harvesting for passively powered sensor networks, IEEE J. Solid-State Circuits 43 (2008) 1287–1302.
[5] K. Kotani, A. Sasaki, T. Ito, High-efficiency differential-drive CMOS rectifier for UHF RFIDs, IEEE J. Solid-State Circuits 44 (2009) 3011–3018.
[6] F. Qiuyun, N. Gay, C. Bansleben, R. Hildebrand, M. Heiss, A. Turke, Optimization of the NMOS and PMOS gate cross-connected rectifier for RF power extraction in RFID applications, in: Proceedings of the Asia-Pacific Microwave Conference, 2008, pp. 1–4.
[7] D.S. Liu, F.B. Li, X.C. Zou, Y. Liu, X.M. Hui, X.F. Tao, New analysis and design of a RF rectifier for RFID and implantable devices, Sensors 11 (2011) 6494–6508.
[8] R.E. Barnett, J. Liu, S. Lazar, A RF to DC voltage conversion model for multi-stage rectifiers in UHF RFID transponders, IEEE J. Solid-State Circuits 44 (2009) 354–370.

[9] Federal Communications Commission, Codes of Regulation, U.S., Part 15, Low Power Broadcasting, available at ⟨www.fcc.gov⟩.
[10] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, S. Otaka, A 950-MHz rectifier circuit for sensor network tags with 10-m distance, IEEE J. Solid-State Circuits 41 (2006) 35–41.
[11] H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, A passive UHF RF identification CMOS tag IC using ferroelectric RAM in 0.35-μm technology, IEEE J. Solid-State Circuits 42 (2007) 101–110.
[12] H. Lin, K.H. Chang, & S.C. Wong, Novel high positive and negative pumping circuits for low supply voltage, in: Proceedings of the IEEE Circuits and Systems, 1999, pp. 238–241.
[13] K. Kotani, T. Ito, Self-Vth-cancellation high-efficiency CMOS rectifier circuit for UHF RFIDs, IEICE Trans. Electron. E92-C (2009) 153–160.
[14] G. Papotto, F. Carrara, G. Palmisano, A 90-nm CMOS threshold-compensated RF energy harvester, IEEE J. Solid-State Circuits 46 (2011) 1958–1997.
[15] O.-Y. Wong, H. Wong, C.-W. Kok, W.-S. Tam, Dynamic analysis of two-phase switched-capacitor DC–DC converters, IEEE Trans. Power Electron 29 (2014) 302–317.
[16] O.-Y. Wong, H. Wong, W.-S. Tam, C.-W. Kok, Modelling of maximum power efficiency of charge pump circuits, IET Electron. Lett. 50 (2014) 1233–1234.
[17] T. Tanzawa, S. Atsumi, Optimization of word-line booster circuits for low-voltage flash memories, IEEE J. Solid-State Circuit 34 (1999) 1091–1098.
[18] H. Chung, B.O. and A. Ioinovici, Switched-capacitor-based DC-to-DC converter with improved input current waveform, in: Proceedings of the IEEE International Symposium on Circuits Systems, 1996, pp. 541–544.
[19] O.-Y. Wong, H. Wong, C.-W. Kok, W.-S. Tam, A dynamic-biasing $4\times$ charge pump based on exponential topology, J. Circuit Theory Appl. 43 (2015) 401–414.