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Short communication

A 200 MHz CMOS rectifier with wide power dynamic range and high-sensitivity for RF energy harvesting

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ABSTRACT

This paper presents a high-efficiency CMOS rectifier with wide dynamic range (DR) and high sensitivity aimed at radio-frequency energy harvesting (RFEH). A nonlinear DC bias is applied to the gate of the rectifying transistors in the proposed cross-coupled rectifier. This is not only beneficial for enhancing the rectifying transistor's forward current during low-power operation but also suppressing the leakage loss during high-power operation. Therefore, the power conversion efficiency (PCE) and sensitivity of the rectifier can be improved significantly. Besides, the DR of the proposed rectifier can be extended. For validation, a prototype is designed and simulated in a 40-nm CMOS process. The simulated results show that the proposed rectifier achieves a 26.7 dB (from -32.1 to -5.4 dBm) for the PCE > 40%. In addition, the proposed rectifier reaches a peak PCE of 88.6%, and a sensitivity of -19.3 dBm when the output is 1 V. The proposed rectifier is a good candidate for being used in RFEH systems.

1. Introduction

Given that the Internet of Things (IoT) is experiencing a rapid process of development, the application of wireless sensor networks (WSN) has become increasingly common. However, the high costs associated with manual maintenance pose a challenge and potential impracticality for the use of cable connections or batteries to power large-scale WSN devices [1]. Fig. 1 presents a schematic block diagram depicting a radio-frequency energy harvesting (RFEH) system designed for WSN. It significantly reduces the reliance of devices on batteries and extends their operational lifespan [2]. This advancement paves the way for the large-scale deployment of WSNs [3–5]. The rectifier, which is capable of transforming RF power to DC power, plays a crucial role in the RFEH system. Subsequently, the DC–DC converter processes this DC voltage to provide an optimal supply for the WSN devices.

The Dickson and the cross-coupled differential-drive (CCDD), which can be seen in Fig. 2(a) and (b), are the commonly used topologies for CMOS rectifiers. The operating principle of these two rectifiers are discussed in [6,7], respectively. During high power operation, the Dickson rectifier can achieve high PCE. However, when the input power is low, it suffers from a high startup voltage, which leads to reduced PCE and lower sensitivity. Specifically, the sensitivity refers to the least input power when produce a voltage of 1 V. Conversely, the CCDD rectifier employs a dynamic compensation technique. This compensation strategy enhances the conduction of rectifying transistors

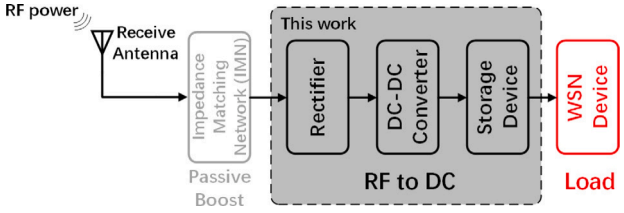

Fig. 1. Block diagram of a typical RFEH system in wireless sensor networks.

and reduces the threshold voltage, thereby enabling it to achieve higher PCE and sensitivity. However, a significant power loss occurs due to reverse leakage, which results in a decline in PCE and a reduction in the dynamic range (DR). We describe the input power range in which the power conversion efficiency (PCE) is above 40% as DR. Fig. 2(c) and (d) illustrate the PCE and the output voltage varying with the input power for both Dickson and CCDD rectifiers, respectively. In general, the CCDD rectifier is widely used under low power requirements due to its self-starting and low threshold voltage characteristics.

Lately, various techniques have been applied for the RF rectifier to enhance its performance. In [8], the double-sided rectifier is proposed to compensate for the gate of the rectifying transistors separately. This structure achieves significant performance improvements in terms of

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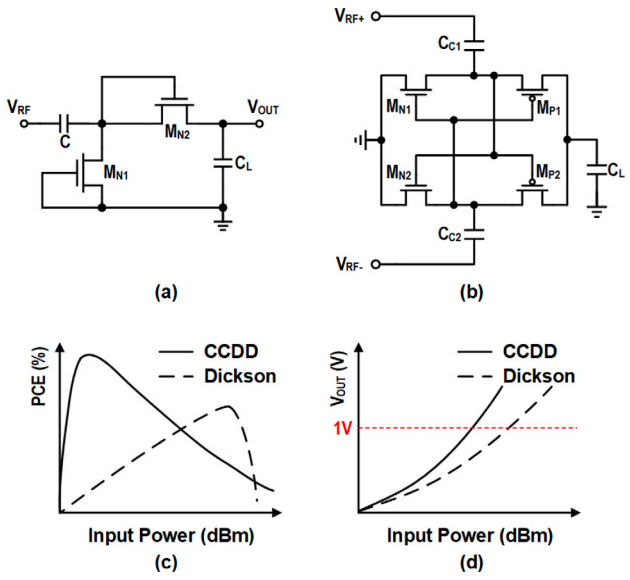

Fig. 2. Schematics of (a) Dickson and (b) CCDD rectifiers, (c) their PCE and (d) output voltage versus different input power.

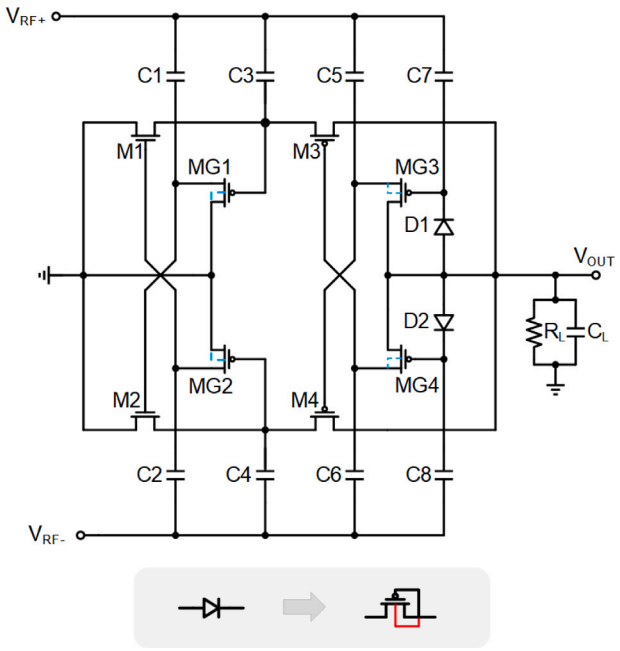

Fig. 3. Schematic of the proposed rectifier.

PCE and sensitivity. Under low power condition, the diode-connected PMOS transistors remain off, resulting in the DC bias of the rectifying transistors to be zero. This enhances the forward current of the PMOS rectifying transistors. The diode-connected PMOS transistors turn on as the input power further increases, which elevates the gate DC bias of the PMOS rectifying transistors. This results in a decrease in reverse leakage, thereby increasing the net charge delivered to the load, which boosts both PCE and sensitivity. Furthermore, [9] provides a dynamic and static bias compensation technique to enhance PCE and sensitivity. This innovative approach introduces a voltage from previous rectifier stage to adjust the gate DC bias of the current stage, enhancing the PCE during low input power. However, significant leakage at high input power results in a rapid decline in PCE, and the DR is consequently limited. Moreover, the gate voltage boosting technique [10] is applied to the all-NMOS architecture. It enhances the conductivity of the rectifying NMOS transistors significantly during low power operation.

In this article, we present a dynamically compensation technique for the gates of the transistors used for rectification, enhancing both low-power and high-power performances. We introduce and analyze the operating mechanism of the proposed design in Section 2. In Section 3, we offer the results obtained from the simulation, make a comparison, and have a discussion. we provide the simulation results, comparison, and discussion. Finally, we summarize some conclusions in Section 4.

2. Proposed rectifier

The schematic of the proposed rectifier as shown in Fig. 3. It comprises four transistors that are used for rectification (M1-4) which are low-threshold, four low-threshold PMOS transistors (MG1-4) for providing nonlinear gate DC bias voltage to M1-4, two diode-connected PMOS transistors (D1,2) are connected to the gate of MG3,4. It is noted that the substrate of D1 and D2 are connected to the drain for reducing reverse current. Additionally, there are six biasing capacitors (C1,2,5,6,7,8) and two charging capacitors (C3,4).

Fig. 4 illustrates the curve of the drain current of a diode-connected PMOS transistor varying with V_{SG} for the width-to-length ratio (W/L) of 120 nm/40 nm. Its substrate is connected to the source terminal.

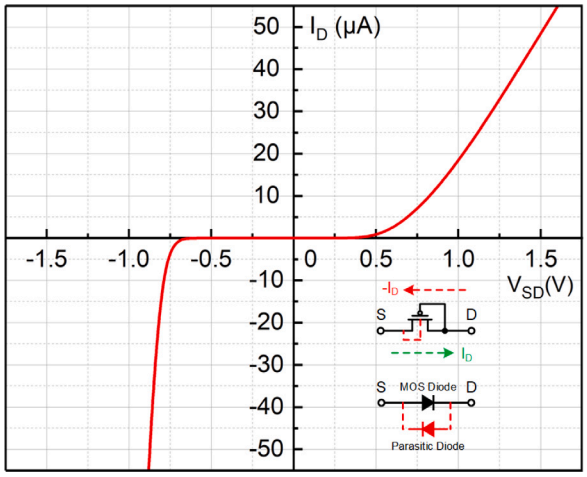

Fig. 4. I-V curve of diode-connected PMOS transistor when the substrate of the device is connected to the source terminal.

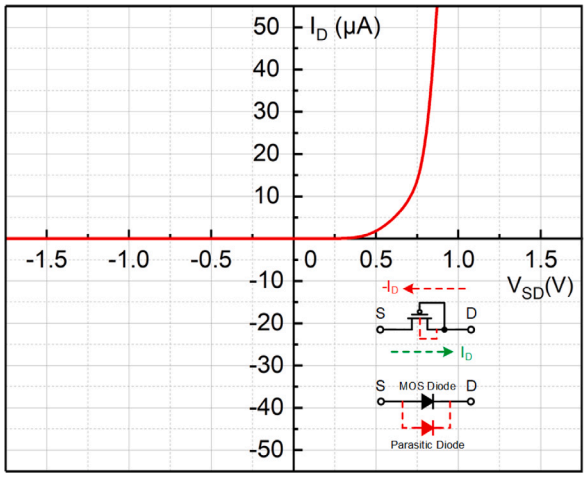

Fig. 5. I-V curve of diode-connected PMOS transistor when the substrate of the device is connected to the drain terminal.

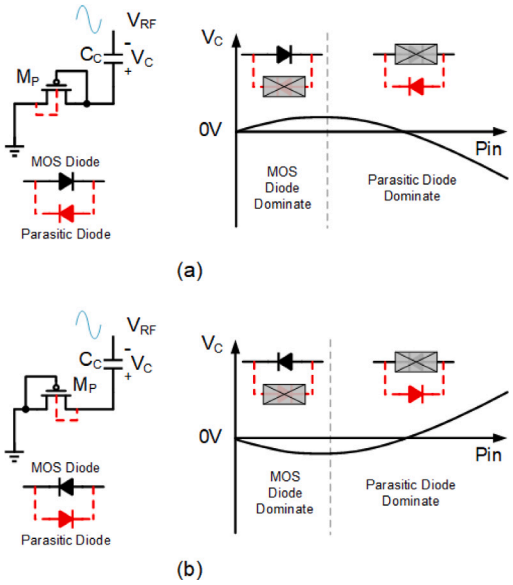

Fig. 6. The DC voltage of the charging capacitor C_C versus the input RF power when the substrate of the device is connected to the source and drain terminals respectively.

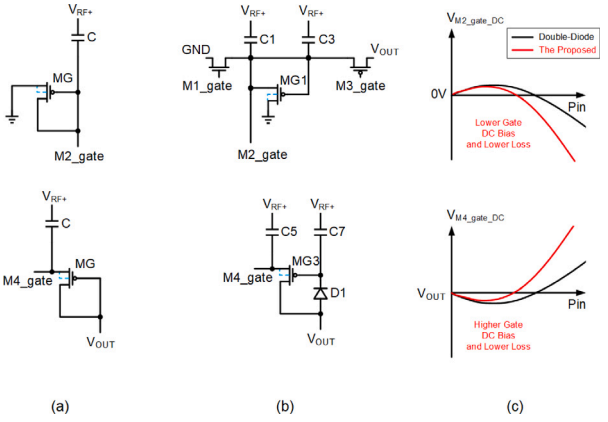

Fig. 7. The gate DC voltage of the rectifying transistors is compared for (a) the Double-Diode structure and (b) the proposed structure, as illustrated in (c).

When the signal amplitude below 0.3 V, the MOS diode working in the subthreshold region. Thus, a forward current is generated over a entire RF cycle. While the RF signal amplitude exceeds 0.3 V, the parasitic diode becomes dominant due to its significant increasing current. This current exhibits a rapid increase with the rising amplitude of the RF signal. Based on the operational characteristics of the parasitic diode and MOS diode, the diode-connected PMOS transistor exhibits a forward conduction current when the RF signal amplitude remains below 0.3 V. However, when the amplitude exceeds 0.3 V, the forward current gradually decreases and ultimately transitions into a reverse current. As the amplitude further increases, the reverse current also experiences an increase. Fig. 5 shows the I-V curve of a diode-connected PMOS transistor with the substrate connected to the drain terminal. The parasitic diode and the MOS diode have the same direction, which leads to a negligible reverse leakage current. Therefore, we can generate a DC bias that varies nonlinearly with changes in input power by attaching the diode-connected PMOS transistor's source to its bulk.

Fig. 6 depicts the nonlinear variation of the DC voltage (V_C) across the charging capacitor (C_C) versus the input power under a RF environment. The DC voltage shown in Fig. 6(a) is used for compensating the rectifying NMOS transistors. In low power operation, increasing the gate DC bias enhances the forward current of the NMOS. Alternatively, in high power operation, reducing the gate DC bias leads to a reduction in the leakage current flowing through the rectifying NMOS transistors. Conversely, the rectifying PMOS transistors require a gate DC bias as depicted in Fig. 6(b). In general, we achieve high efficiency under low power to high power conditions by applying appropriate gate DC bias to the rectifying transistors. This enhancement increases sensitivity while also broadening the DR. However, the gate DC bias of the rectifying NMOS transistors cannot decrease rapidly, while that of the rectifying PMOS transistors cannot increase as required when transitioning from low input power to high input power. This results in leakage loss that cannot be effectively suppressed. Therefore, we bias the gates of the diode-connected PMOS transistors to achieve a more appropriate DC bias for the gate of the rectifying transistors, effectively suppress the leakage loss and broaden the DR.

Fig. 7 exhibits the gate DC bias of the rectifying transistors vary with the input power for the different structures. The proposed structure reduces the current of the MOS diode by biasing the gates of the diode-connected PMOS transistors. This allows the rectifying transistors to achieve an appropriate DC bias. It is noteworthy that, under low input power, the diode-connected MOS transistors operate in the subthreshold region, as modeled in [6,7], expressed as:

$$I_{D,N(sub)} = I_{s0} e^{\frac{V_{GS}}{nV_T}} \left[1 - e^{\left(-\frac{V_{DS}}{V_T}\right)}\right](1 + \lambda_{sub} V_{DS}) \tag{1}$$

$$I_{D,P(sub)} = I_{s0} e^{\frac{V_{SG}}{nV_T}} \left[1 - e^{\left(-\frac{V_{SD}}{V_T}\right)}\right](1 + \lambda_{sub} V_{SD}) \tag{2}$$

where

$$I_{s0} = \mu_N C_{ox} V_T^2 \frac{W}{L} e^{\left(\frac{-V_{th} - V_{off}}{nV_T}\right)} \tag{3}$$

where the currents flowing through the drains of the NMOS and PMOS transistors are represented as $I_{D,N(\text{sub})}$ and $I_{D,P(\text{sub})}$ in the subthreshold region. The voltage between the gate and the source (or source and gate) of the transistor is represented as $V_{GS}(V_{SG})$ while voltage between the drain and the source (or source and drain) is indicated by $V_{DS}(V_{SD})$. The thermal voltage, is given by V_T = kT/q. The slope factor n, which is approximated as 1. The $(1+\lambda_{sub}V_{DS})$ is represented by channel length modulation effect where λ_{sub} is the channel length modulation factor. I_{s0} is process dependent parameter defined by (3), where μ stands for the carrier mobility, V_{th} stands for the transistor's threshold voltage, W/L represents the ratio of the width to the length, C_{ox} denotes the oxide capacitance per unit area, and V_{off} is the offset voltage in the subthreshold region. It can be observed from (1) and (2) that controlling the VGS and VDS of the diode-connected MOS transistors are two feasible circuit design strategies to increase the subthreshold current. However, modifying parameters such as μ, C_{ox}, and V_T typically requires process optimization or special processing during manufacturing. This could result in higher costs, as it involves alterations to transistor materials, structures or process steps.

Fig. 8 depicts the operating principle of the proposed design. It shows the capacity to convert RF inputs within a broad range into a DC voltage. Assuming a steady-state operation, M_2 and M_3 are active while M_1 and M_4 remain inactive during low power operation within the initial half-RF cycle as input voltage $V_{RF+} > V_{RF-}$. At this stage, the MOS diodes of MG2,3 dominate the charging of C2 while discharging C5 which enhances the forward conduction current of the rectifying transistors, as depicted in Fig. 8(a). When the voltage of V_{RF+} and V_{RF-} reverses, M_2 and M_3 turn off while M_1 and M_4 turn on. It can be observed in Fig. 8(b). The MOS diodes perform the charging of C1 and the discharging of C6 as illustrated in Fig. 8(a).

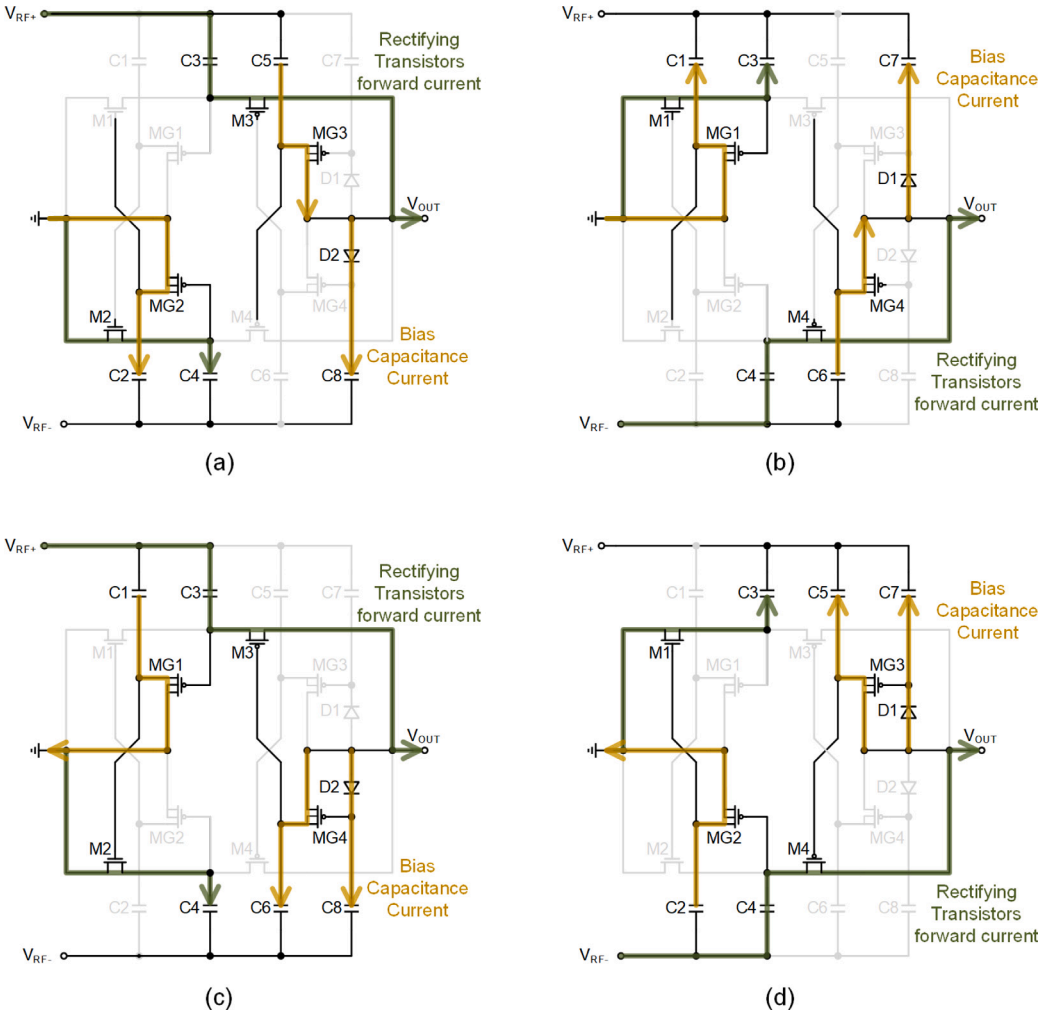

Fig. 8. Operation of the proposed rectifier. (a) positive-cycle, low-power. (b) negative-cycle, low-power. (c) positive-cycle, high-power. (d) negative-cycle, high-power.

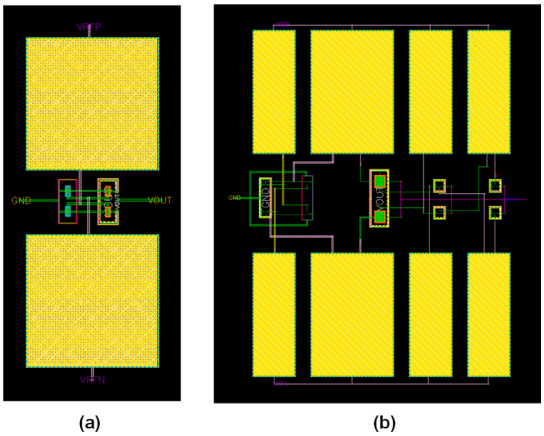

Fig. 9. Chip layout of (a) CCDD and (b) proposed rectifier.

Subsequently, M2,3 and M1,4 alternately conduct within the RF cycle as shown in Fig. 8(c) and (d) when the received power is high. The parasitic diodes dominate the discharging of C1,2 while charging C5,6 which provide appropriate gate DC bias for the rectifying transistors and thereby significantly reducing the reverse current. Notably, D1,2 charges C7,8 under both low and high input power conditions, providing an appropriate bias for the gates of MG3,4.

3. Simulation results and discussion

The proposed rectifier and the CCDD rectifier are simulated using a standard 40-nm TSMC CMOS process in Cadence environment for a fair comparison. It is noteworthy that low-threshold transistors are used as the rectifying transistors in both rectifiers. A 1pF MOM capacitor is selected as the load capacitor to reduce output ripple. Additionally, charging capacitors use MOM capacitors to minimize the influence of capacitance changes on rectifier operation. The layouts of the CCDD rectifier and the proposed rectifier are shown in Fig. 9. The proposed rectifier occupy a die area of 63 μm × 89 μm, and the CCDD rectifier occupy 20 μm × 50 μm. For precise assessment of the rectifier's performance, we assume ideal impedance matching. The received power can be calculated after eliminating the reflection effects [11–13], as follows:

$$P_{rec} = P_{in}(1 - |S_{11}|^2) \quad (4)$$

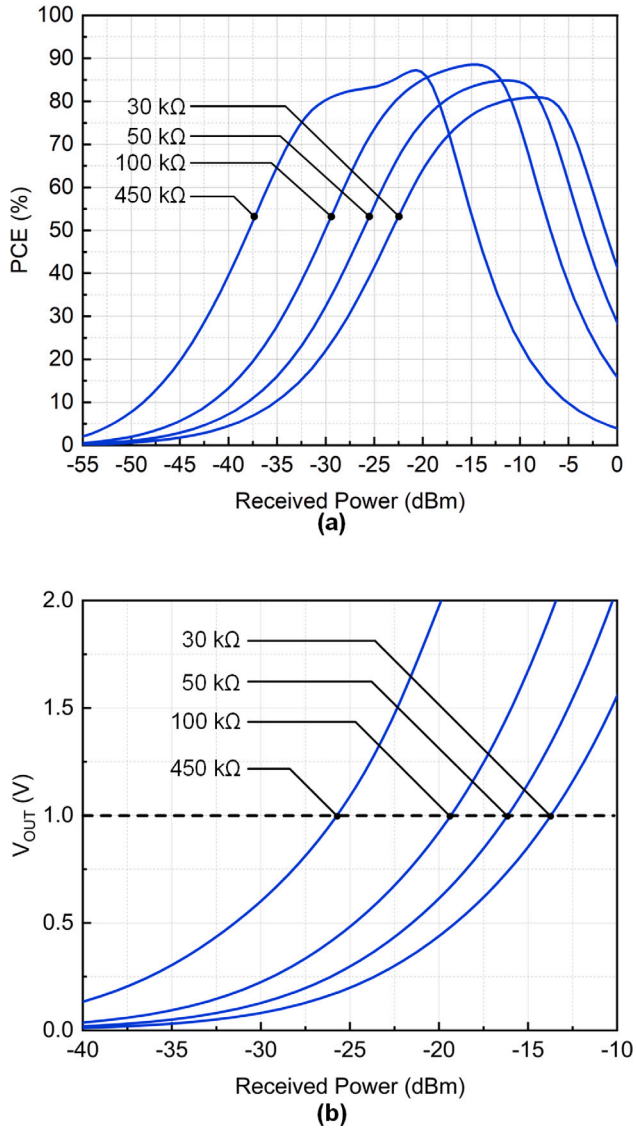

Fig. 10. Post-layout simulation of (a) the PCE and (b) the output voltage versus RF input power at 200 MHz with different loads.

where P_{rec} represents the received power of the rectifier, P_{in} denotes the input power from the source, and S_{11} is the reflection coefficient.

The input power source is set at 200 MHz, which is the general frequency band for the implantable WSN in the medical field. This frequency band has low losses when penetrating obstacles, enabling more efficient energy transmission in such environments. We simulate the PCE of the proposed rectifier, which varies with received power under four different loads. The results are shown in Fig. 10(a). Here, this load range (30–450 kΩ) is obtained by taking a ADE simulation in Cadence software. As can be observed, it achieves a 88.6% peak PCE with a 100 kΩ and a −14.8 dBm received power. These results show that the PCE increases until it reaches its peak value as the received power increases, and then decreases with the received power further increases. Furthermore, the proposed rectifier exhibits a wide DR. It can ensure that the PCE stays over 40% when the received power experiences a change starting at −32.1 dBm and ending at −5.4 dBm when the load resistance is 100 kΩ. The simulated output voltage under diverse loads as shown in Fig. 10(b). The proposed rectifier generates 1 V under a −19.3 dBm received power for a load of 100 kΩ. For the open load condition with a load impedance of 50 MΩ, the proposed rectifier attains a 32.9% peak PCE. In addition, a −35.8 dBm sensitivity

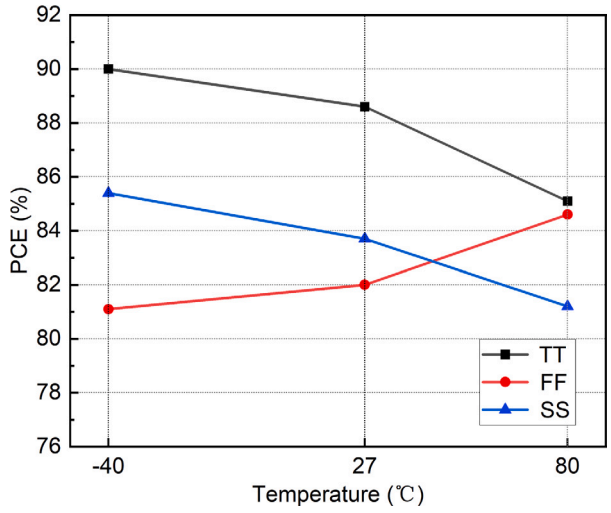

Fig. 11. The peak PCE of the proposed rectifier across different process corners and temperature ranges.

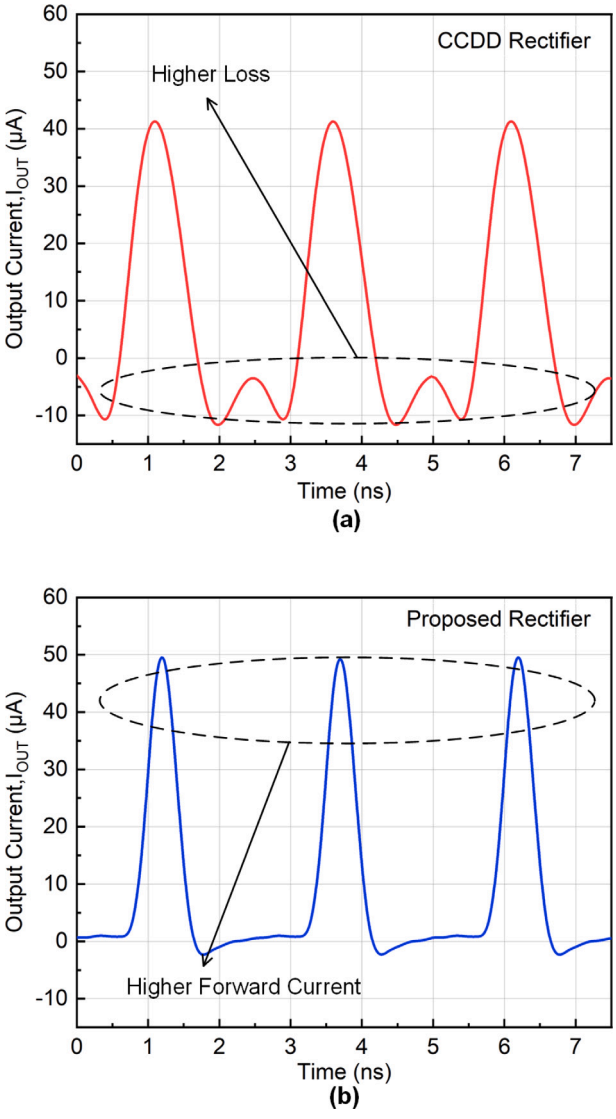

Fig. 12. The simulated transient output current for R_L = 100 kΩ and received power of −20 dBm with (a) the CCDD rectifier and (b) the proposed rectifier.

Table 1
Performance summary and comparison.

Architecture	Load (kΩ)	Frequency (MHz)	Technology (nm)	Number of stages	Area ($\times 10^3$ μm^2)	Additional requirements	Sensitivity[a] (dBm)	Peak PCE (%)	Dynamic range[b] (dB)	Simulation/ Measurement
Proposed design	**100**	**200**	**40**	**1**	**5.61**	–	**−19.3**	**88.6**	**26.7**	**Simulation**
CCDD using low threshold transistor	100	200	40	1	1	–	−13.8	70.7	13.6	Simulation
Gate voltage boosting [10]	10	200	180	1	N.A.	Deep N-well	−15	57.6	9	Measurement
Dual-Mode nested [11]	100	433	65	1	6.48	–	−19.2	86	26.1	Measurement
Dual-output [14]	12	0.012	65	1	3.72	Active NMOS+ DC–DC Combiner	N.A.	84	N.A.	Measurement
Dual-path [12]	100	900	65	3	23	–	−15.5	79.7	12.5	Measurement
Individual-capacitor coupling [13]	100	900	130	3	N.A.	Deep N-well	−18.7	80.3	14.5	Measurement
Reconfigurable [15]	1000	915	180	1-2-4-8	1080	–	−14.8	47.9	11	Measurement
Dynamic and static VT compensation [9]	450	915	130	10	29	–	−16	42.4	2.5	Measurement
Auxiliary self-biased [16]	200	915	130	6	63.58	–	−17.3	72.9	>9	Measurement
Hybrid stage [17]	100	920	180	3	11	Deep N-well	−15	45	5	Simulation
Dual gate and body self-biasing [18]	100	920	180	3	8.058	–	−18.4	78.15	>15	Simulation
Fully self-biased [19]	10	953	65	1	3.619	–	−3.5	60.5	14	Simulation
CCDD [20]	100	953	180	1	13.4	–	−12.9	86.2	15	Measurement
Self body biasing [21]	2	953	130	3	N.A.	–	−5.2	69.5	7.1	Measurement
Reverse DC feeding [22]	10	953	130	3	N.A.	Deep N-well	−6.3	72.2	13	Measurement
Self-biased gate [23]	1000	1070	65	10	73.2	Deep N-well	−13	30	0	Measurement
LC source degeneration [24]	0.5	2400	65	1	95	Deep N-well	−0.2	67.6	19	Measurement

[a] The received RF power needed to achieve an output voltage of 1 V;
[b] Received power range of PCE > 40%;

is achieved when the DC output is 1 V. Fig. 11 shows the variation in peak PCE of the proposed rectifier across different process corners and temperature ranges. The process corners include TT (Typical-Typical), FF (Fast-Fast), and SS (Slow-Slow), while the temperature ranges from −40 °C to 80 °C.

The waveforms of the transient currents delivered to the load under a 100 kΩ load, 200 MHz operating frequency, and −20 dBm received power in the CCDD and the proposed rectifier are shown in Fig. 12. The proposed rectifier exhibits a relatively larger forward current and a negligible reverse current, leading to a higher PCE, as shown in Fig. 13(a). During low power operation, the larger forward current causes the PCE of the proposed rectifier to experience a slight increase. With the received power further increasing, the leakage current is significantly suppressed and the PCE exceeds that of the CCDD rectifier. The capacity to actively bias the gates of rectifying transistors can be considered as an additional trait to broaden the DR. Specifically, the proposed rectifier achieves a 13.1 dB expansion for PCE above 40% and a 17.9% increase in peak PCE. Fig. 13(b) depicts the output DC voltage of the CCDD rectifier and that of the proposed rectifier. The output DC voltage of both rectifiers increases with an increase of the received power. Yet, the received power at peak PCE is different from that required to achieve a 1 V output DC voltage for the CCDD rectifier. This difference results in the CCDD rectifier cannot achieve its optimal sensitivity. Hence, stacking stages is often necessary to eliminate the difference. However, this approach also results in a decrease in PCE due to the increased losses associated with each additional stacking stage. On the contrary, the received power required to achieve the peak PCE of the proposed rectifier is nearly equivalent to that of needed to produce a 1 V output DC voltage, thus ensuring both high sensitivity and high PCE. In a single-stage configuration, the proposed rectifier achieves a sensitivity of −19.3 dBm. This sensitivity shows an improvement of 5.5 dB compared to that of the CCDD rectifier.

Table 1 compares the performance of the proposed rectifier with other recently published works. As summarized, the proposed rectifier provides a peak PCE of 88.6% when driving a load of 100 kΩ. Moreover, it reaches a 26.7 dB DR and a −19.3 dBm sensitivity when the output is 1 V, and it exceeds others reported in the technical literature in terms of their DR and sensitivity. Although CCDD [20] provides a comparable peak PCE, the proposed rectifier provides a higher sensitivity and a wider DR owing to the actively gate biasing technique employed in the design. The sensitivity and peak PCE of the individual-capacitor coupling [9] architecture show a comparable value, yet the proposed rectifier achieves wider DR at high received power.

4. Conclusion

In this article, a high-efficiency CMOS rectifier with high sensitivity and wide DR is presented. It employs a nonlinear gate bias compensation technique to the rectifying transistors, which enhances their conductivity during low power operation and reduces the reverse leakage current at high power, thereby improving both low-power and high-power performances. The proposed rectifier is post-simulated in the 40 nm CMOS technology which exhibits a peak PCE of 88.6%, a DR of 26.7 dB and a sensitivity of −19.3 dBm at 1 V when the received operates at a frequency of 200 MHz and the output is connected to a load of 100 kΩ. Considering its excellent performance, the proposed rectifier is a good candidate for RFEF system.

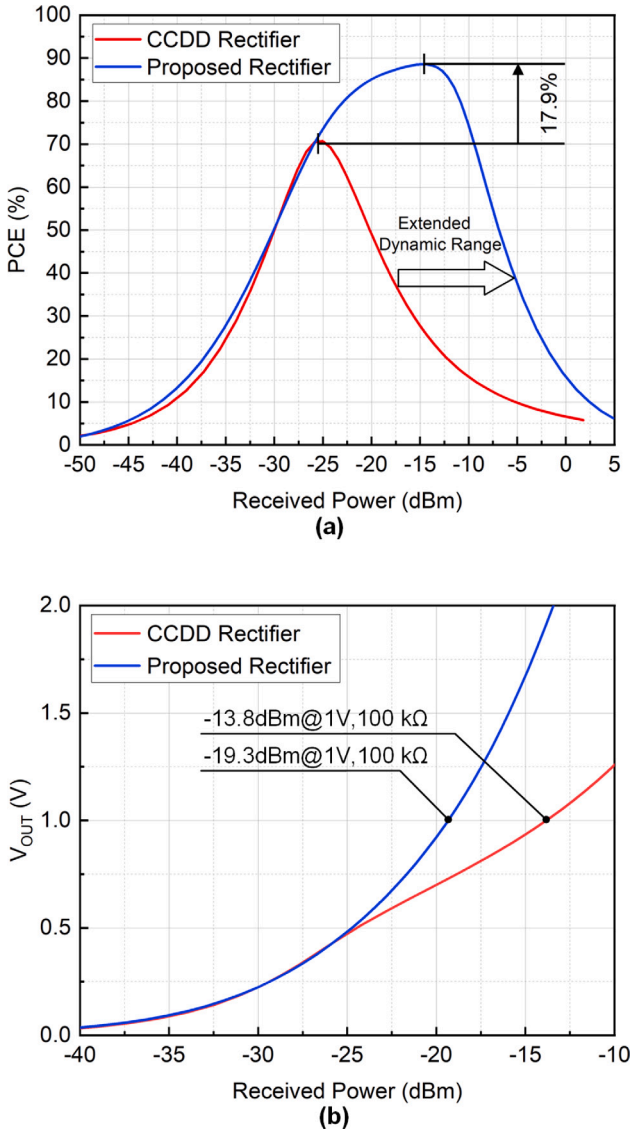

Fig. 13. Simulated performance of the CCDD rectifier and the proposed rectifier at 100 kΩ loads. (a) PCE vs. received power. (b) the output DC voltage vs. received power.

CRediT authorship contribution statement

Rui Wang: Writing – original draft. **Jian Liu:** Writing – review & editing, Funding acquisition. **Di Luo:** Formal analysis, Data curation. **Kang Zeng:** Validation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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