Design of impedance matching circuits for RF energy harvesting systems

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ABSTRACT

This paper presents a systematic design methodology for impedance matching circuits of an RF energy harvester to maximize the harvested energy for a range of input power levels with known distribution. Design of input matching networks for RF rectifier differs from those for traditional RF circuits such as low-noise amplifier because the transistors in the RF rectifiers operate in different regions. In this work, it is shown that the input impedance of the rectifier estimated based on small signal simulation of transistors at the peak of input signal in the rectifier when the transistors are biased with stable DC operating voltage provides the largest harvested energy from a fixed input power. For variable input power levels, a matching network selection strategy is proposed to maximize expected harvested energy given the probability density distribution of input power levels. As an experimental sample, an RF energy harvester circuit is designed to maximize the harvested energy in the 902–928 MHz band employing an off-chip impedance matching circuit designed using the proposed methodology. The proposed RF energy harvester exhibits a measured maximum power conversion efficiency (PCE) of 32% at −15 dBm (32 μW) and delivers an output DC voltage of 3.2 V to a 1 MΩ load.

1. Introduction

There is a growing interest to harvest ambient energy for the operation of portable electronic devices or low power wireless sensors. RF energy harvesting can be used to partially/fully supply the energy required for the operation of portable electronic devices such as wireless sensors, cell phones, bluetooth devices, medical implants and hearing aid devices [1,2]. In an RF energy harvesting system, an antenna receives the incident RF signal, an impedance matching circuit maximizes the power transfer from the receiving antenna to the rectifier and a multi-stage rectifier converts the incoming RF signals to an output DC voltage.

Impedance matching circuit is crucial in optimizing the performance of the RF energy harvesting system [3,4]. Small signal modeling technique to approximate the behavior of nonlinear devices with linear equation used in designing an impedance matching circuit for traditional RF circuits such as a low noise amplifier (LNA) cannot be used in an RF energy harvester due to the large input signal and absence of an input DC bias. The large input signal without any DC bias results in the rectifying device to operate in different regions of operation within the same input cycle. This leads to variation in the input impedance of the rectifier with the received power and the output load and degradation of the overall power conversion efficiency (PCE) of the energy harvester due to the impedance mismatch between the antenna and the rectifier [5]. Fixed LC impedance matching circuits are used to match the input impedance of the rectifier to the output impedance of the antenna. A fixed impedance matching circuit is implemented onto a printed circuit board (PCB) in [3,6,7] to fine tune the impedance match between the

antenna and the rectifier. The impedance matching circuit implemented in [8] is optimized to achieve maximum sensitivity and maximum voltage gain from the antenna to the rectifier's input. A transformer is used for impedance matching in [9] which has an advantage of lower die area and robustness compared to the LC matching method. An impedance matching circuit is designed at the minimum input power available at the antenna in [10] and at a specified input power level in [11–13]. A fixed impedance matching circuit is implemented on-chip in [4] and a CAD-oriented design procedure is proposed to maximize the overall PCE with the impedance matching circuit. However, the reported fixed impedance matching circuits are designed for a specific input voltage and power level and do not consider the variation in the rectifier's impedance and the resulting impedance mismatch. To ensure impedance match between the antenna and the rectifier there has been innovative solutions in designing the impedance matching circuit using tunable matching techniques. Authors in [14,15] suggested tuning the inductor and the capacitor using MOS varactor or thin-film varactor in order to ensure maximum PCE for all input operations. The impedance variation in the antenna-rectifier interface is compensated by a control loop in [16] which provides voltage to a capacitor bank. The control loop is implemented off-chip using microcontroller and requires a supply voltage for operation. Although these techniques reduce the impedance mismatch, the power consumption associated with the additional circuitry may outweigh their benefit at low power regimes.

In this paper, a systematic methodology for design of impedance matching circuits for RF energy harvesting systems is proposed. In Section 2, the rectifier's input impedance is calculated for different input power levels based on the small signal model of the rectifying
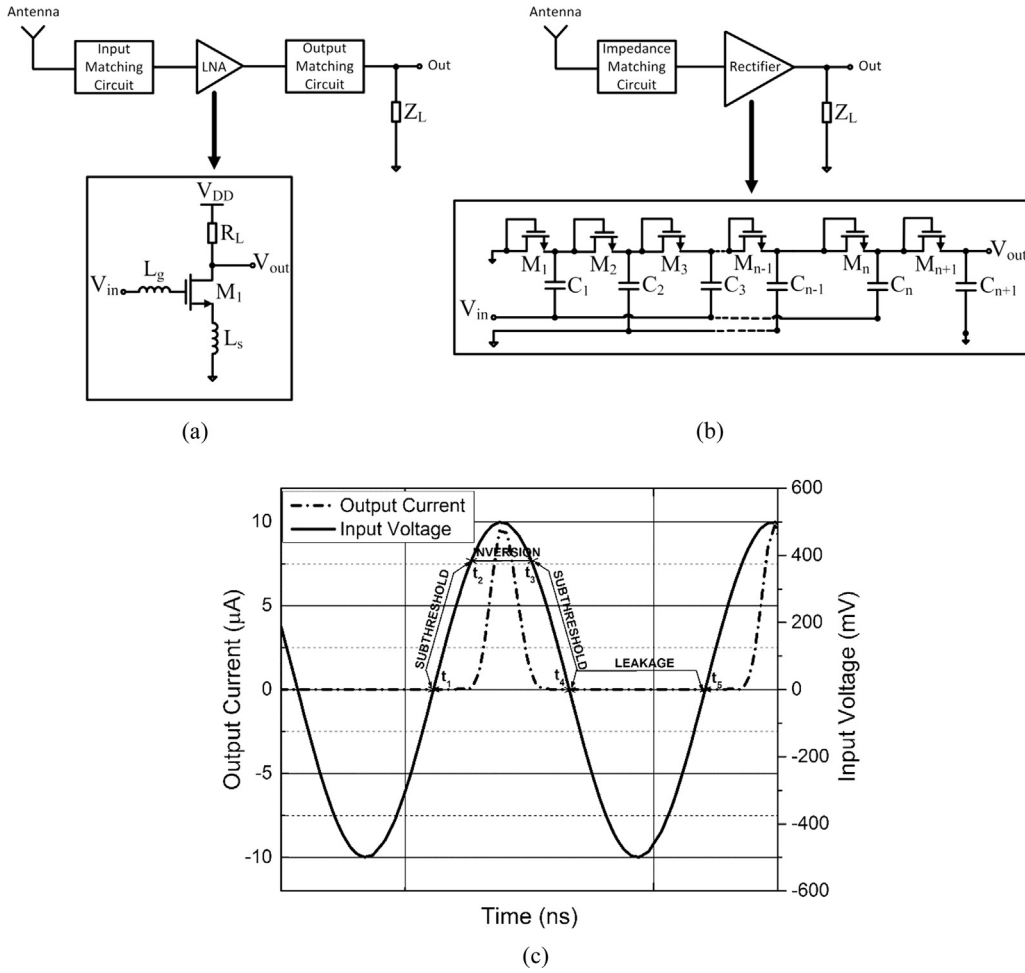
Fig. 1. (a) Block Diagram of LNA with impedance matching circuit, (b) RF energy harvester with impedance matching circuit. (c) Transient analysis of output current and input voltage of rectifier.

device when the transistors are biased with DC voltages under stable condition. Section 3 describes the design of the impedance matching circuits for a fixed input power. In Section 4, a strategy is proposed to select a fixed impedance matching circuit for variable input power with a known distribution. Section 5 describes the design and implementation of a sample off-chip impedance matching circuit based on the proposed methodology and reports the measurement results of the overall performance of the RF energy harvester.

2. Input impedance of RF rectifier

An impedance matching circuit is required to maximize power transfer between the source and the load. The impedances of the source and the load are matched at the desired operating frequency such that the impedances are complex conjugates of each other. The first step in the design of matching networks is to find the input impedance of the load (RF rectifier) to be matched to the output impedance of the source (antenna), typically 50 Ω. For traditional RF circuits such as low-noise amplifiers (LNAs) as shown in Fig. 1(a), the input impedance can be found by linearizing the transistor equations around the biasing point (small-signal modeling). The small variation in input signal guarantees that small-signal parameters of the transistors remain relatively constant, and the calculated input impedance accurately predict the behavior of the circuit during the normal operation. A fixed impedance matching circuit can then be designed to match the output impedance of the antenna to the input impedance of the LNA. However, the input impedance of an RF rectifier as shown in Fig. 1(b) cannot be modeled by linearizing the transistor equations around a single biasing point.

The modeling of the input impedance of an RF rectifier differs from an LNA because.

1. For a fixed input power, the small-signal input impedance of an RF rectifier varies within the same cycle depending on the biasing point where the linearized input impedance is obtained.
2. The input impedance of an RF rectifier changes dramatically for different input powers as the input signal amplitude changes.

Let's examine the behavior of an RF rectifier for a fixed input power producing a sinusoidal voltage signal with constant amplitude at the input of the rectifier. Within one cycle of input signal, the rectifying device operates in different regions namely subthreshold region, inversion region and the leakage region as seen in Fig. 1(c) that depicts the simulated result of output current versus input voltage for a PMOS voltage doubler. The subthreshold operation extends from $V_{in}=0$ to $V_{in}=|V_{TP}|$, where V_{in} is the input voltage. The current in this region is an exponential function of the input voltage. The inversion region extends from $V_{in}=|V_{TP}|$ to $V_{in}=V_{amp}$. The current in this region is a square function of the input voltage and increases rapidly with the input voltage. In the inversion region, the output current reaches its peak value when $V_{in}=V_{amp}$. Finally, the leakage region extends from $V_{in}=0$ to the next $V_{in}=0$ in the negative half-cycle. The small-signal input impedance of the rectifier varies according to the region of operation of the transistor and within each region of the operation.

The rectifier input impedance can be represented as $R_{rec}-jX_{rec}$ where R_{rec} is the real part of the rectifier's input impedance and X_{rec} is its imaginary part. The real part of the impedance is determined by the

real power consumption of the circuit resulting from the resistive losses and the load current. The imaginary part of the impedance is determined by the effective input capacitance of the circuit that depends on the number of stages, device and external bonding capacitance. The input impedance of the rectifier changes with the input power level and varies within the same input voltage cycle for a constant power level. An input impedance of the rectifier has to be selected from the different impedances obtained at different voltage levels within the same input cycle for the design of impedance matching circuit.

The input impedance for a constant power level at different input bias level within the same cycle is simulated as follows. The input impedance of the rectifier is estimated using CAD simulator based on small signal simulation of transistors at the different DC input signal level when the transistors are biased with stable DC operating voltage. Transient simulation is performed on the rectifier and DC node voltages under stable condition are obtained. The MOS transistors are biased according to their steady state condition and a small signal is then applied at different input DC bias level. As the rectifier can be modeled as a resistive and capacitive component in parallel, Y parameters are obtained for easy calculation of input resistance and input capacitance. Once the Y parameter for different input voltage levels (input DC bias levels) are known, $Y_{in,\ real} = 1/R_{in}$ and $Y_{imag} = \omega_0 C$ is used to calculate the resistance and the capacitance value. A 12-stage threshold-compensated multistage rectifier using Dickson multiplier topology [17,18] in 0.13 μm CMOS technology is used for simulating the input impedance. The input resistance and input capacitance of the rectifier as a function of the DC input bias for the different input power to the rectifier is shown in Fig. 2(a) and (b), respectively. As predicted, the input impedance of the rectifier varies within the same input cycle for a constant power level. For an input power level to the rectifier (P_{in}) of −15 dBm producing a voltage amplitude (V_{rect}) of 280 mV at the input of the rectifier, the small-signal input resistance and capacitance are 206 Ω and 0.46 pF, respectively if the input terminal is biased with a DC voltage of 280 mV. If the DC bias of 280 mV is changed to 260 mV, an input resistance of 273 Ω and a capacitance of 0.44 pF are obtained which shows the strong dependency of small-signal parameters on the input DC bias voltage. Similar trend have been observed for the variation of input resistance and capacitance.

3. Design of impedance matching circuit for fixed input power

An ideal impedance matching circuit for RF energy harvesting must not only provide the desired impedance matching between the source and load but also must do so with minimum insertion loss so that the amount of harvested can be maximized from the limited source energy.
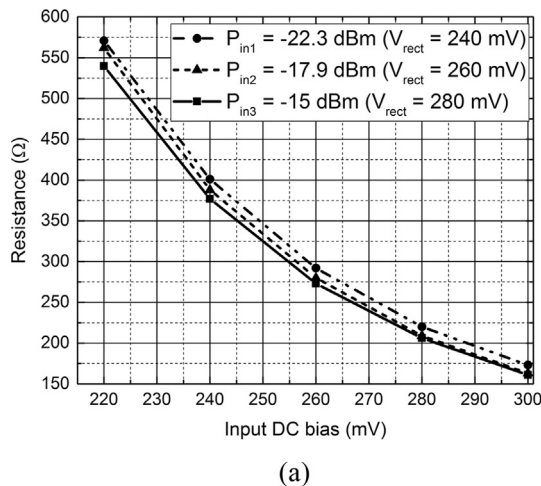
Comparative study of different matching circuit topologies suggests simple 2-component L-section for matching networks operating in low power regimes as the topology of choice as L-section matching circuit is able to provide desired input matching with minimal losses compared to other topologies using more passive components [3,4]. The L-section matching circuit also provides passive voltage amplification of the input voltage. The adopted L-section matching circuit to match the impedances between the source and the load (RF rectifier) is shown in Fig. 3. An internal resistance $R_s = 50\ \Omega$ is assumed for the power source. The reference power notations are represented as follows. Source power is represented by P_s, available power from the antenna by P_{av}, input power to the rectifier by P_{in} and the output power delivered to the load by P_L.

The matching section components L_m and C_m are calculated by cancelling the imaginary component of the impedance and equating the real part at the desired frequency. Equating the real part of the antenna and the rectifier's impedance we get

$$R_s = R_{in} \cdot \left(\frac{1}{1 + Q^2} \right) \tag{1}$$

The quality factor Q is

$$Q = \sqrt{\frac{R_{in}}{R_s} - 1} \tag{2}$$

The quality factor can also be expressed as the ratio of the imaginary part of the impedance to its resistance.

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)} = \frac{\mathrm{Im}(1/Y)}{\mathrm{Re}(1/Y)} = \frac{\mathrm{Im}\left(\dfrac{1}{\dfrac{1}{R_{in}} + j\omega_0 C_{in} + \dfrac{1}{j\omega_0 L_m}} \right)}{\mathrm{Re}\left(\dfrac{1}{\dfrac{1}{R_{in}} + j\omega_0 C_{in} + \dfrac{1}{j\omega_0 L_m}} \right)}$$

$$= \frac{R_{in}}{\omega_0 L_m} - \omega_0 C_{in} R_{in} \tag{3}$$

L_m is calculated using (4) as

$$L_m = \frac{R_{in}}{\omega_0 (Q + \omega_0 R_{in} C_{in})} \tag{4}$$

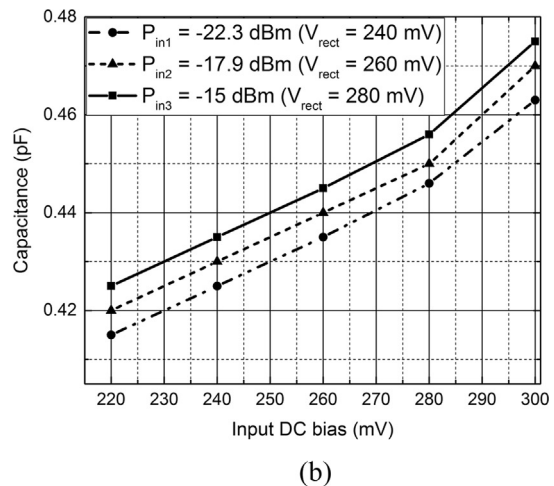The L-section capacitor C_m is calculated by equating the imaginary part to zero, we get

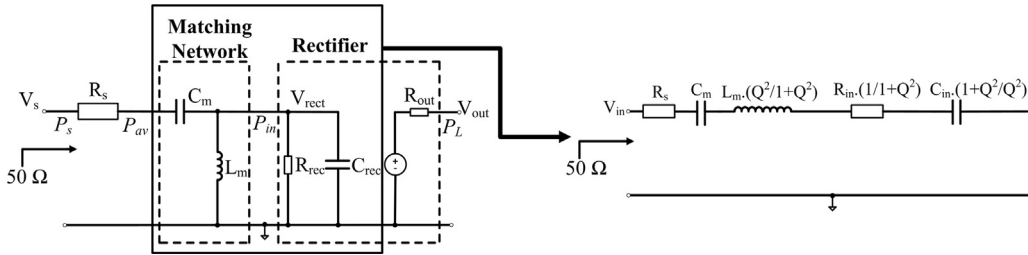**Fig. 2.** (a) Resistance and (b) capacitance of the rectifier as a function of input DC bias.

Fig. 3. Modeling of the impedance matching circuit and the rectifier.

$$\frac{1}{j\omega_0 C_m} + j\omega_0 L_m\left(\frac{Q^2}{1+Q^2}\right) + \frac{1}{j\omega_0 C_{in}\left(\frac{1+Q^2}{Q^2}\right)} = 0 \tag{5}$$

Solving (5) for C_m, we get

$$C_m = \frac{R_{in}}{L_m(R_{in} - R_s)} \cdot \frac{1}{\left(\omega_0^2 - \frac{1}{L_m C_{in}}\right)} \tag{6}$$

The L-section impedance matching circuits with the passive components L_m and C_m are designed for different input conditions.

The input resistance and input capacitance of the rectifier circuit varies for the different input DC bias levels as shown in Fig. 2(a) and (b). Now the question is at what input signal level the small-signal input impedance must be calculated in order to maximize the power transfer from antenna to the rectifier and produce maximum harvested energy. As the input current and the input power of the rectifier are significantly larger during the inversion region than in other regions of the operation, the point that should be selected for estimation of the input impedance of the rectifier must lie within the inversion region. In order to find the desired point in the inversion region for design of matching circuits, extensive simulations have been performed as described below.

L-section impedance matching circuit is designed at different input voltage bias levels for a fixed source power level within the inversion region to convert the calculated input impedances to 50 Ω which is the internal resistance of the power source. At a constant source power P_s with the designed impedance circuits for the different input DC bias levels, the harvested power is simulated so that an impedance matching circuit providing the highest harvested power can be selected. The harvested power graph versus input DC bias for different values of source power is shown in Fig. 4. $P_{s1} = -11.9$ dBm, $P_{s2} = -11$ dBm and $P_{s3} = -7.5$ dBm corresponds to source power giving V_{rect} of 240 mV, 260 mV and 280 mV for an impedance matching circuit realized at the peak of the input voltage signal. When the impedance matching circuit is designed at the peak of the input signal with $P_{s1} = -11$ dBm

Fig. 4. Harvested power as a function of input DC bias at different source power levels.

($V_{rect} = 260$ mV) the harvested power is 3.16 μW. The harvested power degrades to 1.22 μW when the impedance matching circuit is designed at an input DC bias of 240 mV. Similarly for $P_{s2} = -7.5$ dBm resulting in $V_{rect} = 280$ mV, when the impedance matching circuit is designed for the peak of the input signal the harvested power is 10.5 μW which degrades to 9.2 μW and 7.5 μW for input DC bias of 260 mV and 240 mV, respectively. Based on the simulation results in Fig. 4, it can be concluded that to maximize the power transfer and the amount of harvested power, the matching network must be designed to convert the small-signal input impedance calculated when input port is biased at the peak of input signal.

Fig. 5(a) and (b) shows the rectifier's resistance and capacitance as a function of input power to the rectifier calculated at the peak of the input signal. At extremely low input power of approximately −33 dBm (500 nW), the input resistance R_{in} is 13.9 kΩ. The input resistance decreases rapidly with increase in the input power. For −30 dBm (1 μW) of input power the input resistance is 5.8 kΩ and decreases to 620 Ω for an input power of −22.6 dBm (5.5 μW) and to 96 Ω at an input power of −9.6 dBm (110 μW). The input capacitance graph as a function of received power is shown in Fig. 5(b). For an input power range of −30 dBm to −10 dBm, the variation in the capacitance is from 0.4 to 0.56 pF.

4. Selection of impedance matching circuit for variable input power

As the distance between RF energy emitter and harvester varies depending on their relative locations and existence of obstacles, the amount of available input power dramatically changes for a practical RF energy harvester. The different input power results in variation of rectifier's input voltage amplitude, and consequently results in different input impedances of RF rectifiers at the peak of the received voltage signal. The variation in the input impedance of the rectifier with the input power to the rectifier results in reflection at the antenna – matching circuit – rectifier interfaces for a fixed impedance matching circuit. The PCE of the RF rectifier with the impedance matching circuit is defined in (7) as the ratio of the DC output power to the available RF power from the antenna.

$$PCE_{matching-rectifier} = \frac{P_L}{P_{av}} \tag{7}$$

Including the effect of output resistance of the antenna (R_s) which is assumed to be 50 Ω, the PCE of the overall system can also be expressed as

$$PCE_{system} = \frac{P_L}{P_s} \tag{8}$$

PCE_{system} is smaller than $PCE_{matching-rectifier}$ due to the additional loss at the resistor R_s. The effect of the impedance mismatch on the output power for different values of source power P_s is shown in Fig. 7(a). The impedance matching circuits for different input power condition are realized by giving $V_{rec} = 200$ mV, 240 mV, 280 mV and 300 mV where V_{rec} is the voltage amplitude at the input of the rectifier. The realized L-
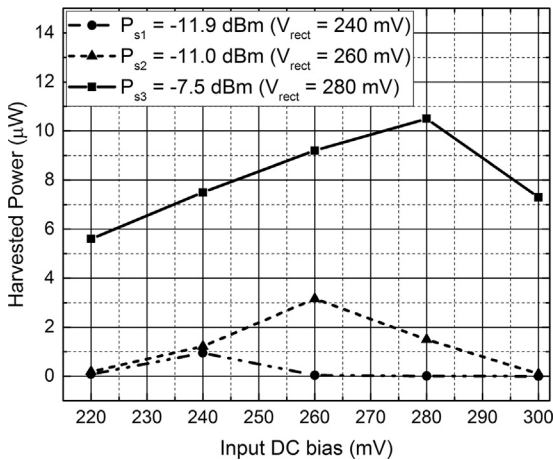
(a)

(b)
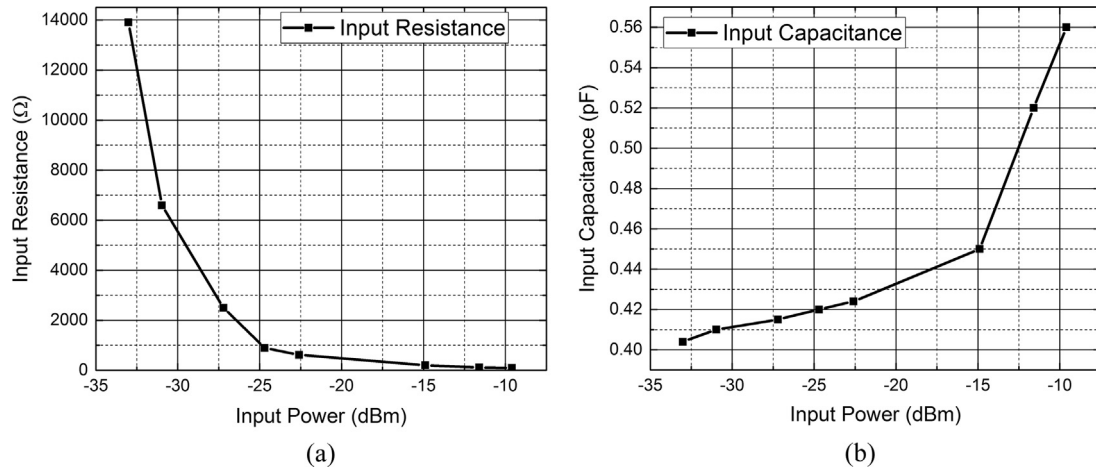
Fig. 5. (a) Input resistance and (b) input capacitance of the rectifier as a function of input power to the rectifier.

200 mV matching circuit

240 mV matching circuit

280 mV matching circuit
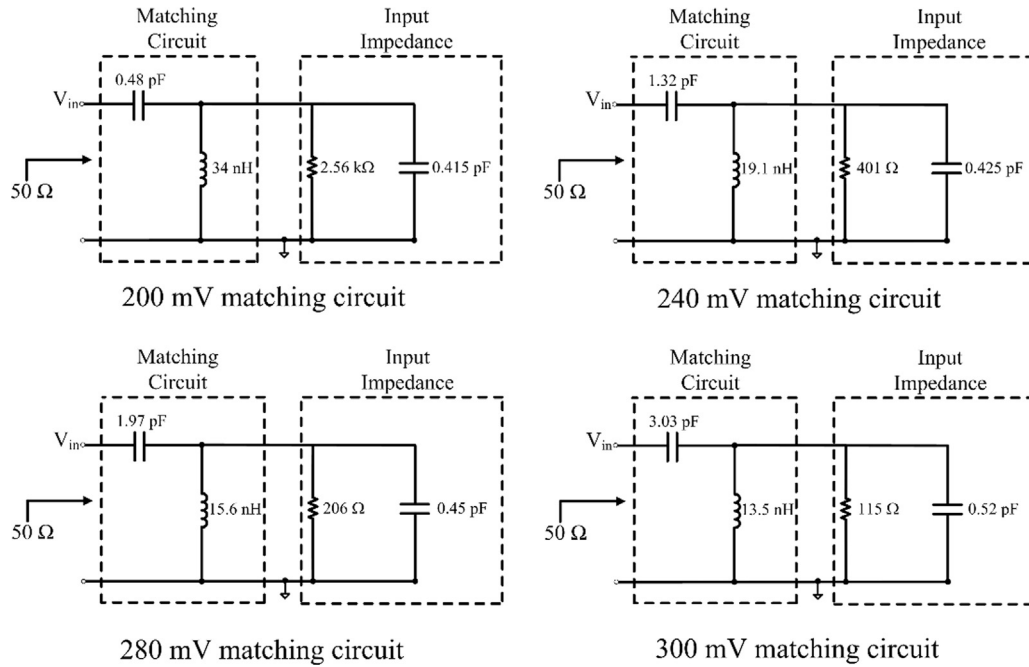
300 mV matching circuit

Fig. 6. Designed impedance matching circuits for different input conditions.
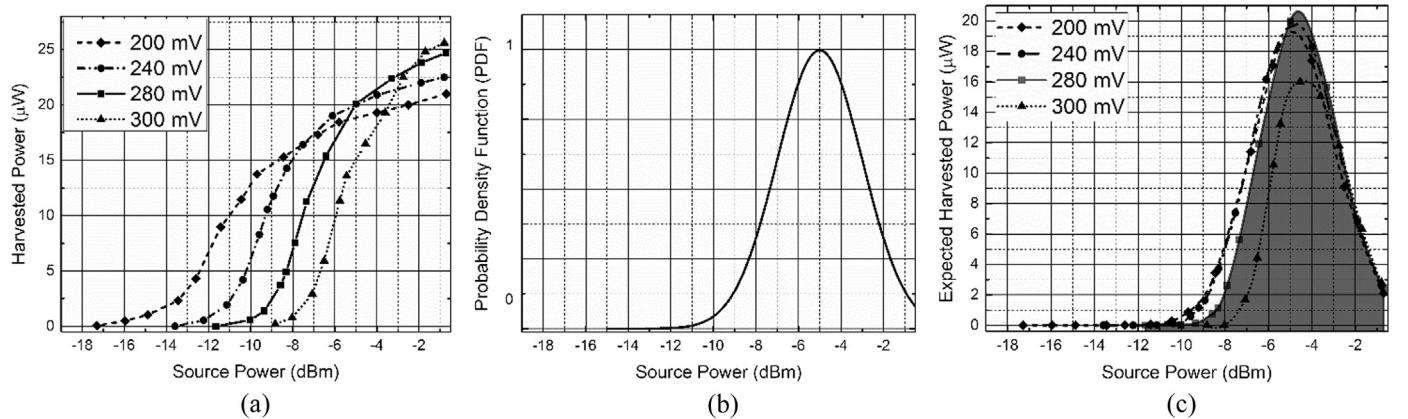

(a)

(b)

(c)

Fig. 7. (a) Output power versus source power for different input matching circuits. (b) Probability density function. (c) Expected harvested output power for different impedance matching circuits.
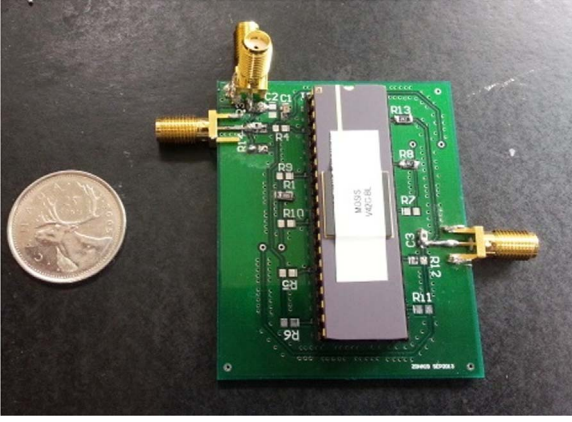
Fig. 8. PCB to measure performance of the RF energy harvester with off-chip impedance matching circuit.

section impedance matching circuits for the different input voltage condition are illustrated in Fig. 6. The DC node voltages under stable condition are obtained for the different input conditions. The rectifier is biased according to their steady state condition and a small signal is applied to compute the input impedance of the rectifier and the matching circuits for different input voltage amplitudes and power. The matching circuit realized by giving $V_{rec} = N$ mV is referred as N mV matching circuit. As seen in Fig. 7(a), when P_s is below -10 dBm the output power is the highest for the 200 mV matching circuit. The input impedance mismatch is the lowest for the 200 mV matching circuit for source power less than -10 dBm. As the source power increases the mismatch becomes larger compared to other matching circuits. Each of the impedance matching circuit provides the largest output power when the impedance mismatch is the least. For a source power greater than -4 dBm, the 300 mV matching circuit provides the highest output power while the 200 mV matching circuit has the most impedance mismatch.

Now the question is at what input power level we must design the impedance matching circuit that produces the largest harvested power if the input power varies with a known distribution. An N mV impedance matching circuit gives the highest harvested power for only a narrow range of source power levels. The goal is to design a fixed impedance matching circuit that maximizes the amount of harvested power for a defined range of source power levels without significantly degrading the harvested power for other input power levels. Fig. 7(a) shows the harvested power versus source power with different impedance.

matching circuits. The probability of a power level to be present at the source is expressed by a probability distribution function (PDF) as shown in Fig. 7(b). The expected harvested power is given by

$$E[X] = \int_{-\infty}^{\infty} x. f(x)dx = \int_{-\infty}^{\infty} P_s. PCE_{system}. PDF[P_s]dx \quad (9)$$

where $E[X]$ is the expected harvested power with a matching circuit represented by a random variable X. The integration of the product of the source power, PCE_{system} and the PDF over the entire source power range gives the expected harvested power. Fig. 7(c) shows the product of the harvested power and the PDF for the different impedance matching circuits for a range of source power levels. The shaded area under the curve represents the expected harvested power for the corresponding matching network. The expected harvested powers are calculated for different random variables X_n where $X_1, X_2 .... X_n$ are the different impedance matching circuits. The input matching circuit which gives the largest shaded area for the expected harvested power curve is then selected as the impedance matching circuit of choice that maximizes the expected harvested power given the PDF of input power. The selected matching circuit gives the best overall PCE_{system} over the defined range of power levels.
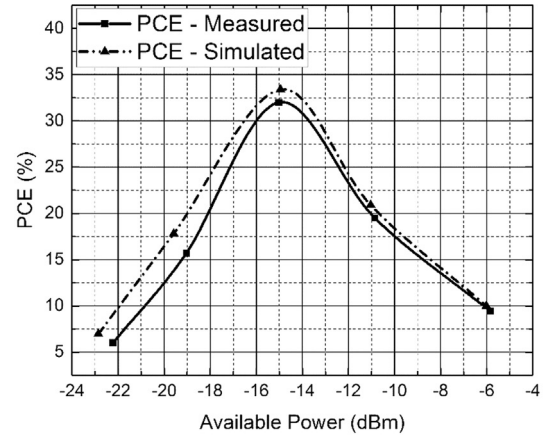
(a)
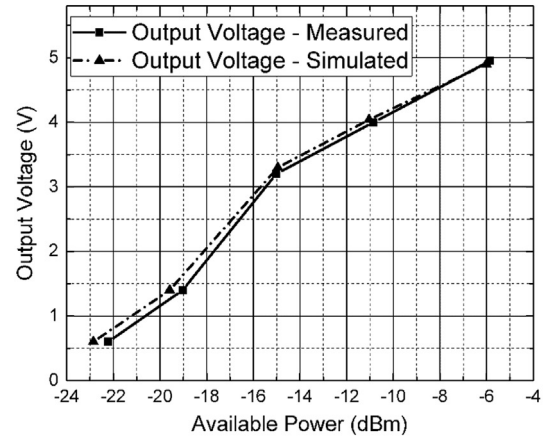
(b)
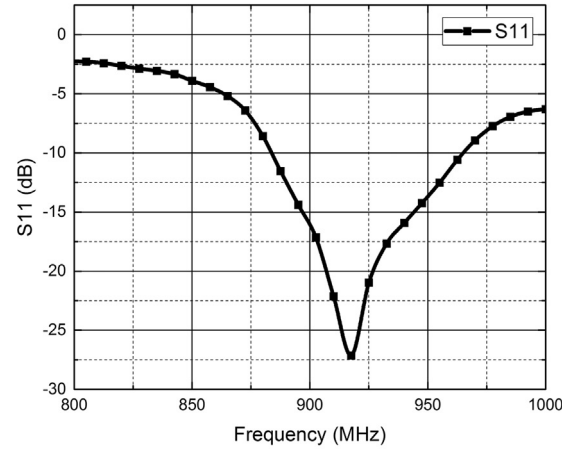
(c)

Fig. 9. (a) Measured and simulated PCE as a function of available power for a 1 MΩ load. (b) Measured and simulated output voltage as a function of available power for a 1 MΩ load. (c) Measured return loss for the RF harvesting system.

5. Experimental results

The performance of an off-chip impedance matching circuit for an RF energy harvester operating with a known input probability density function is examined in this section. A uniform density function is used in this design example assuming an equal probability for the source power to be between $a = -6$ dBm (250 μW) to $b = -3$ dBm (500 μW) and a zero probability for the other power levels. The probability density function is defined as

Table 1
Performance summary and comparisons.

	This Work	Abouzied – 2015 [17]	Hugo – 2015 [18]	Stoopman – 2014 [19]	Papotto – 2011 [4]
Technology	130 nm	180 nm	180 nm	90 nm	90 nm
Frequency	902–928 MHz	798 MHz	1.3 GHz	868 MHz	915 MHz
Impedance matching technique	Variable input voltage/power level matching	Fixed voltage/power level matching	Transformer-based matching	Adaptive control circuit	Fixed voltage/power level matching
Maximum PCE	32% @ − 15 dBm	n.a.	Less than 1%	24% @ − 21 dBm	11% @ − 18.8 dBm
Input power range PCE greater than 20%	15–78 μW	n.a.	PCE less than 1%	5–25 μW	PCE less than 11%
Load	$R_L = 1$ MΩ	Open Load	$R_L = 10$ MΩ	$R_L = 1$ MΩ	$R_L = 1$ MΩ

$$f(x) = \begin{cases} \frac{1}{b-a} & \text{for } a \leq x \leq b \\ 0 & \text{for } x < a \text{ or } x > b \end{cases} \qquad (10)$$

For a random variable $X_1, X_2 \ldots . X_n$ where X_1 is the 200 mV matching circuit, X_2 is the 240 mV matching circuit, X_3 is the 280 mV matching circuit and X_n is the nth matching circuit, the expected value is expressed as

$$E[X] = \int_{-\infty}^{\infty} x . f(x) dx = \int_{a}^{b} P_s . PCE_{system} . \frac{1}{b-a} dx \qquad (11)$$

A matching circuit is selected such that to maximize the expected harvested energy power. In this design example, $E[X_3]$ gives the maximum expected value. The 280 mV matching network gives the best PCE_{system} and the highest harvested power compared to the other impedance matching circuits in the source power range of − 6 dBm to − 3 dBm, as seen in the simulated harvested power graph of Fig. 7(c). To test the overall performance of the RF energy harvester, a rectifier chip is designed and fabricated in 0.13 μm CMOS process and wire-bonded onto a 2-layer FR-4 PCB board as shown in Fig. 8. An off-chip impedance matching circuit using AVX thin-film capacitor $C_m = 1.7$ pF and thin-film inductor $L_m = 15$ nH (280 mV matching circuit) is designed for a rectifier's input impedance of 206 Ω//0.45 pF. The chip is tested with Agilent MXG-N5181 signal generator using modulated continuous signal in the ISM band of 902–928 MHz similar to the test setup in [19]. $PCE_{matching-rectifier}$ is measured which represents the ratio of P_L and P_{av}. The output DC voltage is obtained with an oscilloscope or a digital multimeter.

The measured and simulated PCE curve and the output DC voltage as a function of available power at the antenna are shown in Fig. 9(a) and (b), respectively. The measured results are found to be in close agreement with the simulation results. The output DC voltage increases with the available input power as seen from Fig. 9(b). An output DC voltage of 1 V is obtained at an input power of only 8.9 μW (− 20.5 dBm) for a 1 MΩ load. Fig. 9(c) shows the plot of the measured return loss for the rectifier with the impedance matching circuit.

Table 1 summarizes the performance of this work and compares it with the published state-of-the-art works. A maximum PCE of 32% is measured at an input power of 32 μW (− 15 dBm) with an output DC voltage of 3.2 V for a 1 MΩ load. The PCE is greater than 20% for the available power range of 15 μW–78 μW (63 μW) for a 1 MΩ load. The proposed impedance matching technique with the rectifier achieves large PCE over a wide range of input power levels as seen from Table 1. Without the proposed impedance matching method, the PCE will degrade significantly over a range of input power levels. In comparison with recent works, only work in [14] achieves an efficiency greater than 20% for a range of 5–25 μW.

6. Conclusions

This paper present a systematic methodology for design of impedance matching circuits of RF energy harvesters to maximize the harvested energy for a defined range of input power levels with a known distribution. The RF rectifier has been modeled to include the effect of the variation in the input impedance of the rectifier due to the large input signal variations. It has been shown that the matching circuits that convert the input impedance of the rectifier at peak voltage level for a fixed input power produces the largest harvested power. A procedure for selecting the impedance matching circuit for a defined range of input power levels with known distribution is proposed in this paper. The selected impedance matching circuit provides the largest harvested power and maximizes the PCE for a defined range of input power. A rectifier chip and an off-chip impedance matching circuit are implemented onto a PCB and the overall performance is measured. A maximum PCE of 32% is measured at an input power of 32 μW (− 15 dBm) with an output DC voltage of 3.2 V for a 1 MΩ load.

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