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Process and temperature robust voltage multiplier design for RF energy harvesting

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ABSTRACT

Process and temperature invariant voltage multiplier performance has been examined. The analytical predictions of ripple voltage and frequency response are in good agreement with ADS simulation results. In addition, a threshold voltage compensation scheme is investigated to improve the output voltage sensitivity against process variations and temperature fluctuation. The threshold voltage compensation technique effectively reduces the temperature and process variability on the voltage multiplier performance.

1. Introduction

Battery supported electrical systems have established themselves in numerous applications including cell phones and medical devices. However, durability of the battery is a major problem in some applications, such as implantable chips. That brings an interesting topic for batteryless electronic design. Energy is scavenged from an external source such as radio-frequency waves, piezoelectric energy, thermal energy, or solar energy. For such a system, harvesting energy from surrounding ambient is environmentally friendly and a good option for low maintenance.

Scavenging energy from piezoelectric, thermal, and solar energy has been well studied [1–7]. Radio frequency identification (RFID) is a popular application for remotely powered system. Thanks to higher level of integration, RFID tags nowadays are dramatically smart with large amount of memory and sensor capabilities. By using energy harvesting, the system can be employed without frequent human intervention [8]. Recently, batteryless wireless body area network systems are focus of research. For example, three body sensors, which use RF energy harvesting technique, are implemented in the human body to detect the signal of ECG, EEG, and EMG [9]. Parks et al. [10] successfully performed a sensor operation by a 500 MHz digital TV broadcasting radio signal. Olgun et al. [11] developed a technique to drive a sensor using Wi-Fi signal, which is operated at frequency of 2.45 GHz. RF powered micro-systems hold the promise of the smallest, lightest and in many cases the cheapest system solution.

As RF energy harvesting is to convert ambient radio-frequency signal to DC supply voltage, a high efficient rectifier design becomes very important. Because of its low turn-on voltage, the Schottky diode has been used for wireless powered systems [12]. The diode technique, however, is not compatible with current CMOS technology. Thus, the threshold voltage (V_{th}) cancellation technique in CMOS technology is utilized to improve the efficiency [13,14]. Other papers focus on the improvement of sensitivity using an off-chip impedance matching network [15] and temperature and process compensation techniques [16]. However, reliability analysis on voltage multiplier for RF energy harvesting has not been studied yet.

In this paper, the temperature and process variability on p-channel MOSFET voltage multiplier has been examined. Section 2 presents the operation of the voltage multiplier and the key parameters for model predictions. The model predictions are compared with ADS simulation. Section 3 describes the design of threshold voltage compensation and circuit implementation. Impact of temperature and process variations on voltage multiplier with or without threshold voltage compensation is compared. Finally, the conclusion is given in Section 4.

2. Analysis and evaluation of the voltage multiplier

RF energy harvester is mainly made of several elements: on-chip antenna, RF–DC rectifier, storage capacitor, and voltage regulator. In this section, the operation principle of MOSFET-based voltage multiplier and the analysis for key parameters is presented.

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2.1. Operation principle of n-stage voltage multiplier

The Greinacher principle [17] can be used to build a voltage multiplier to supply the energy harvesting system. The three-stage voltage multiplier is shown in Fig. 1. This n-stage voltage multiplier consists of a cascade of n-low threshold p-channel MOSFETs, which gate and source terminals are connected. The coupling capacitor in each stage pumps the voltage to a high potential level. Each p-channel MOSFET here functions as a diode, which switches on and off by different cycles. The input signal is a cosine waveform with an output amplitude V_m and frequency f_0.

$$V_{RF} = V_m \cos(2\pi f_0 t) \tag{1}$$

The basic circuit operation is explained as follows: The nth stage unit cell is shown in Fig. 2 (a) and (b). $C_{H(n)}$ is the horizontal capacitor. $C_{V(n)}$ and $C_{V(n-1)}$ are the vertical capacitors.

During the negative cycle of input signal shown in Fig. 2(a), with the decrease of input signal, V_k decreases as well, the transistor $M_{P(n)}$ turns on. The current flows from the capacitor $C_{H(n)}$ to $C_{V(n)}$. When an input signal changes to the positive cycle in Fig. 2(b), V_k increases as well as the input. The transistor $M_{p(n-1)}$ turns on, and transistor $M_{p(n)}$ turns off. Then, the current flows from the capacitor $C_{V(n-1)}$ to the capacitor $C_{H(n)}$. Essentially, Fig. 2(b) is a diode clamp (doubler) circuit. The capacitor is charged on the negative half cycles to the peak AC voltage (V_{pk}). The output is the superposition of the input AC waveform and the steady DC of the capacitor. The effect of the circuit is to shift the DC value of the waveform. The negative peaks of the AC waveform are "clamped" to 0 V (actually $-V_{DROP}$, the small forward turn-on voltage of the diode) by the diode. Therefore the positive peaks of the output waveform are $\sim 2V_{pk}$. Fig. 2(a) serves as a rectifier to convert a sinusoidal input waveform to a quasi-DC signal. After n-stage operations, the input signal is multiplied to the load capacitor CL.

In Fig. 1 the gate terminal is connected to the source terminal. Thus, V_{out} for the n-stage multiplier is:

$$V_{out} = 2n \times (V_{RF} - V_{DROP}) = 2n \times (V_{RF} - |V_{TP}|) \tag{2}$$

In Fig. 2 the threshold voltage of the p-channel transistor is a function of body-source bias V_{BS} as:

$$V_{TP} = V_{TP0} + \gamma\left(\sqrt{|2\phi_F - V_{BS}|} - \sqrt{|2\phi_F|}\right) \tag{3}$$

where V_{TP0} is the threshold voltage without the body effect, γ is the body effect factor, and ϕ_F is the Fermi potential. With a decrease in threshold voltage magnitude, the DC output voltage becomes higher. To eliminate the body effect, the body terminal can be tied to the source.

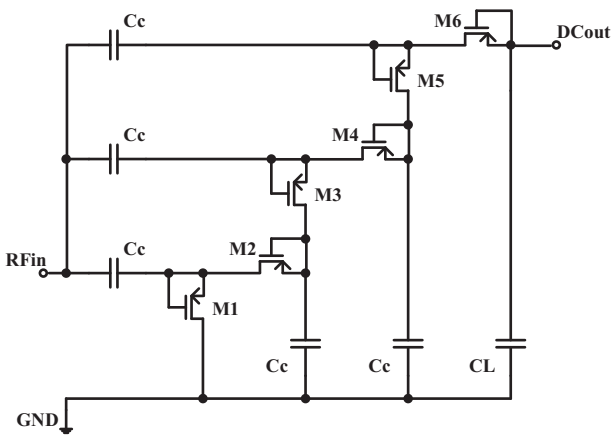

Fig. 1. Schematic of a p-channel MOSFET voltage multiplier.

2.2. Key parameters and reliability issues

The output of voltage multiplier has an ac ripple [18]. The ripple voltage is given by:

$$V_{Ripple} = \frac{I_{out}}{f_c C_L} = \frac{V_{out}}{f_o R_L C_L} \tag{4}$$

where I_{out} is the output current and R_L is the load resistance.

Fig. 3 shows the ADS simulation result compared with the analytical predictions. It is clear from this figure that the ripple voltage decreases with an increase in operation frequency.

In Fig. 3 the frequency is swept from typical 900 MHz to 2.4 GHz used in wireless communications. As the frequency varies not only the ripple voltage, but the output voltage of the rectifier changes as well. The output voltage as a function of the optimal load resistance at the operation frequency is given by [19]:

$$V_{out} = \sqrt{KC_L R_L f_o} \tag{5}$$

where K is a constant with a unit of V^2.

Fig. 4 displays the ADS simulation results compared with the model predictions. Excellent agreement between the model predictions and simulation results is obtained. In this figure, $K = 0.32\ V^2$ is used. Comparing with the ripple voltage in Fig. 3, the output voltage in Fig. 4 is more sensitive to frequency of operation.

For p-channel transistors used in the voltage multiplier, negative bias temperature instability (NBTI) is a major reliability concern. NBTI is mainly caused by the interfacial layer hydrogen diffusion into the SiO_2 insulator and partial recovery associated with reduction in traps [20]. NBTI manifests as an increase in the threshold voltage magnitude and a decrease in drain current. The shift of threshold voltage due to NBTI is expressed as power-law time dependence. After the aging time above 10^6 s, the threshold voltage increases and the circuit performance degradation can reach up to 15% [21]. To account for the NBTI threshold voltage drift, the output voltage as a function of V_{TP} is simulated. The model predictions and ADS simulation results are shown in Fig. 5. As seen in this figure the output voltage increases with a decrease in threshold voltage magnitude.

It is worth pointing out that the threshold voltage strongly dependent on temperature [22]:

$$|V_{TP}| = |V_{TP0}(T_0)| - \alpha_T(T - T_0) \tag{6}$$

α_T lies in the range of 0.5–4 mV/K. In our case, $\alpha_T = 0.6$ mV/K and $V_T(T_0) = -0.44$ V are used. With the increase of temperature, the threshold voltage would be decreased. The decrease in threshold voltage leads to an increase in the output voltage of the voltage multiplier. The temperature dependent characteristics are evaluated with a temperature sweep from −50 to 100 °C. As seen in Fig. 6 the ADS simulation results are in good agreement with the model predictions. The simulation results show that the output voltage increases with temperature as predicted. The increase of temperature can be from device self-heating or ambient temperature rises.

3. Threshold voltage compensation design and analysis

3.1. Model of threshold voltage compensation

As (2) implies that the output voltage reduces because of the transistor threshold voltage. If a DC offset voltage is applied between the gate and source, the transistor can turn on below the threshold voltage. Thus, the output voltage may increase. Fig. 7 shows the voltage multiplier using a DC offset voltage at the gate of each p-channel transistor.

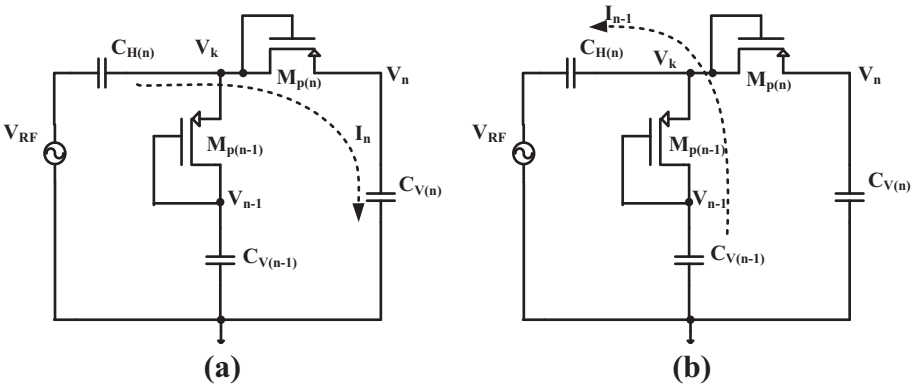

Fig. 2. (a) Negative cycle of input signal and (b) positive cycle of input signal.

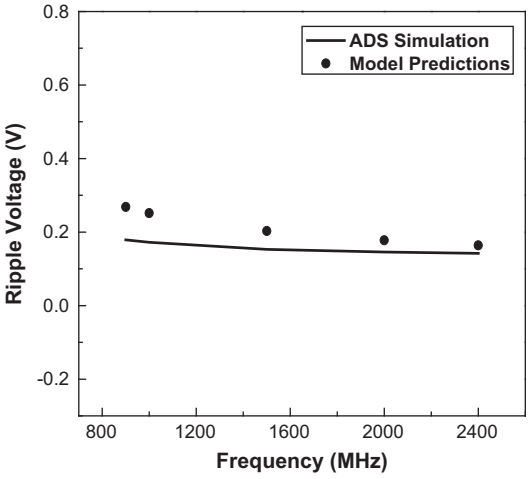

Fig. 3. Ripple voltage as a function operation frequency.

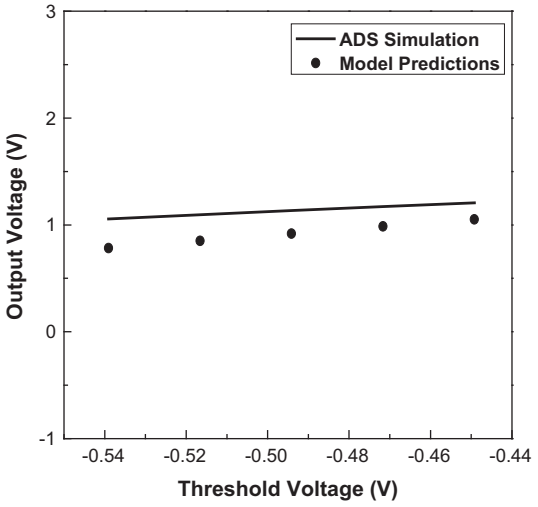

Fig. 5. Output voltage versus threshold voltage drift.

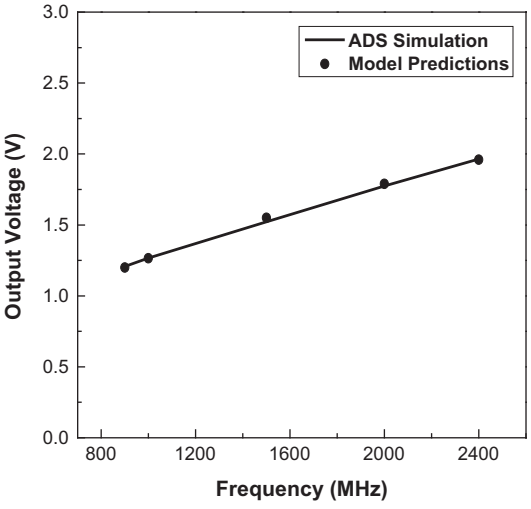

Fig. 4. Output voltage versus frequency.

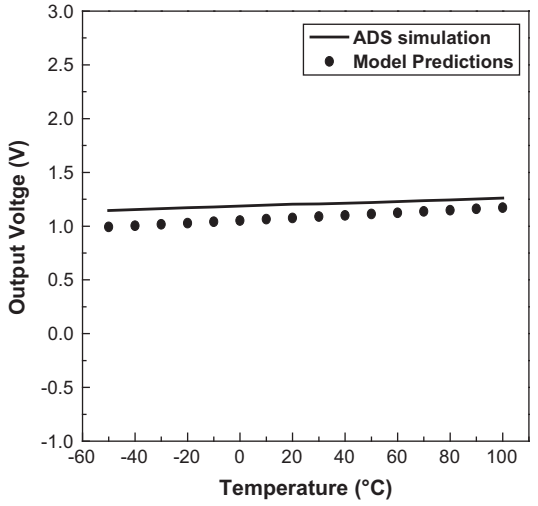

Fig. 6. Output voltage versus temperature.

If the DC offset voltage is equal to the threshold voltage, the turn-on voltage loss is removed. The ideal output voltage of the voltage multiplier is then equal to the input amplitude times the number of stages. In the voltage multiplier, the power conversion efficiency is expressed as:

$$\eta_{PC} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{V_{out} I_{out}}{V_{in} I_{in}} \tag{7}$$

where P_{out} is the power delivered to the load, P_{in} is the power available at the source, and P_{loss} donates the power loss in each

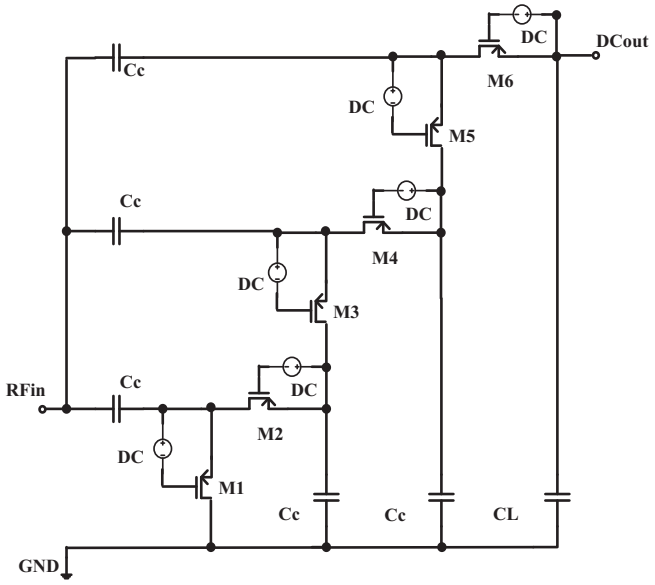

Fig. 7. Voltage multiplier using DC offset voltage between the gate and source of each transistor.

transistor. Note that the voltage conversion efficiency is defined by V_{out}/V_{in} [23].

The voltage and power conversion efficiency of the voltage multiplier are simulated at the input voltage amplitude of 800 mV at 900 MHz. The coupling capacitor is 900 fF and the load resistor is 5 kΩ. As shown in Fig. 8 the output voltage is 1.2 V for the circuit without any DC offset at the gate of pMOS. However, the output voltage increases to 2.2 V at the offset voltage of 0.6 V. For the power conversion, the power conversion efficiency increases with DC offset voltage, reaches the maximum at DC offset of 0.5 V, but decreases afterwards. The decrease in power conversion efficient beyond 0.5 V DC offset voltage is due to reverse leakage current. The leakage current consumes more power, which makes the power conversion efficiency to drop (see Fig. 9).

3.2. Implementation of the threshold voltage compensation scheme

In order to achieve the concept of threshold voltage compensation, Fig. 10 provides the circuit schematic of the voltage multiplier with the compensation circuit. The auxiliary bias circuit is added to

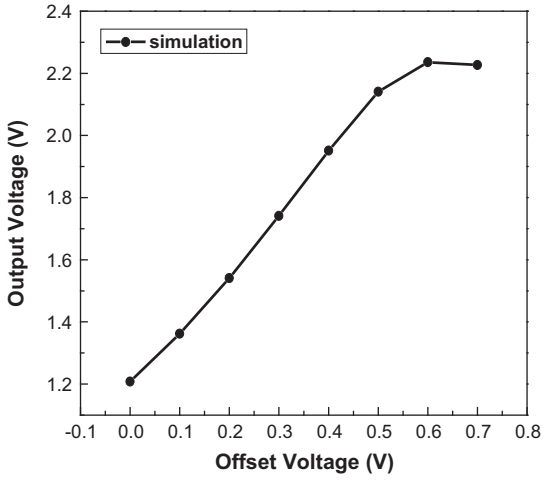

Fig. 8. Voltage conversion on bias voltage at 900 MHz input signal.

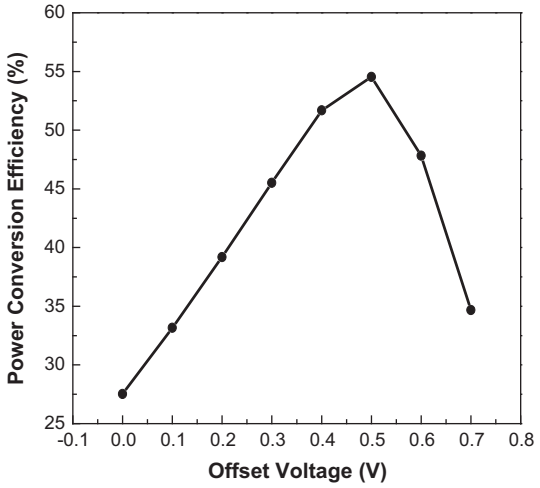

Fig. 9. Power conversion efficiency on bias voltage at 900 MHz input.

the transistors M2 and M4. For the first stage, an isolated pMOS diode M7 is added to the main transistor M2, which connects between the source and the gate of M2. The resistor value $R1$ adjusts the appropriate voltage drop of M7. The threshold compensation voltage is described by the V_{drop} on the transistor M7. A decoupling capacitor Cc is added to remove the RF input that couples through the gate-to-source of transistor M2. Biasing resistor $R1$ is typically large, because it can reduce the power imposed on the transistor M7. Also, the big resistance improves the stability of the entire output voltage. For example, when the threshold voltage decreases due to process variation, it produces more drain current and voltage drop $I_D \times R1$ on the biasing resistor $R1$ leading to a smaller source-to-gate voltage on main transistor M2. The smaller V_{SG} reduces the drain current and compensates the initial increase in I_D.

In Fig. 10 two auxiliary bias circuits are implemented on the first and second stages of the voltage multiplier. In this circuit design, all transistors M1–M8 are p-channel MOSFETs, which have 20 fingers and 1.5 μm channel width on each finger. The standard threshold voltage is −0.45 V for 0.18 μm mixed-signal RF technology. In our design, the coupling capacitor Cc is 900 fF, and the output storage capacitor CL is 1 pF. In addition, the output load resistance R_L is 5 kΩ and the bias resistor $R1$ and R_2 is 8 kΩ. The voltage multiplier operates at 900 MHz with an 800 mV amplitude RF input signal. The threshold compensation in Fig. 10 can be improved using a p-channel transistor to substitute the resistor as shown in Fig. 11. For example, M2, M7, R1, Cc (and M4, M8, R2, Cc) in Fig. 10 can be replaced by M1, M2, M3, Cc in Fig. 11. In Fig. 11 the forward current of a pMOS transistor in saturation can be written as:

$$I_{D1} = \frac{\beta_1}{2}\left(V_{SG1} - |V_{tp}|\right)^2 = \frac{\beta_1}{2}\left(V_{in} - V_{out} + V_{SG2} - |V_{Tp}|\right)^2 \tag{8}$$

where $\beta_1 = \mu_{p1} C_{ox} W_1/L_1$.

As seen in Fig. 11 then output current can be written as:

$$I_{out1} = I_{D1} - I_b \tag{9}$$

where I_b due to the transistor M2 in subthreshold conduction is expressed as:

$$I_b = I_s \times e^{\frac{q\left(V_{SG2} - |V_{Tp}|\right)}{nkT}} \tag{10}$$

In (10) I_s is the specific current given by $2n\beta_2(kT/q)^2$, where n is the slope factor which is normally 1.2–1.6 in CMOS technology.

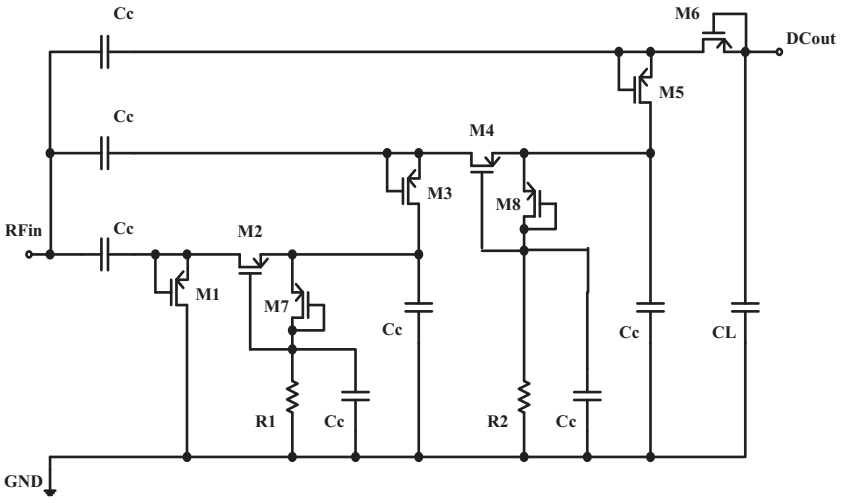

Fig. 10. Implementation of the threshold compensation of voltage multiplier.

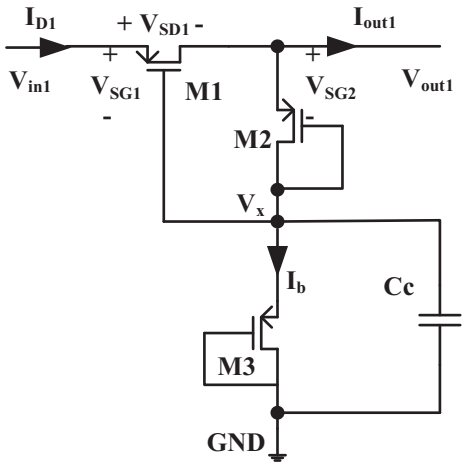

Fig. 11. Improved V_T compensation using a pMOS to replace the resistor.

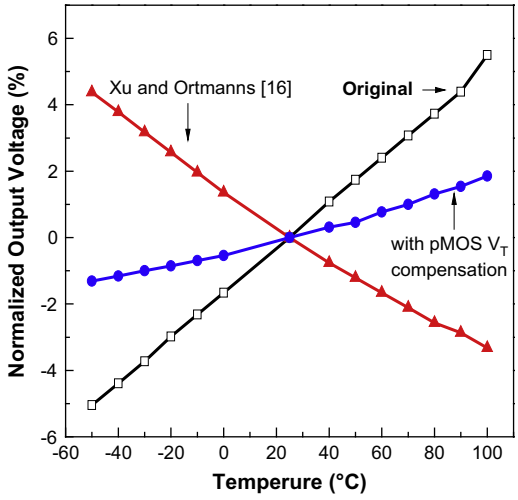

Fig. 12. Normalized output voltage versus temperature.

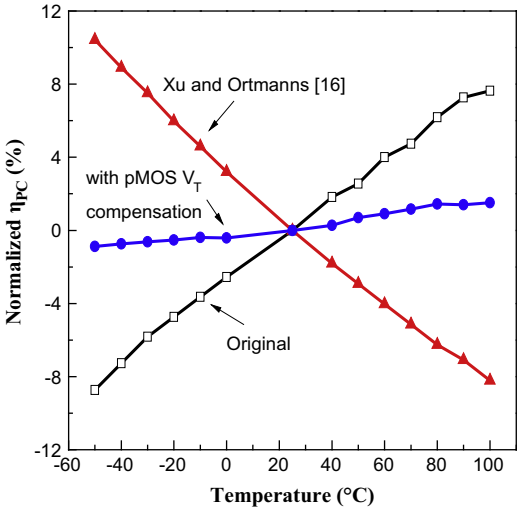

Fig. 13. Normalized power conversion efficiency versus temperature.

As seen in (10) if $|V_{tp}|$ goes up, I_b drops and the effective channel resistance R_{Ch} of M3, which is inversely proportional to its channel current, goes up. The node voltage V_x (=$I_b \times R_{Ch}$) is, thus, relatively unchanged. This makes V_{SG1} stable. Also, when $|V_{tp}|$ goes up, I_{D1} decreases according to (8). The decrease in I_{D1} and I_b simultaneously results in a relatively stable output current and output voltage using the V_T compensation scheme in Fig. 11.

The ADS simulation is performed with a temperature sweep from −50 to 100 °C. The output voltage and power conversion efficiency normalized to its respective value at 25 °C as a function of temperature for the voltage multiplier with and without compensation scheme are compared in Figs. 12 and 13, respectively. In these figures, the empty squares represent the normalized output voltage using the original circuit without any compensation, the solid triangles represent the normalized output voltage using the compensation circuit by Xu and Ortmanns [16], and the solid circles represent the normalized V_{out} using the V_T compensation with p-channel transistors. As seen in Fig. 12 the output voltage temperature sensitivity of the voltage multiplier with threshold voltage compensation by p-channel transistors reduces significantly compared to the original circuit without compensation (resulting in a positive temperature coefficient) and the compensation circuit by Xu and Ortmanns [16] (resulting in a negative temperature coefficient). For example, the output voltage sensitivity at 100 °C reduces from about 5% to 1.8% after compensation. Fig. 13 shows the normalized power conversion efficiency versus temperature.

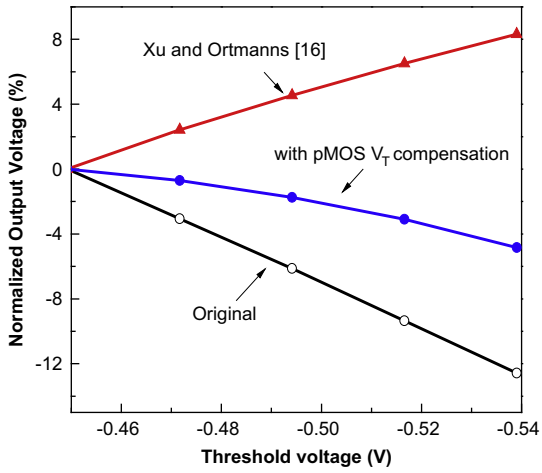

Fig. 14. Normalized output voltage versus threshold voltage drift.

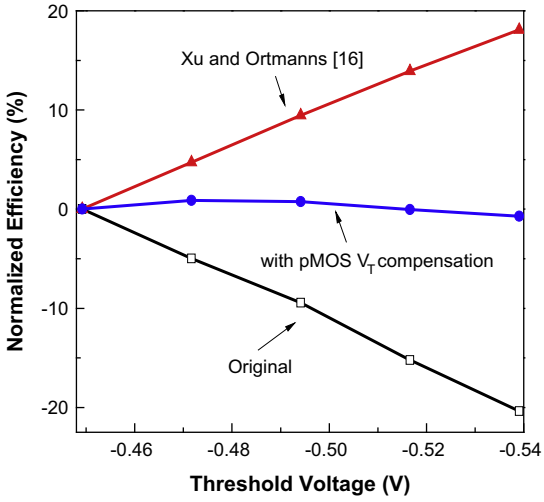

Fig. 15. Normalized power conversion efficiency versus threshold voltage drift.

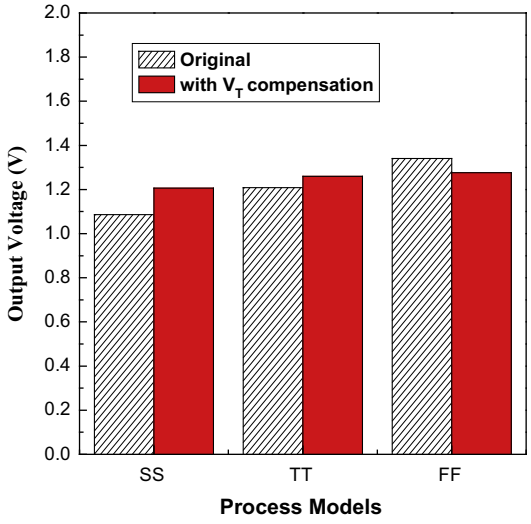

Fig. 16. Output voltage versus process models.

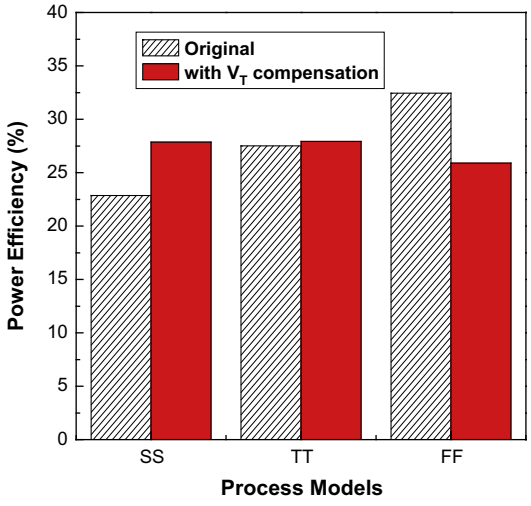

Fig. 17. Power conversion efficiency versus process models.

The voltage multiplier with V_T compensation using p-channel transistors clearly reduces the power conversion efficiency temperature sensitivity significantly. At 100 °C the η_{PC} sensitivity reduces from about 10% to 1.5% using the pMOS threshold voltage compensation.

Reliability effects such as threshold voltage degradation in the voltage multiplier with the compensation circuit using Fig. 11 in Fig. 10 are further evaluated. Fig. 14 shows that the normalized output voltage and Fig. 15 displays the normalized power conversion efficiency versus threshold voltage shift for the voltage multiplier with or without threshold voltage compensation. Again, the compensation circuit effectively reduces the threshold voltage drift effect on the output voltage and power conversion efficiency as shown in Figs. 14 and 15. For example, when $|V_{tp}|$ goes up, I_{D1} and I_b decrease simultaneously according to (8) and (10). This results in a relatively stable output current in (9) using the V_T compensation scheme in Fig. 11. Consequently, their normalized output voltage and power conversion efficiency are less sensitive to threshold voltage shift resulting from reliability degradation. On the other hand, the use of the resistor in the compensation circuit in [16] shows positive threshold voltage sensitivity. For instance, when $|V_{tp}|$ increase, I_b decreases. Since the resistor R provides a constant resistance, the node voltage V_x ($=I_b \times R$) thus decreases. This results in an increase in V_{SG1}. Therefore, the output current in (9) increases. The output voltage and power efficiency using the compensation circuit in [16] show significant threshold voltage sensitivity as evidenced by the simulation results in Figs. 14 and 15.

To further examine the reliability impact on voltage multiplier, ADS simulation using different process models has been performed. The output voltage and power conversion efficiency versus process models for the voltage multiplier with and without compensation are compared in Figs. 16 and 17, respectively. There are three process models evaluated; namely, slow nMOS slow pMOS (SS model), typical nMOS typical pMOS (TT model), and fast nMOS fast pMOS (FF model). As seen in Figs. 16 and 17, the circuit with V_T compensation shows less process variation impact compared to those of the original circuit, especially for the power conversion efficiency.

4. Conclusion

Reliability and process variability of the voltage multiplier for RF energy harvesting have been studied. Effects of threshold voltage drift due to p-channel transistor negative bias temperature

instability and temperature variation are examined. The use of a DC offset voltage at the gate of pMOS and a p-channel transistor to replace the compensation resistor reduces the sensitivity of the output voltage and power conversion efficiency of the voltage multiplier. The voltage multiplier using our modified threshold voltage compensation technique above provides robust circuit performance against process variations and temperature drift for long term reliability.

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