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High-efficiency CMOS rectifiers with wide power dynamic range based on leakage-current-suppressing and adaptive-biasing techniques for RF energy harvesting

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ABSTRACT

This article proposes two high-efficiency CMOS rectifiers with wide power dynamic range (WPDR) for radio frequency energy harvesting (RFEH). The first rectifier (LCS-R1) incorporates a leakage-current-suppression (LCS) technique to enhance power conversion efficiency (PCE) by dynamically reducing the drain–source voltage (V_{DS}) of the main transmission MOSFETs, which minimizes power dissipation. Based on the LCS-R1 architecture, the second rectifier (LCSAB-R2) integrates gate and substrate adaptive-biasing techniques to reduce the effective threshold voltage (V_{TH}) of the MOSFETs. The LCS and adaptive-biasing techniques demonstrate good compatibility, enabling the LCSAB-R2 achieves improved PCE and extended power dynamic range (PDR). To validate the proposed schemes, both rectifiers are implemented in a TSMC 40 nm CMOS process with chip areas of 0.0121 mm^2 and 0.0036 mm^2, respectively. Simulation results demonstrate that LCS-R1 and LCSAB-R2 achieve peak PCEs of 69% and 89.4% at 433 MHz with a 200 kΩ load. Furthermore, the PDR for PCE > 40% are 23 dB and 27.7 dB, respectively.

1. Introduction

Wireless energy harvesting is a technology that utilizes RF signals in the environment as an energy source, which has broad application prospects and potential. With the popularization of low-power electronic devices and the rapid development of wireless sensor networks [1,2], it has become increasingly important to find sustainable energy solutions to replace traditional battery power [3]. RF energy harvesting has garnered widespread attention as a sustainable and efficient energy solution.

RFEH technology is widely utilized in wireless power supply applications, including wireless sensor networks (WSNs) and wireless power transmission (WPT). Its adoption aims to decrease battery usage, reduce environmental pollution, and improve system durability. WSNs are networks of many distributed sensor nodes for collecting and transmitting environmental data [4]. These sensor nodes are typically powered by batteries, which have limited capacity. As a result, their batteries require periodic replacement and disposal, which can pose environmental pollution risks if not handled properly. RFEH technology offers an alternative power supply solution for WSNs, reducing the reliance on batteries in such devices.

By integrating RFEH technology into WSNs, sensor nodes can harvest energy from the surrounding RF environment, which typically provides power densities ranging from 0.08 nW/cm^2 – 1 μW/cm^2 [5]. This approach not only eliminates the need for frequent battery replacements, reducing the generation of used batteries and their associated environmental pollution, but also significantly lowers the maintenance costs of WSNs by saving time and human resources.

The application of RFEH technology has the potential to greatly enhance the sustainability and reliability of WSNs [6]. By embedding RFEH systems into individual wireless communication devices, the reliance on traditional batteries can be substantially minimized. This integration reduces the size of the required batteries, decreases the frequency of replacements, and, in some cases, may eliminate the need for batteries altogether.

RFEH technology faces several challenges in wireless power supply applications, including the low energy density of RF signals, limited transmission distance, low energy conversion efficiency. Additionally, fluctuations in signal strength and availability can adversely affect the performance and stability of RF energy harvesting systems [7]. To address these challenges, achieving high PCE and a WPDR is critical in the design of RF energy harvesting systems. Moreover, evaluating

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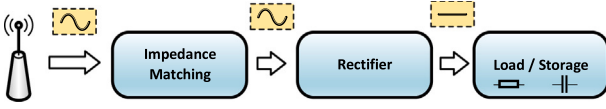
Fig. 1. Conceptual block diagram of RF energy harvesting system.

Fig. 2. Schematic of the N-stage Dickson charge pump rectifier.

Fig. 3. Schematic of the Cross-Coupled Differential Drive (CCDD) rectifier.

the specific application scenarios is essential to ensure the system's feasibility and adaptability. This evaluation helps guarantee that the RF energy harvesting system meets the power supply requirements of the intended application while maintaining reliable operation.

A conceptual block diagram of the RF energy harvesting system is shown in Fig. 1. The system includes an antenna or receiver that collects RF energy and channels it through a matching network to an RF-to-DC rectifier, which efficiently converts the harvested RF signals into DC power [8]. The converted DC energy is then delivered to a power management circuit for voltage regulation and current control, ensuring the device's operational requirements are met. Additionally, some RF energy harvesting systems integrate energy storage devices, such as batteries or supercapacitors, to store energy and provide power when RF signals are unavailable. Power losses occur during the transmission of RF energy from the antenna input to the load, with the RF-DC converter or rectifier module being the primary source of these losses. Therefore, minimizing energy loss in this module is a key focus of research.

Fig. 2 shows a traditional Dickson rectifier design that uses a diode-connected MOSFET instead of a Schottky diode. This approach was more cost-effective due to its compatibility with CMOS processes. However, the diode-connected MOSFETs had a high threshold voltage, which reduced both PCE and sensitivity at low input power levels. To address this issue, a static threshold compensation technique was introduced. While this technique successfully lowered the threshold voltage, it also increased power loss due to reverse leakage current. Subsequently, differential-driven CMOS rectifiers were proposed [9], as illustrated in Fig. 3. This topology reduces on-resistance and reverse leakage current in MOSFETs, enhancing sensitivity with its differential input design. Nevertheless, at high input power levels, the reverse leakage current increases significantly, leading to a drop in PCE and limiting the dynamic range (DR) of the CCDD topology. Various methods and techniques have since been developed to mitigate reverse leakage current. Despite its limitations, the CCDD rectifier remains widely used in many energy harvesting systems due to its simplicity and effectiveness.

In [10], an adaptive-biasing technique is proposed to supply bias current to the gate of the PMOS transistor, thereby limiting power loss at high input power levels. However, the complexity of the bias circuit restricts its impact, as it only addresses power consumption in the PMOS. In [8,11], a diode-connected structure is introduced as a bias circuit for double-sided rectifiers, which effectively reduces the rectifier's power consumption, achieving a peak PCE of 86%. In [12], a stacking diode structure is employed to bias the NMOS transistor, resulting in significant reduction in power consumption at high input power levels. Additionally, in [13], an adaptive-biasing technique is used to reduce the threshold voltage of MOS transistors, leading to a dynamic range of 14.5 dB.

This paper presents a LCS technique that effectively mitigates reverse leakage current under high input power, thereby improving the
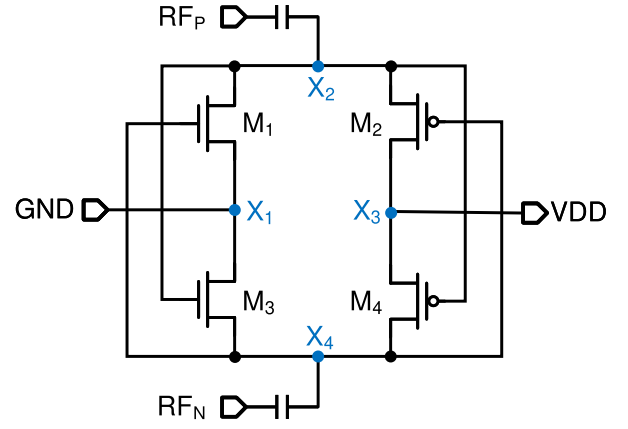
dynamic range of the rectifier. Additionally, adaptive-biasing techniques are applied to the gate, leading to a significant enhancement in the PCE of the rectifier. The application of dynamic substrate biasing on the PMOS substrate further reduces the effective threshold voltage, thereby improving the rectifier's sensitivity. The structure of the paper is as follows: Section 2 analyzes the factors contributing to the decline in power transfer efficiency in conventional rectifiers. Section 3 introduces the proposed rectifiers and presents the corresponding simulation results. Section 4 provides a conclusion.

2. Technical analysis

The CCDD rectifier is shown in Fig. 3. The device is capable of achieving high sensitivity and high PCE, although it is worth noting that its performance may be limited to a narrow input power range. We designed a CCDD-structured rectifier using a TSMC 40 nm process for simulation and analysis. To compare the proposed rectifier, a 200 kΩ resistor was used as the load.

Since impedance matching network design is not considered in this study, the actual power absorbed by the rectifier, denoted as P_{abs}, must be determined to accurately evaluate its PCE. This is accomplished by measuring the input reflection coefficient (S_{11}) and calculating the absorbed power as:

$$P_{abs} = P_{inc}\left(1 - |S_{11}|^2\right) \tag{1}$$

where P_{inc} is the incident power delivered by the source, $|S_{11}|$ is the magnitude of the reflection coefficient at the operating frequency, $|S_{11}|^2$ represents the fraction of incident power that is reflected due to impedance mismatch [14].

As shown in Fig. 4, the peak PCE of 76.8% is achieved at an input power level of −27.2 dBm. However, the PCE gradually decreases with increasing input power due to the rise in reverse leakage current.

The next part will analyze the reasons for the decrease in PCE under high input power conditions.

Fig. 5 shows the transient voltage and current waveforms of the NMOS transistors (M1, M3) at $P_{abs} = -25$ dBm. One operating cycle exhibits both forward and reverse conduction regions. As $V_S > V_D$, the MOSFET enters the cutoff region when $V_{GD} \ll V_{TH}$. The reverse leakage current in this region is approximately 31 nA, which can be considered negligible. As V_{GD} increases, the device transitions from the cutoff region into the subthreshold region.

The drain current of an NMOS transistor operating in the subthreshold region can be expressed as:

$$I_D = I_0 \cdot \exp\left(\frac{V_{GS} - V_{th}}{n \cdot U_T}\right) \cdot \left(1 - \exp\left(-\frac{V_{DS}}{U_T}\right)\right) \tag{2}$$
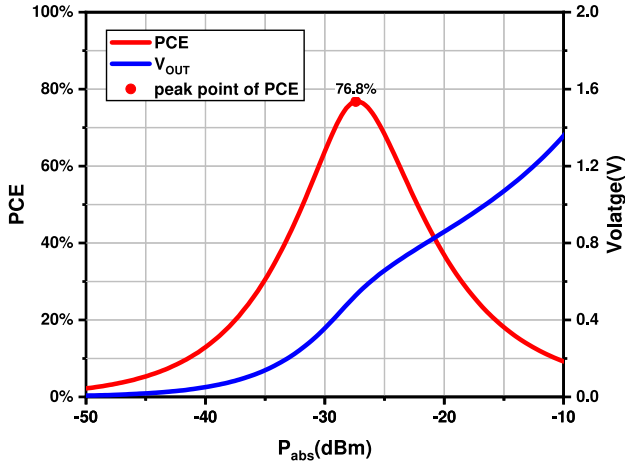
Fig. 4. Simulated PCE of the CCDD rectifier versus P_{abs} at a load of $200\,\text{k}\Omega$.
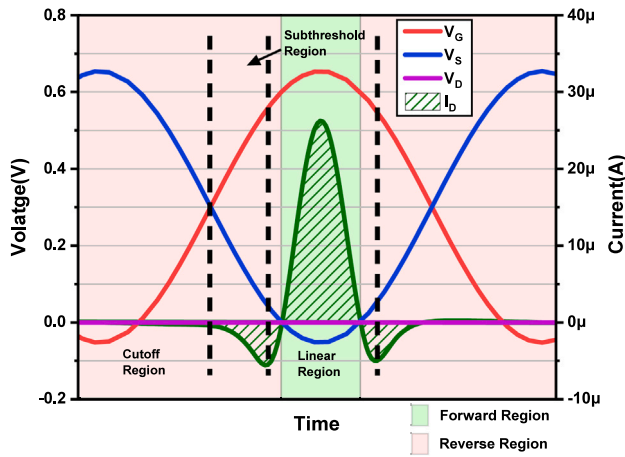

Fig. 5. Transient waveform of NMOS transistor (M_1,M_3) within one operating cycle at $P_{abs} = -25\,\text{dBm}$.

Fig. 6. Simulated current through NMOS transistor (M_1,M_3) at different input powers within one operating cycle.

where I_0 is a device-dependent current coefficient incorporating process and geometric parameters, n is the subthreshold swing factor, and U_T is the thermal voltage. For $V_{DS} > 3U_T$, the exponential term $(1 - \exp(-V_{DS}/U_T))$ approaches unity, resulting in a simplified expression:

$$I_D = I_0 \cdot \exp\left(\frac{V_{GS} - V_{TH}}{n \cdot U_T}\right) \tag{3}$$

When $V_D > V_S$, the MOSFET operates in the forward conduction mode and remains in the linear region. The drain current I_D in the linear region of a MOSFET is given by:

$$I_D = k'\left(\frac{W}{L}\right)\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \tag{4}$$

where I_D denotes the drain current, k' is a process-dependent transconductance parameter, W and L are the channel width and length of the MOSFET, respectively, V_{GS} is the gate-to-source voltage, V_{th} is the threshold voltage, and V_{DS} is the drain-to-source voltage.

Fig. 5 shows that the NMOS transistor enters the reverse conduction region twice within one operating cycle. The peak reverse and forward currents are 5.3 µA and 25 µA, respectively. This indicates that the reverse leakage current is non-negligible.

The PMOS transistor (M_2, M_4) will also exhibit reverse leakage current. In the CCDD structure, the alternating conduction of NMOS and PMOS tra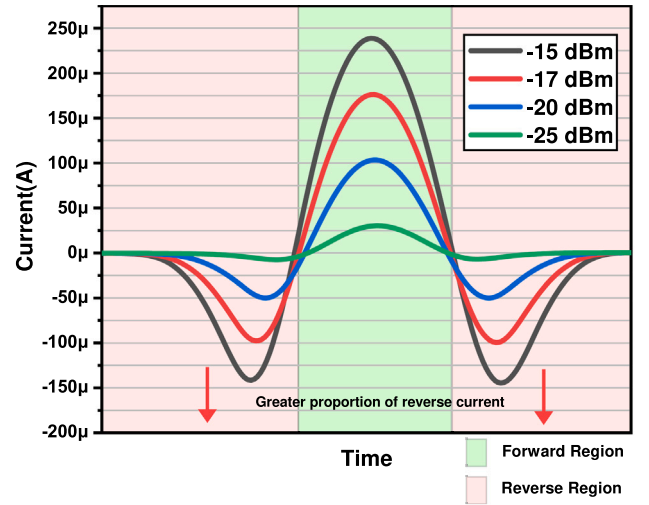nsistors causes the RF port capacitance to alternate between charging and discharging states. This alternation ultimately allows the current to flow from GND to the VDD port, completing the RF to DC conversion.

It is well known that PCE is significantly influenced by reverse leakage current [14]. Fig. 6 shows the transient conduction current of the NMOS transistor (M_1,M_3) tested under different input power levels. As the input power increases from -25 dBm, the proportion of reverse leakage current gradually increases, leading to a gradual decrease in PCE. The results are consistent with the PCE curve shown in Fig. 4.

Since the forward current through the rectifier is an inevitable consequence of its operation, one approach to enhancing the PCE of the rectifier is to reduce the proportion of reverse leakage current in the total current over a single cycle. In order to more accurately represent the impact of reverse leakage current on PCE, it can be represented by measuring the power consumption of MOSFETs. Fig. 7 shows the power consumption of the MOSFETs when the rectifier's output voltage reaches 1 V. The data indicates that the peak power consumption of the NMOS is 20 µW, while that of the PMOS is 10 µW. In comparison, the load resistor consumes only 5 µW at this point. The MOSFETs consume most of the power, causing the PCE in this state to drop to 22.5% (Fig. 4). The large drain-to-source voltage differential during reverse leakage current significantly increases the power consumption. Specifically, the power dissipated due to reverse leakage current is approximately twice that of the forward conduction current.

Based on the power consumption analysis of the MOSFETs, two effective strategies to improve PCE are identified:

1. Reducing the proportion of reverse current during the MOSFET's operation cycle.
2. Minimizing the drain–source voltage V_{DS} of the MOSFETs.

This work enhances the PCE by decreasing the MOSFET's power consumption during rectifier operation through the mitigation of reverse leakage current and partial excess forward current.

3. Proposed design

3.1. Proposed LCS-R1

Fig. 8 illustrates the proposed LCS-R1. It employs the leakage-current-suppressing (LCS) technique. Depletion-type NMOS transistors configured in a diode-connected structure are added to both the DC
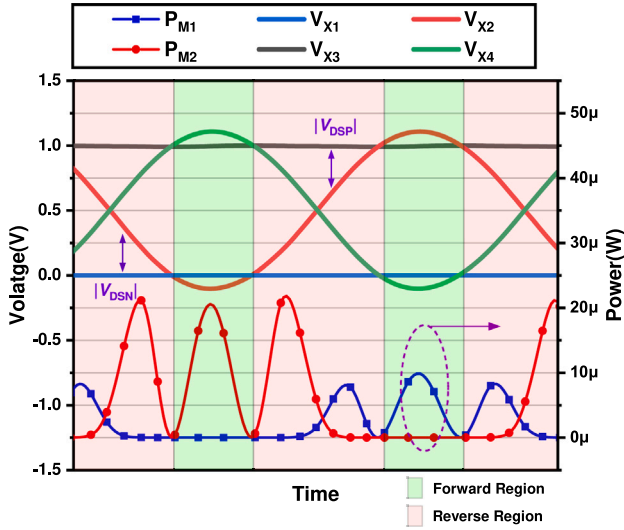
Fig. 7. Transient waveforms of MOSFETs voltage and power consumption in the CCDD rectifier at $V_{OUT} = 1\,$V.
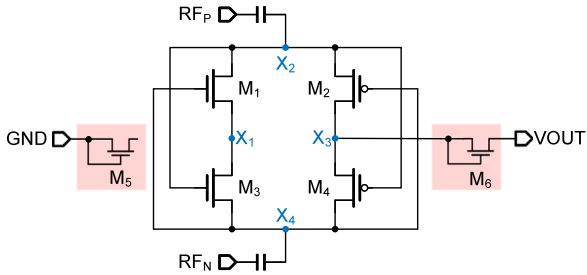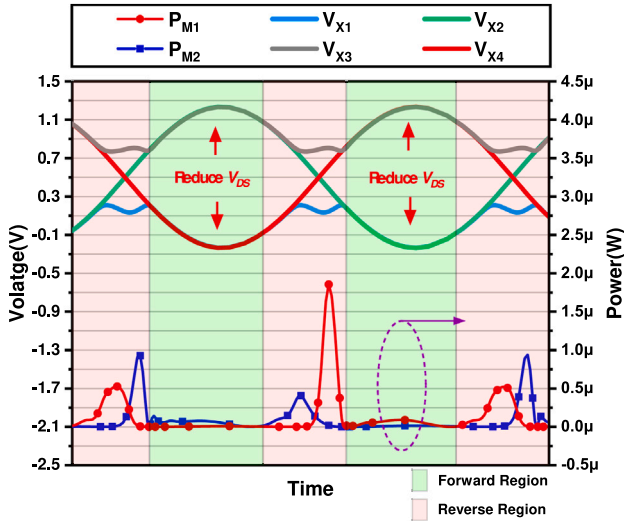

Fig. 8. Schematic of the proposed LCS-R1.

Fig. 9. Transient waveforms of MOSFET voltage and power consumption in the LCS-R1 at $V_{OUT} = 1\,$V.

voltage input and output ends of the rectifier. The use of depletion-type NMOS transistors ensures proper conduction at both the input and output ports even under low input power conditions, thereby maintaining high sensitivity. This circuit structure effectively reduces the reverse leakage current in the main MOS transistors (M$_1$–M$_4$), while also lowering their drain–source voltage V_{DS} during conduction.
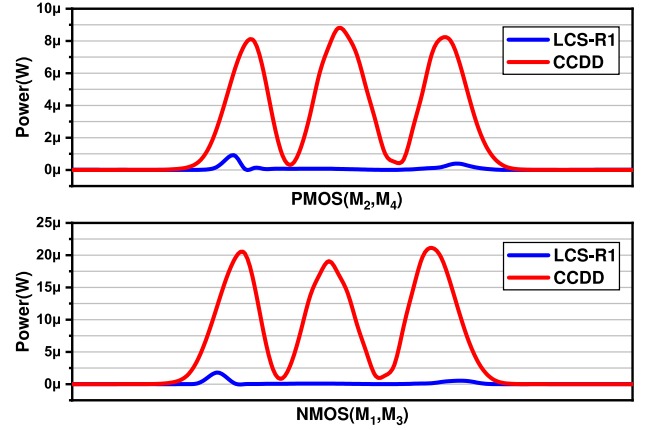

Fig. 10. Transient power consumption of the main transmission MOSFETs (M1-4) over one operating cycle in the CCDD and LCS-R1 at $R_L = 200\,$kΩ and $V_{OUT} = 1\,$V.

Fig. 9 shows the internal node voltages (X$_1$–X$_4$) of the LCS-R1 rectifier at 1 V output voltage, as well as the power consumption of MOSFETs M$_1$ and M$_2$. Unlike the CCDD rectifier, the voltage at node X$_1$ and X$_3$ is not fixed.

As the voltage at node V_{X_2} decreases and V_{X_4} increases, MOSFET M$_1$ turns on, leading to a rise in I_{M_1}. At this stage, M$_3$ remains in cutoff, resulting in $I_{M_1} = I_{M_5}$. The increase in I_{M_1} raises the drain–source voltage V_{DS,M_5} of M$_5$, which in turn causes a voltage drop at node X$_1$, as shown in Fig. 9. This voltage drop at X1 reduces V_{DS,M_1}, thereby limiting the current I_{M_1} and suppressing excessive power dissipation in M$_1$. Similarly, when V_{X_2} rises and V_{X_4} falls, M$_3$ and M$_5$ conduct, synchronizing the voltage at X$_1$ with V_{X_4}. Therefore, M$_5$ effectively suppresses the excess forward conduction current of M$_1$ and M$_3$, thereby reducing the power loss during conduction. Similarly, the LCS circuit at the output increases the voltage at node X$_3$ during forward conduction, thereby reducing the power dissipation of the PMOS transistor in its forward conduction state.

Similar to the limitation of forward current, when reverse leakage current occurs in M$_5$, the voltage at node V_{X_1} rises in response to the dynamic increase at nodes V_{X_2} or V_{X_4}, thereby reducing the V_{DS} of M$_1$/M$_3$. For the depletion-type NMOS transistor M$_5$, $V_{GS} = 0\,$V. When $V_{DS} > -V_{TH}$, the NMOS enters saturation. With $V_{TH} = -195\,$mV, the depletion-type NMOS can effectively suppress reverse leakage current even at moderate input power levels.

Since the node voltages V_{X_1} and V_{X_3} dynamically change with the direction of current flow, the LCS technique significantly suppresses both forward and reverse conduction losses. Fig. 10 shows a comparison of the power consumption in the MOSFETs of the proposed LCS-R1 and the CCDD.

As shown in Fig. 9, the LCS technique enables the main transmission MOSFETs (M$_1$-M$_4$) to operate with an extremely low V_{DS}, resulting in minimal power consumption. However, implementing the LCS technique requires precise adjustment of the width-to-length ratios (W/L) of MOSFETs M$_5$ and M$_6$. Otherwise, the dynamic range extension capability of the rectifier cannot be effectively achieved. Fig. 11 compares the dynamic range extension performance of the LCS structure across varying width-to-length (W/L) ratios of the MOSFETs. It is evident that an inappropriate W value can degrade either the PCE or the dynamic range. Therefore, a proper W value should be estimated during the design of the LCS structure.

Under steady-state operation of the rectifier, the DC level at node X$_2$ stabilizes at approximately half the output voltage ($V_{X_2} = \frac{1}{2}V_{OUT}$). Given $V_{RFP} = -V_{RF}$, this condition leads to $V_{X_2} = \frac{1}{2}V_{OUT} - V_{RF}$. Due to the negligible V_{DS} of M$_1$, we can approximate $V_{X1} \approx V_{X2}$. Since
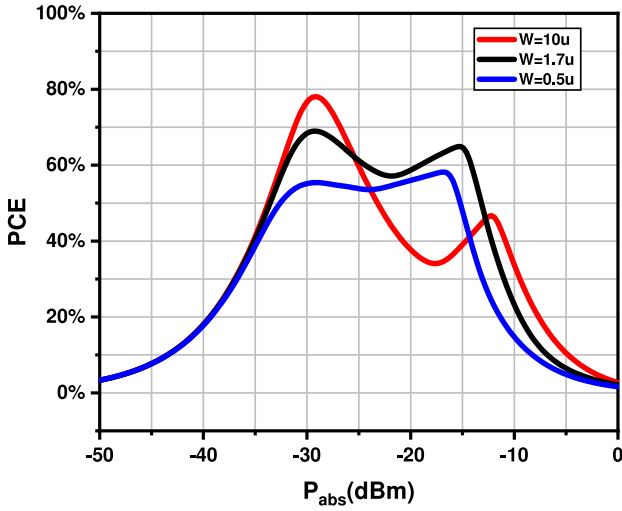
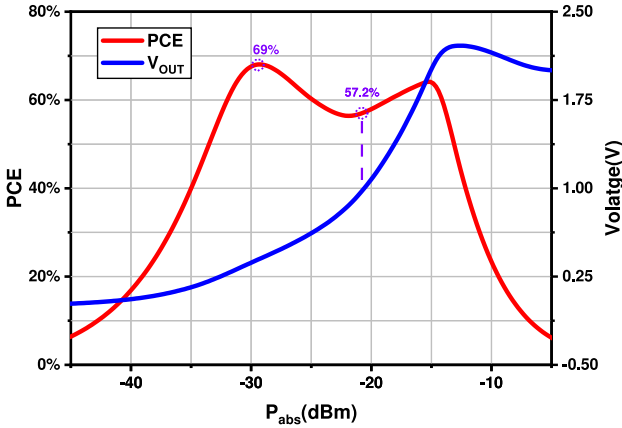**Fig. 11.** PCE of MOSFETs (M5, M6) with varying W/L ratios.

Fig. 12. Simulated PCE and V_{OUT} versus P_{abs} for the LCS-R1 with R_L = 200 kΩ.

Fig. 13. (a)-The proposed architecture, (b)-Schematic of the proposed LCSAB-R2 rectifier.

depletion-type NMOS transistors have $V_{TH} < 0$, for M5 we derive $V_{DS} < V_{GS} - V_{TH}$, placing it in the linear region. With $V_{GS} = V_{DS} = V_{RF} - \frac{1}{2}V_{OUT}$, the forward conduction current of M5 is obtained from (4) as:

$$
\begin{aligned}
I_D &= k'\frac{W}{L}\left(\frac{V_{DS}^2}{2} - V_{th}V_{DS}\right) \\
&= k'\frac{W}{L}\left[\frac{(V_{RF} - \frac{1}{2}V_{OUT})^2}{2} - V_{th}(V_{RF} - \frac{1}{2}V_{OUT})\right] \\
&= k'\frac{W}{L}\left(\frac{1}{8}V_{OUT}^2 + \frac{1}{2}(V_{th} - V_{RF})V_{OUT} \right. \\
&\quad \left. + \frac{1}{2}V_{RF}(V_{RF} - 2V_{th})\right)
\end{aligned}
\tag{5}
$$

From Fig. 9, approximately 50% of the operating cycle shows M5 conduction, leading to the estimation $I_{D,M5} \approx 2I_{OUT}$. Substituting into (5), we derive:

$$
\begin{aligned}
k'\frac{W}{L} &= \frac{2V_{OUT}}{R_L\left[\frac{1}{8}V_{OUT}^2 + \frac{1}{2}(V_{th} - V_{RF})V_{OUT} + \frac{1}{2}V_{RF}(V_{RF} - 2V_{th})\right]} \\
&= \frac{16V_{OUT}}{R_L\left[V_{OUT}^2 + 4(V_{th} - V_{RF})V_{OUT} + 4V_{RF}(V_{RF} - 2V_{th})\right]}
\end{aligned}
\tag{6}
$$

Using design parameters $V_{OUT} = 1$ V, $R_L = 200$ kΩ, and $V_{RF} = 0.6$ V (slightly higher than $\frac{1}{2}V_{OUT}$), process data yields $k' = 275.72\ \mu A/V^2$ and
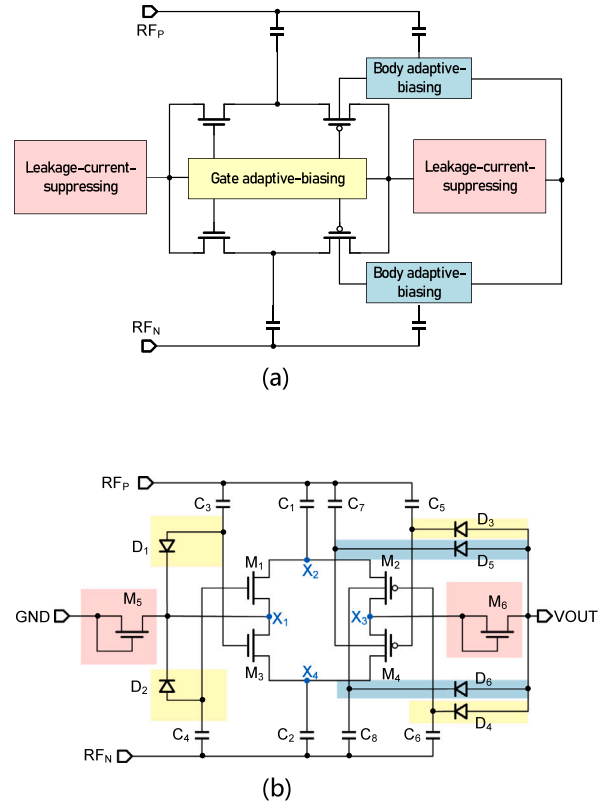
$V_{TH} = -195$ mV. Eq. (6) gives $W/L = 1.48$, leading to $W = 1.776\ \mu m$ for $L = 1.2\ \mu m$. Improper W/L selection for the LCS MOSFETs compromises the wide-dynamic-range performance. Excessive W increases the main MOSFETs' V_{DS} (no longer negligible), raising power consumption and degrading PCE at high input powers. Conversely, insufficient W limits the current supply capability of M5/M6 at low input levels, reducing rectifier sensitivity. Therefore, moderate W values are critical for optimal LCS performance.

The proposed LCS technique effectively minimizes the power dissipation of the main rectifying transistors (M1–M4), shifting the primary source of power consumption to the LCS structure (M5 and M6). This technique addresses the issue of reduced PCE in CCDD topology under high input power conditions, thereby expanding the power dynamic range (PDR) of the rectifier.

Fig. 12 shows the PCE and output voltage V_{OUT} of the LCS-R1 versus actual absorbed power P_{abs}. At a frequency of 433 MHz and a load of 200 kΩ, the peak PCE of the LCS-R1 achieves 69%. The dynamic range for PCE greater than 40% is 22.9 dB, spanning from −35.0 dBm to −12.1 dBm. The input power required to achieve $V_{OUT} = 1$ V is −20.6 dBm, which is a 4 dB improvement compared to the CCDD rectifier.

When the output voltage is 1 V, the proposed LCS-R1 rectifier achieves a peak efficiency of 57.2%, while the PCE of the conventional CCDD rectifier is 24.2%. Although the LCS-R1 exhibits a 7.8% degradation in peak PCE at low input power levels due to the additional two NMOS transistors, its key advantages lie in the extended dynamic range and improved sensitivity. Specifically, the power dynamic range with PCE > 40% is extended by 10.2 dB, and the sensitivity is enhanced by 4.1 dB simultaneously. The wider dynamic range enables the rectifier to provide stable output in complex electromagnetic environments.

The LCS technique demonstrates pronounced advantages under high input power conditions. Although the LCS structure itself incurs power dissipation, its power consumption remains relatively low in the high-power regime. Meanwhile, this technique achieves a net gain in overall
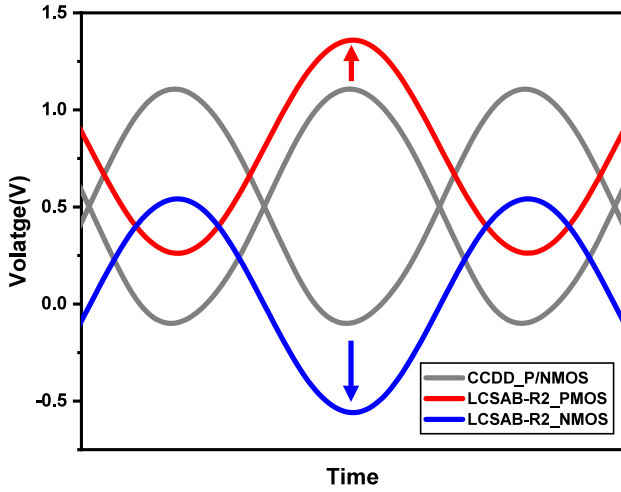
Fig. 14. Transient waveforms of the MOSFET gate voltage in the LCSAB-R2 and CCDD rectifiers at $V_{OUT} = 1$ V.
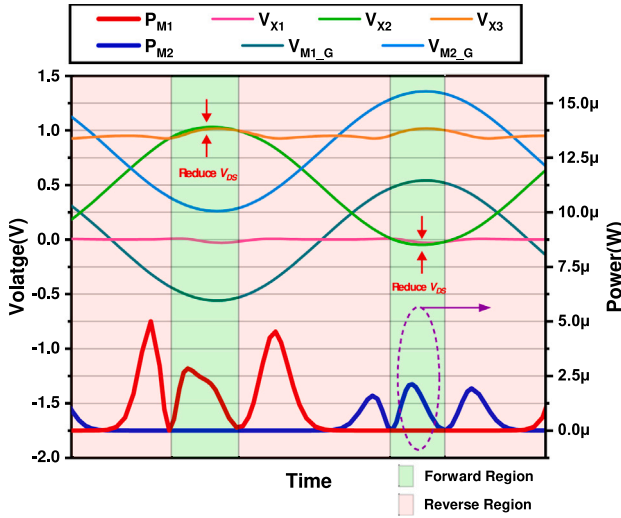

Fig. 15. Transient power consumption of the MOSFET over one operating cycle in the CCDD and LCSAB-R2 rectifiers at $R_L = 200$ kΩ and $V_{OUT} = 1$ V.

Fig. 16. Average power consumption of the MOSFET in the proposed rectifiers and the CCDD rectifier at $V_{OUT} = 1$ V and $R_L = 200$ kΩ.

Fig. 17. Average power consumption in the Leakage-current-suppressing and adaptive-biasing circuits at $V_{OUT} = 1$ V and $R_L = 200$ kΩ.

PCE by dynamically suppressing the power dissipation of the main transmission MOSFETs (M_1-M_4). This characteristic makes LCS-R1 particularly suitable for high-power-density applications.

3.2. Proposed LCSAB-R2

The LCSAB-R2 topology, based on the integration of leakage-current suppression and adaptive-biasing techniques, incorporates gate adaptive-biasing circuits, as shown in Fig. 13.

The integration of adaptive-biasing circuits is primarily aimed at reducing the overdrive voltage of the main transmission MOSFETs (M_1-M_4) under high input power conditions, which in turn suppresses reverse leakage current and minimizes additional power consumption from forward current. To ensure that the gate voltage biasing does not impede the normal operation of the rectifier, capacitors C_3 - C_6 are employed to directly couple the RF signal to the gate of the MOS transistors. Diodes D_1 to D_4 are utilized to furnish DC biasing for the gate voltage, with the notable distinction that the biasing diodes for NMOS(M_1,M_3) and PMOS(M_2,M_4) transistors exhibit opposing orientations. This discrepancy arises from the necessity to diminish the gate voltage for NMOS transistors while elevating it for PMOS transistors
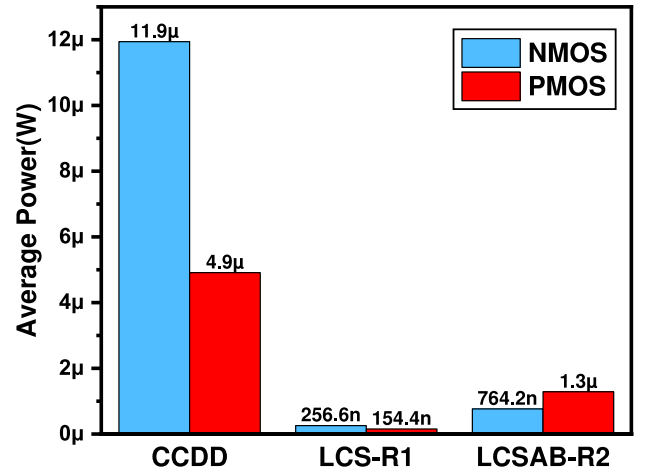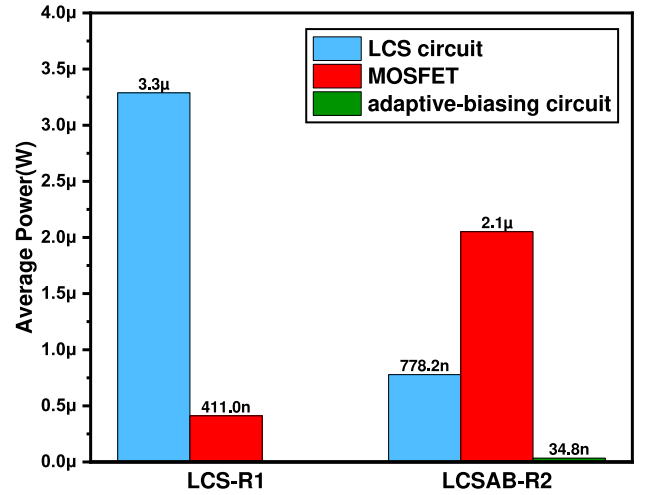
to minimize MOS transistor power consumption under high-power input conditions. Additionally, the adaptive-biasing circuit (D_5, D_6) is integrated into the substrate of the PMOS transistor to reduce its threshold voltage and enhance the sensitivity of the rectifier [15].

With the adaptive-biasing circuit connected to the gates of M_1 to M_4, at low RF power levels, the voltage drop across the diodes is less than the threshold voltage, causing the diodes to behave as open circuits. Consequently, the gate voltages of M_1 to M_4 are effectively directly connected to the RF nodes, reconfiguring the rectifier to a CCDD circuit.

For input power levels in the medium to high range, when the voltage drop across diodes D_1 to D_4 exceeds the threshold voltage, the diodes become forward-biased. In this state, D_2 and D_1, respectively, reduce the gate voltage of M_1 and M_3, while D_4 and D_3, respectively, increase the gate voltage of M_2 and M_4. This results in the superimposition of the RF signal on a DC bias voltage. Fig. 14 compares the transient gate voltages of the CCDD and adaptive-biasing circuits at an output voltage of 1 V. It shows that the NMOS gate voltage in the adaptive-biasing circuit is lower than that in the CCDD rectifier, while the PMOS gate voltage is higher.

In the CCDD rectifier, for the NMOS transistor M_1, the proportion of time within a cycle when the gate–source voltage (V_{GS}) is greater

Table 1
Design parameters of the proposed rectifiers.

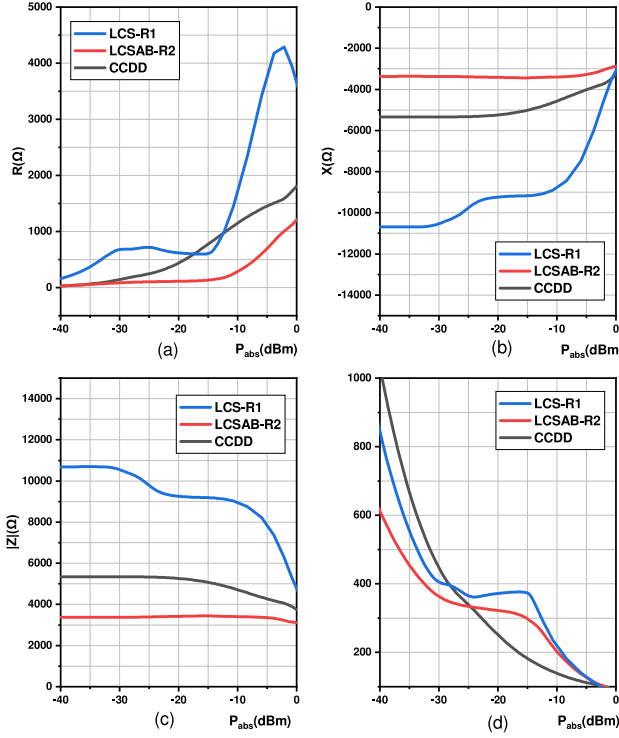| Gate dimensions (μm)	M$_1$	M$_2$	M$_3$	M$_4$	M$_5$-M$_6$	D$_1$-D$_4$	D$_5$-D$_6$
LCS-R1	3/0.04	8/0.04	3/0.04	8/0.04	1.7/1.2	–	–
LCSAB-R2	6/0.04	10/0.04	6/0.04	10/0.04	50/1.2	2.8/2.8	0.5/0.5

Fig. 18. Input impedance characteristics of the rectifiers: (a) input resistance, (b) input reactance, (c) magnitude of the input impedance, and (d) the coefficient K derived from the input impedance.
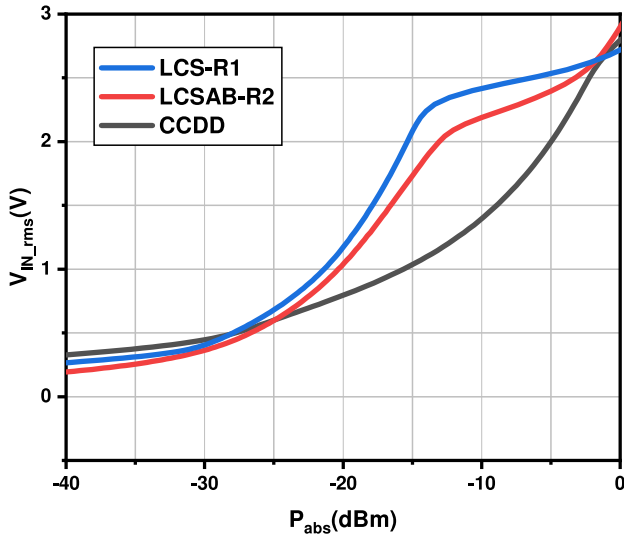

Fig. 19. Simulated input RMS voltage $V_{in,rms}$ versus absorbed power P_{abs}.

Fig. 20. (a) Simulated output voltage V_{out} versus absorbed power P_{abs}. (b) Simulated voltage conversion efficiency (VCE) versus P_{abs}.

power conditions, a very short conduction time is sufficient to provide adequate forward current to the load. Therefore, reducing the forward conduction time of the MOS transistor within a cycle can significantly minimize additional forward power consumption. This phenomenon is one of the reasons why the PCE of the traditional CCDD rectifier decreases under high power input conditions. For the PMOS transistor, the increased gate voltage due to the adaptive-biasing circuits also shortens its conduction time within a cycle. The adaptive-biasing circuits dynamically adjusts the gate voltage of the MOS transistor based on the current output voltage, thereby controlling the conduction time of the MOS transistor within an optimal range. This adjustment not only suppresses the reverse leakage current but also reduces the power consumption of the forward current.

Fig. 15 shows the internal node voltages and MOSFET power consumption of the LCSAB-R2 during operation. As shown in the figure, the LCS technique effectively reduces the V_{DS} of the main MOSFETs, while the adaptive-biasing technique enables dynamic gate voltage adjustment beyond the LCS-R1 architecture. This dual-optimization strategy achieves a higher PCE and extends the power dynamic range.

Fig. 16 presents the simulated average power consumption of the main transmission MOSFETs in the three rectifier architectures at $V_{OUT} = 1$ V. Comparative analysis confirms that the LCS technique significantly reduces the power consumption of the main MOSFETs, from 16.8 μW in the CCDD rectifier to 0.411 μW in the LCS-R1. Fig. 16 presents the simulated average power consumption of the main transmission MOSFETs in the three rectifier architectures at $V_{OUT} = 1$ V.

It is noted that the power consumption of MOS transistors in LCS-R1 is lower than that of the LCSAB-R2. However, its PCE is still lower than that of the LCSAB-R2. Fig. 17 compares the components of power consumption between the LCS-R1 and LCSAB-R2. The figure indicates that the addition of adaptive-biasing circuits significantly reduces the power consumption of the LCS circuit itself. Moreover, the power consumption of the adaptive-biasing circuits is negligible, resulting in a higher overall PCE for the LCSAB-R2 compared to the LCS-R1.

The LCSAB-R2 improves upon LCS-R1 by modifying the main rectifier architecture, demonstrating that the LCS technique can be reused in other advanced rectifiers to enhance dynamic range. Although LCS may introduce additional power consumption, future work could explore enabling the LCS structure only when needed — e.g., based on input power detection — to avoid unnecessary overhead.

Table 1 summarizes the gate dimensions (width-to-length ratios) of the transistors and diodes.

than zero is 50%. However, with the adoption of the adaptive-biasing technique, the gate voltage is superimposed with a negative DC voltage, resulting in a V_{GS} greater than zero for less than 50% of the time. The reduction in the proportion of time during which $V_{GS} > 0$ directly corresponds to a shorter forward conduction period for M$_1$. Under high input
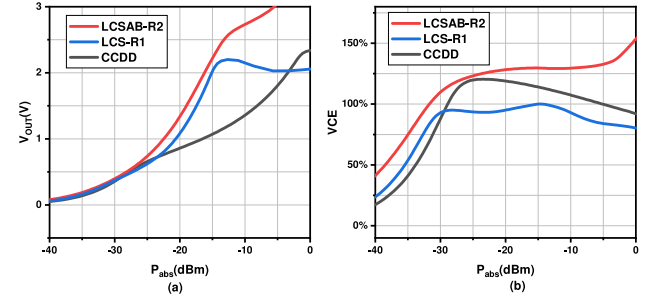
Fig. 21. Simulated PCE versus P_{abs} for LCS-R1, LCSAB-R2, and CCDD at $f = 433\,\text{MHz}$ and $R_L = 200\,\text{k}\Omega$.

3.3. Simulation results

To evaluate the rectifier's true performance, an ideal matching network is employed in this work. Under the same actual received power P_{abs}, the input voltage V_{in} is determined by the rectifier's input impedance. Based on the relation

$$P_{abs} = I_{in,rms}^2 R, \tag{7}$$

where $I_{in,rms} = V_{in,rms}/|Z|$, we rearrange to obtain

$$V_{in,rms} = \sqrt{P_{abs} \cdot \frac{|Z|^2}{R}}. \tag{8}$$

To quantify the impact of impedance on the input voltage, we define an empirical coefficient:

$$K = \sqrt{\frac{|Z|^2}{R}}, \tag{9}$$

so that

$$V_{in,rms} = \sqrt{P_{abs}} \cdot K. \tag{10}$$

The post-layout input impedance $Z = R + jX$ of the rectifier is extracted via large-signal impedance analysis using harmonic balance (HB) simulation. The simulation results are shown in Fig. 18.

The calculated empirical coefficient K is shown in Fig. 18(d). For $P_{abs} > -25\,\text{dBm}$, the K-values of the LCS-R1 and LCSAB-R2 rectifiers exceed that of the CCDD rectifier. Since $V_{in,rms}$ is proportional to K, the input RMS voltages of the LCS-R1 and LCSAB-R2 rectifiers are correspondingly higher than that of the CCDD rectifier under the same P_{abs}. The simulated $V_{in,rms}$ results are presented in Fig. 19.

The ability of a rectifier to convert input voltage into output voltage can be quantified by the voltage conversion efficiency (VCE) [16], defined as:

$$\text{VCE} = \frac{V_{out}}{V_{in,rms}}. \tag{11}$$

The simulated VCE and output voltage V_{out} of the proposed rectifiers are shown in Fig. 20. The LCSAB-R2 achieves a higher VCE than the LCS-R1, which implies that it can deliver a larger V_{out} even when its $V_{in,rms}$ is smaller than that of the LCS-R1.

Fig. 22. Load-dependent PCE versus P_{abs} under varying load conditions ($R_L = 20\,\text{k}\Omega$ to $300\,\text{k}\Omega$).
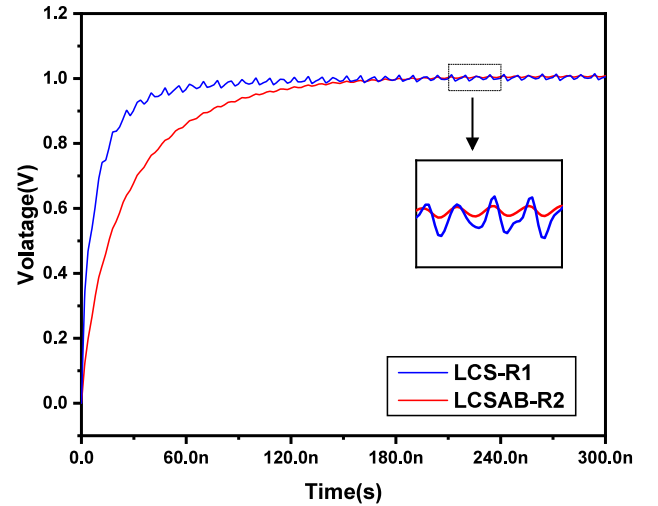

Fig. 23. Transient output voltage waveforms for the proposed rectifiers with $V_{out} = 1\,\text{V}$.

The power conversion efficiency is defined as:
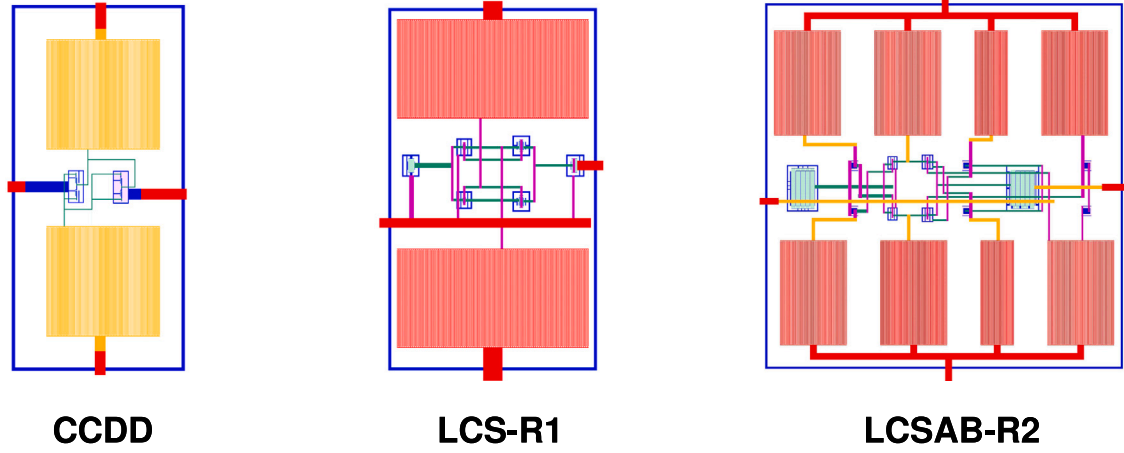
$$\text{PCE} = \frac{P_{out}}{P_{abs}} \times 100\% \tag{12}$$

Fig. 24. Layouts of the three rectifiers in 40 nm CMOS technology. Active areas: LCSAB-R2 (0.12 mm^2), LCS-R1 (0.09 mm^2), CCDD (0.07 mm^2).

Table 2
Comparison with state-of-the-art works.

Ref.	Topology	Technology	Frequency	Load resistance	Peak PCE (%)	Dynamic range (dBm)@PCE>40%	Sensitivity (dBm)@1V
	LCSAB				89.4 @ −19.7 dBm	−38.0 to −10.3	−22.5
This work	LCS	40 nm	433 MHz	200 kΩ	69 @ −29.3 dBm	−35.0 to −12.1	−20.6
	CCDD				76.8 @-27.2 dBm	−33.3 to −20.6	−16.5
[19]'2025	Dynamically biased	65 nm	915 MHz	7 kΩ	80[a,b] @ 0 dBm	−17 to 6[a,b]	−7 @7 kΩ[a,b]
[20]'2025	Dual Gate & Body Self-Biasing	180 nm	920 MHz	100 kΩ	78.5[b] @ −18.7 dBm	−28.5 to −12[a,b]	−18.9 @100 kΩ[b]
[21]'2024	1-stage CCLC	65 nm	2.4 GHz	500 Ω	70[a,b] @ 0 dBm	−7.5 to 10[a]	−3 @1 MΩ
[22]'2023	ALL-NMOS	180 nm	200 MHz	10 kΩ	57.6 @ −13.78 dBm	−17 to −8[a]	−14.8 @1 MΩ
[14]'2023	Advanced topology amalgamation	65 nm	900 MHz	100 kΩ	79.77 @ −17.5 dBm	−23 to −10[a]	−15.5 @100 kΩ
[23]'2023	Dual-Topology	130 nm	900 MHz	100 kΩ	89[a,b] @ −16 dBm	−20 to −5[a,b]	−17.7 @∞Ω
[24]'2022	DDCCB	130 nm	953 MHz	50 kΩ	75.7[b] @ −11 dBm	−14 to −3[a,b]	−14 @50 kΩ[a,b]
[25]'2021	ICC	130 nm	900 MHz	100 kΩ	80.3 @ −17 dBm	−22.5 to −8	−18.7 @100 kΩ
[26]'2020	DM	65 nm	433 MHz	100 kΩ	86 @ −20 dBm	−35 to −14[a]	−19.2 @100 kΩ
[27]'2018	DTMOS CCDD	130 nm	915 MHz	300 kΩ	81.55[b] @ −32 dBm	−36.8 to −22.2[a,b]	–

[a] Estimated from the figure.
[b] Simulation results are reproduced in this work.

where P_{out} is the DC output power and P_{abs} denotes the absorbed RF power.

Power dynamic range (PDR) is another important performance metric for rectifiers. The PDR, characterizing the operational power window with PCE above a specified threshold (e.g., 40 % or 80 % of peak PCE) [17,18]. Mathematically, it is expressed as:

$$PDR (dB) = P_{max} (dBm) − P_{min} (dBm) \quad (13)$$

where P_{max} and P_{min} represent the maximum and minimum input power levels, respectively, at which the rectifier sustains PCE above the designated threshold value.

Fig. 21 shows both pre- and post-layout PCE results for the three circuits, simulated at 433 MHz with a 200 kΩ load. The reported performance metrics correspond to post-layout simulations. The proposed LCSAB-R2 achieves a peak PCE of 89.4% at P_{abs} = −19.7 dBm, with a power dynamic range (PDR) — defined as the input power range over which PCE exceeds 40% — of 27.7 dB, which is 15 dB wider than that of the CCDD rectifier. The proposed LCS-R1 achieves a peak PCE of 69% and a PDR of 22.9 dB under the same criterion.

The performance of the rectifiers varies with different load conditions, as illustrated in Fig. 22. This evaluation tests the proposed rectifiers (LCS-R1 and LCSAB-R2) across a load range of 20 kΩ to 300 kΩ. The LCS-R1 rectifier achieves a peak PCE of 71.9% at a load resistance of 300 kΩ. The LCSAB-R2 rectifier demonstrates its best performance at 200 kΩ. The peak PCE of LCSAB-R2 shows minimal dependence on load variation, with only a 10.3% efficiency fluctuation across the tested load range. Although the PCE of LCS-R1 shows

greater variation across load resistances, it maintains a relatively high efficiency at higher load resistance values.

Fig. 23 shows the output voltage waveforms of the proposed rectifiers (LCS-R1 and LCSAB-R2) when V_{out} = 1 V. The LCS-R1 reaches steady state faster than the LCSAB-R2, while the LCSAB-R2 exhibits a smaller voltage ripple. Fig. 24 shows the layout of the three circuits, designed using a TSMC 40 nm CMOS process.

To fairly quantify the trade-off between PCE and the operational input power range, we define a figure of merit (FoM) as:

$$FoM = Peak PCE × PDR \quad (14)$$

where Peak PCE denotes the maximum power conversion efficiency (expressed in %), and PDR (power dynamic range) represents the input power span (in dB) over which the PCE exceeds 40%. As shown in Fig. 25, the proposed LCSAB-R2 rectifier achieves the highest FoM among all compared designs. To ensure a fair comparison, the DR and PCE data for all reference works are extracted directly from the original figures in their respective publications and re-evaluated using the same criterion of PCE > 40%. Superimposed on the plot are iso-FoM contours (FoM = 5, 10, 15, 20, 25), which clearly highlight the performance advantage of the proposed scheme.

Table 2 presents a summary and comparison of the proposed rectifiers against state-of-the-art CMOS rectifiers. To ensure a fair comparison, simulation results from the original studies are included in the table when available. The table includes several works focused on extending the dynamic range of CMOS rectifiers [14,20–23,25].
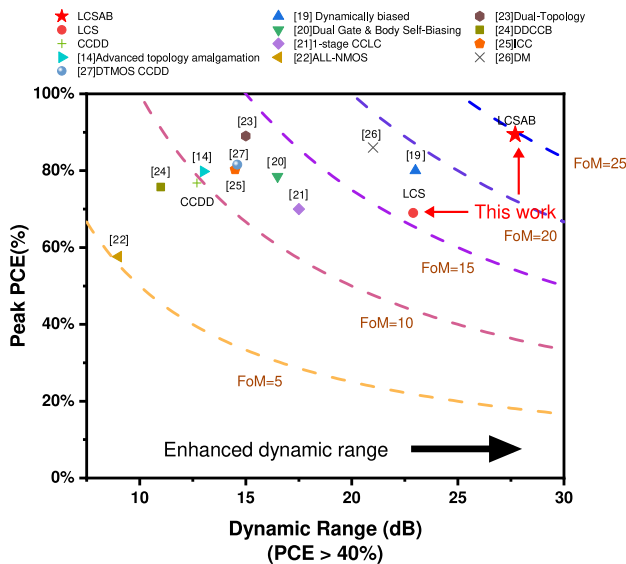
Fig. 25. Peak PCE vs dynamic range for state-of-the-art RF rectifiers, with iso-FoM contours.

This work is designed for operation at 433 MHz, which is a globally available frequency for RF energy harvesting applications, similar to 900 MHz [28]. Although the rectifier proposed in [23] achieves a peak PCE of 89%, its high efficiency is limited to low input power levels, whereas the LCSAB-R2 maintains a high PCE across the entire dynamic range. The proposed LCSAB-R2 achieves a higher peak PCE than those reported in other studies, while both LCS-R1 and LCSAB-R2 demonstrate improved PDR over existing designs.

4. Conclusion

This article presents a leakage-current-suppression (LCS) technique to improve power conversion efficiency (PCE) by effectively mitigating reverse leakage current and power dissipation in rectifying transistors. The implementation methodology of the proposed technique is also discussed in detail. For validation, two rectifiers (designated as LCS-R1 and LCSAB-R2) were implemented using a TSMC 40 nm CMOS process. The LCSAB-R2 incorporates additional gate adaptive biasing and dynamic substrate biasing techniques to extend its input power dynamic range (PDR). Post-simulation results show that both proposed rectifiers achieve wide power dynamic ranges. Specifically, LCS-R1 and LCSAB-R2 achieve dynamic ranges of 22.9 dB and 27.7 dB, respectively, representing substantial improvements over conventional CCDD rectifiers.

CRediT authorship contribution statement

Di Luo: Writing – original draft, Methodology, Investigation, Formal analysis. **Jian Liu:** Writing – review & editing, Investigation, Funding acquisition. **Kang Zeng:** Writing – original draft, Validation. **Rui Wang:** Writing – original draft, Data curation. **Meijing Wang:** Writing – original draft, Investigation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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