

Gate charging

- Bypass capacitor charge is around 26uC

- Gate charge of MOSFET is around 0.2uC Bootstrap circuit
- Inrush current is around 1.7A
- Time constant is 2.2us 200V 12V 2EDB8259Y - UVLO of 8V - 14-SOP package D2
•VH D\_Schottky 10 3٧3 200V U1 ▼ D1 D Q1 2EDB8259Y NMOS CHHD-INA VDDA 2 INB 560k CHLD-OUTA 3 VDDI GNDA 14 4 GNDI C14 C15 5 DIS DISD 1 u 6 DTC 7 N.C. VDDI VDDB D3 D\_Schottky OUTB GNDB 9 R3 100pF 100pF \_ C13 2.2u **÷** Q2 GND  $\rightarrow$ NMOS ISOGND R10 560k GND Shoot—through Protection (STP) and Dead—Time Control (DTC)
If STP/DTC is high or left open, OUTA and OUTB can overlap (SPT and DTC disabled)
If STP/DTC is connected to GNDI with a resistance RDTC, OUTA and OUTB cannot overlap and a "safe dead—time" can be configured: tdt [ns] = 10 x RDTC [k $\Omega$ ]
If STP/DTC is connected to GNDI, OUTA and OUTB cannot overlap (STP only enabled) Sheet: /legA/ File: phaseleg.kicad\_sch Title: Half bridge leg Size: A4 Date: 2025-08-07 Rev: KiCad E.D.A. 9.0.3 ld: 2/5

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•VH D\_Schottky R12 10 3٧3 200V U2 Q3 D4 2EDB8259Y NMOS CHHD-INA VDDA R17 2 INB 560k CHLD-OUTA 15 3 VDDI GNDA 14 C20 4 GNDI C22 C23 5 DIS DISD 1 u 6 DTC 7 N.C. VDDI VDDB C16 C17 C18 D6 D\_Schottky OUTB GNDB 9 R11 100pF 100pF \_ C21 2.2u **÷** GND  $\rightarrow$ NMOS ISOGND R18 560k GND Shoot—through Protection (STP) and Dead—Time Control (DTC)
If STP/DTC is high or left open, OUTA and OUTB can overlap (SPT and DTC disabled)
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