Instr	Op$_{5:0}$	RegWrite	RegDst	AluSrc	Branch	MemWrite	MemtoReg	ALUControl$_{2:0}$	Jump	index2adr	jal
R-type	000000	1	~~1~~ 0	0	0	0	0	Diff.	0	0	0
lw	100011	1	~~0~~ 0	1	0	0	1	010(add)	0	0	0
sw	101011	0	X	1	0	1	X	010(add)	0	0	0
beq	000100	0	X	0	1	0	X	110(sub)	0	0	X
j	000010	0	X	X	X	0	X	XXX	1	X	X
addi	001000	1	0	1	0	0	0	010(add)	0	0	0
index2Adr	000000	1	01	0	0	0	0	010(add)	0	1	0
jal	000011	1	10	X	X	0	X	XXX	1	X	1

index2adr   R[rd] = R[rs]*4 + R[rt]

jal   R[$ra] = PC + 4, PC = JTA

MIPS single-cycle processor datapath diagram with handwritten annotations.

Labels visible in the diagram:

- Jump
- Control Unit
- MemtoReg
- MemWrite
- Branch
- ALUControl$_{5:0}$
- ALUSrc
- Op
- Funct
- RegDst
- RegWrite
- val (handwritten, blue)
- index2Adr (handwritten, red)
- shamt
- CLK
- PC'
- PC
- Instruction Memory (A, RD, Instr)
- PCJump
- PCPlus4
- 4
- Register File (WE3, A1, A2, A3, WD3, RD1, RD2)
- SrcA
- SrcB
- ALU
- Zero
- ALUResult
- WriteData
- Data Memory (CLK, WE, A, RD, WD, ReadData)
- Result
- PCSrc
- Sign Extend
- SignImm
- <<2
- PCBranch
- Write Reg$_{4:0}$
- 31:26
- 5:0
- 25:21
- 20:16
- 15:11
- 15:0
- 27:0
- 31:28
- 25:0