

S7CAS-PLEIDES-CARTE-MERE_P06**S7APP1-2****P-06*****Revision 1.00******Date : 2026-01-21***

Revision history	

Package size conversion	
Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

Project Title			
S7CAS-PLEIDES-CARTE-MERE_P06			
Global Project			
S7APP1-2			
Size 11x17	Group P-06	Revision 1.00	
Date 2026-01-21		Sheet 1	of 18
Filename S7CAS-PLEIDES-CARTE-MERE_P06_TITLE.SchDoc			Designers Étienne Provencher Antoine Allard

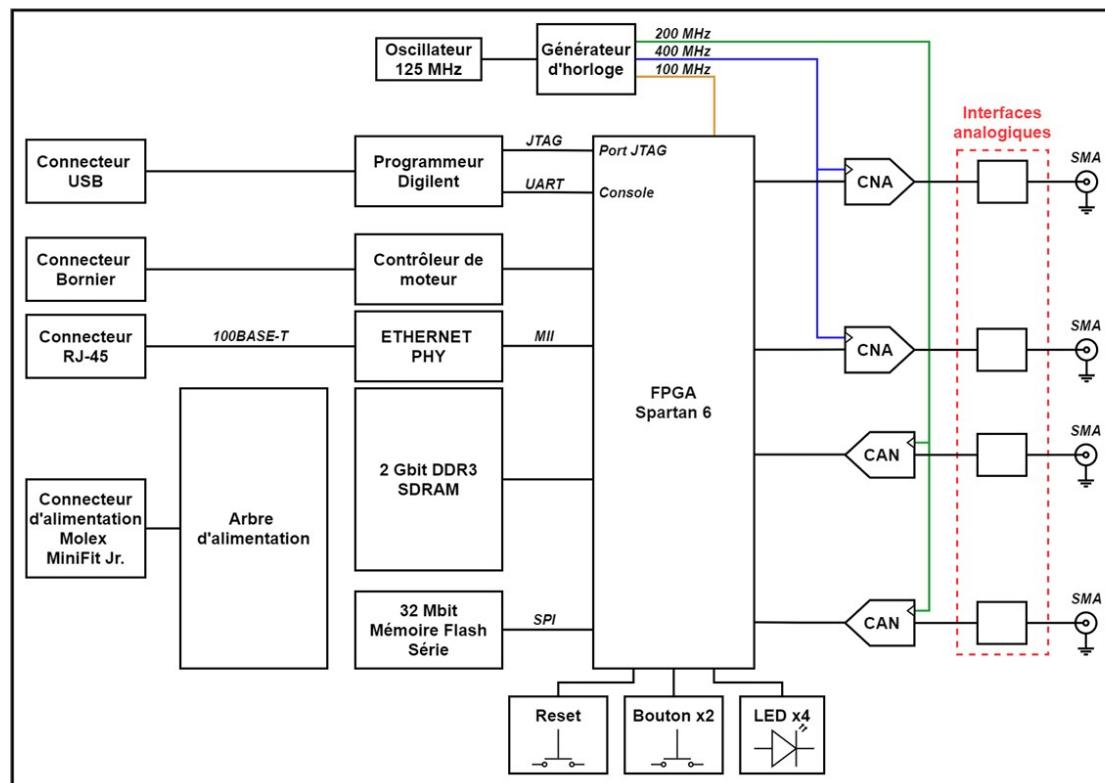


Figure 2 : Diagramme fonctionnel de la carte *Pléïades*

BLOCK DIAGRAM			
Sheet Name	S7CAS-PLEIDES-CARTE-MERE_P06		
Project Title	S7APP1-2		
Size 11x17	Group P-06	Revision 1.00	
Date 2026-01-21	Sheet 2 of 18		
Filename S7CAS-PLEIDES-CARTE-MERE_P06_BLOCK_DIAGRAM.SchDoc	Designers Étienne Provencher Antoine Allard		

24V External PSU or Battery	
V 24 V	I 4.73 A
P 113.52 W	

LMZ23605TZE 1	
SWR	eff : 87 %
Max current : 5A	
Vin 24V	Vout 5.81V
lin 0.92A	lout 3.32A
Pin 22.17W	Pdis 2.88W
Pout 19.29W	

PTN04050AAZT 1	
SWR	eff : 61 %
Max current : 1A	
Vin 5.81V	Vout -5.5V
lin 0.084A	lout 0.056A
Pin 0.49W	Pdis 0.19W
Pout 0.3W	

TPS7A3301RGWR 2	
LDO	eff : 94 %
Max current : 1A	
Vin 5.81V	Vout -5V
lin 0.056A	lout 0.056A
Pin 0.30 W	Pdis 0.02W
Pout 0.28W	

PTH08T241WAZ 1	
SWR	eff : 92 %
Max current : 10A	
Vin 5.81V	Vout 3.6V
lin 2.37A	lout 3.52A
Pin 13.78W	Pdis 1.1W
Pout 12.68W	

NCP59744MN1ADJ 2	
LDO	eff : 92 %
Max current : 3A	
Vin 3.6V	Vout 3.6V
lin 1.436A	lout 1.436A
Pin 5.25W	Pdis 0.43W
Pout 4.74W	

NCP59744MN1ADJ 1	
LDO	eff : 92 %
Max current : 3A	
Vin 3.6V	Vout 3.3V
lin 0.025A	lout 0.025A
Pin 0.091W	Pdis 0.008W
Pout 0.083W	

NCP59744MN1ADJ 2	
LDO	eff : 92 %
Max current : 3A	
Vin 3.6V	Vout 3.3V
lin 0.585A	lout 0.585A
Pin 2.11W	Pdis 0.18W
Pout 1.93W	

NCP59744MN1ADJ 2	
LDO	eff : 50 %
Max current : 3A	
Vin 3.6V	Vout 1.8V
lin 0.566A	lout 0.566A
Pin 2.04W	Pdis 1.02W
Pout 1.02W	

NCP59744MN1ADJ 2	
LDO	eff : 42 %
Max current : 3A	
Vin 3.6V	Vout 1.5V
lin 0.482A	lout 0.482A
Pin 1.73W	Pdis 1.01W
Pout 0.72W	

MAX15027ATB+T 2	
LDO	eff : 21 %
Max current : 1A	
Vin 3.6V	Vout 0.75V
lin 0.429A	lout 0.429A
Pin 1.543W	Pdis 1.223W
Pout 0.32W	

A

-Sequence :
-Flash
-Autre

Total Global Power Tree Efficiency :
 $104.41 / 113.52 = 92\%$

Regulated global Power Tree Efficiency :
 $12.97 / 22.08 = 58.7\%$

D

1

LMZ23605TZE 1

SWR	eff : 71 %
Max current : 5A	
Vin 5.81V	Vout 1.2V
lin 0.87A	lout 3A
Pin 5.07W	Pdis 1.47W
Pout 3.6W	

2

3

4

5

6

2

3

4

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6

24V

V 24 V	I 3.810 A
P 91.44 W	

-5V

V -5 V	I 0.056 A
P 0.28 W	

5V

V 5 V	I 0.056 A
P 0.28 W	

3V3D

V 3.3 V	I 1.436 A
P 4.74 W	

3V3FLASH

V 3.3 V	I 0.025 A
P 0.083 W	

3V3A

V 3.3 V	I 0.585 A
P 1.93 W	

1V8D

V 1.8 V	I 0.566 A
P 1.02 W	

1V5D

V 1.5 V	I 0.482 A
P 0.72 W	

VTTDDR (0.75V)

V 0.75 V	I 0.429 A
P 0.32 W	

1V2D

V 1.2 V	I 3 A
P 3.6 W	

A

B

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D

E

F

G

H

Sheet Name	
POWER TREE	
Project Title	
Size	Group
11x17	P-06
Date	Sheet
2026-01-21	3 of 18
Filename	Designers
S7CAS-PLEIADES-CARTE-MERE_P06_POWER_TREE.SchDoc	Étienne Provencher Antoine Allard

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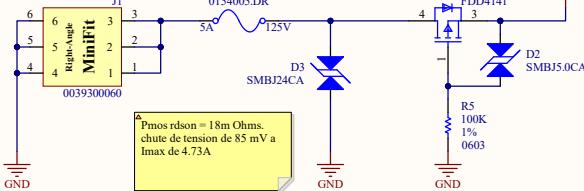
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Y

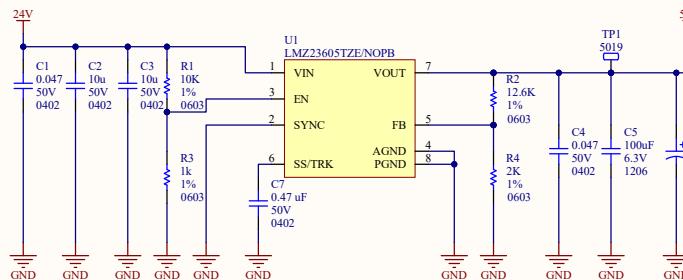
Z

A

B

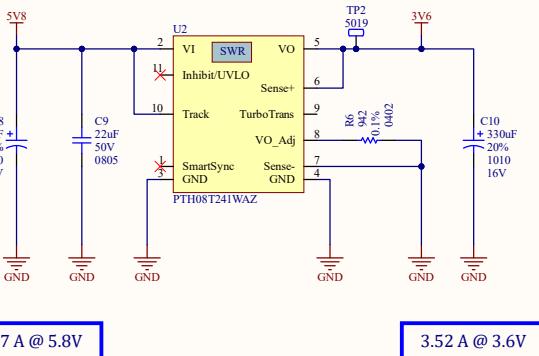
Power input & Protections

4.73 A @ 24V

Bucks 24V à 5.8V

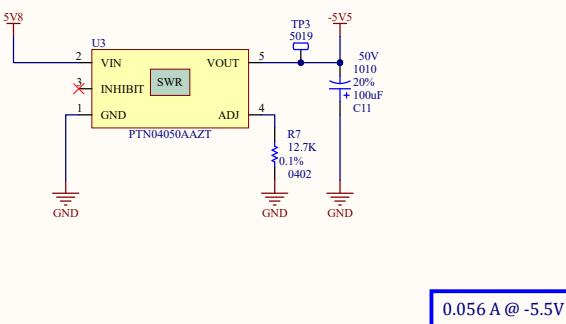
0.92 A @ 24V

3.39 A @ 5.81V

Bucks 5.8 à 3.6

2.37 A @ 5.8V

3.52 A @ 3.6V

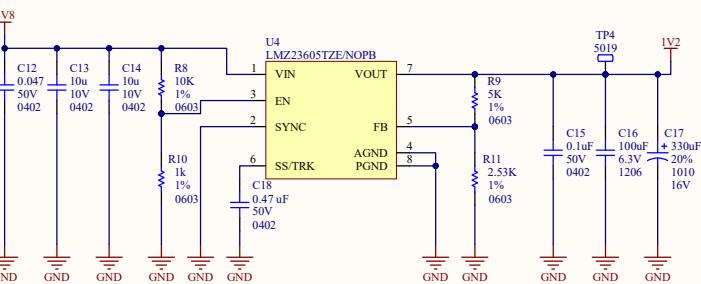
Bucks 5.8 à -5.5

0.084 A @ 5.8V

0.056 A @ -5.5V

Power table

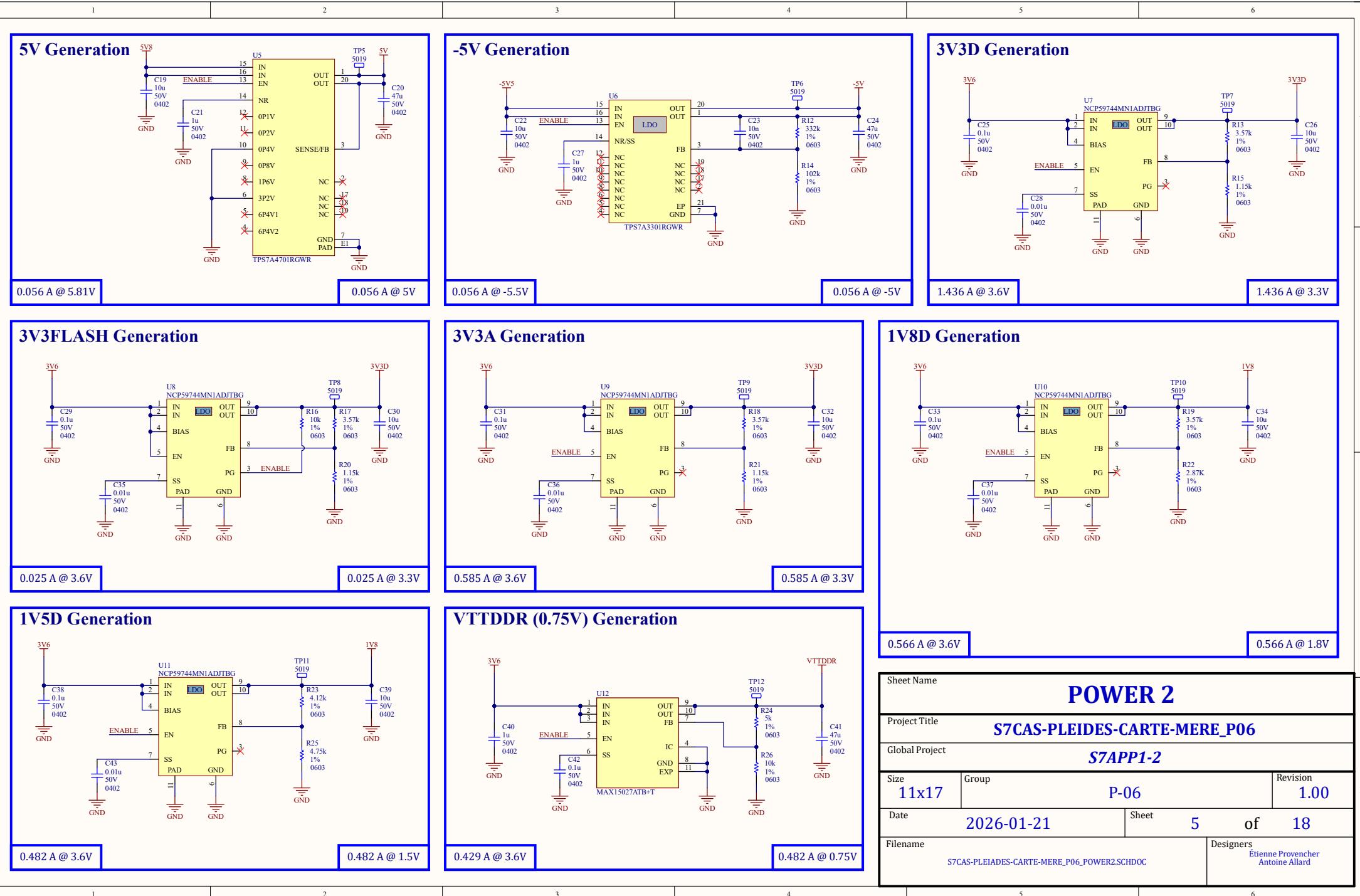
Sheet	Current @ 24V	Current @ 5V	Current @ -5V	Current @ 3V3D	Current @ 3V3FLASH	Current @ 3V3A	Current @ 1V8D	Current @ 1V8D	Current @ 1V2D	Current @ VTTDDR (0.75V)
FPGA1	0 mA	0 mA	0 mA	0.1 A	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FPGA2	0 mA	0 mA	0 mA	0.05 A	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FPGA3	0 mA	0 mA	0 mA	0.15 A	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FPGA4	0 mA	0 mA	0 mA	0.25 A	0 mA	0 mA	0 mA	0 mA	3 A	0 mA
CLOCK	0 mA	0 mA	0 mA	690 mA	0 mA	175 mA	0 mA	0 mA	0 mA	0 mA
ETHERNET	0 mA	0 mA	0 mA	28 mA	0 mA	34 mA	0 mA	0 mA	0 mA	0 mA
DDR3	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	182 mA	0 mA	429 mA
MISC	10 mA	0 mA	0 mA	42 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
MOTOR	3.8 A	0 mA	0 mA	4 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FLASH	0 mA	0 mA	0 mA	0 mA	0 mA	25 mA	0 mA	0 mA	0 mA	0 mA
ADC	0 mA	43.2 mA	43.2 mA	0 mA	0 mA	320 mA	165 mA	0 mA	0 mA	0 mA
DAC	0 mA	13.3 mA	13.3 mA	0 mA	0 mA	56 mA	401 mA	0 mA	0 mA	0 mA
USB_PROG	0 mA	0 mA	0 mA	122 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
Total	3.810 A	0.056 A	0.056 A	1.436 A	0.025 A	0.585 A	0.566 A	0.482 A	3.000 A	0.429 A

Bucks 5.8V à 1.2V

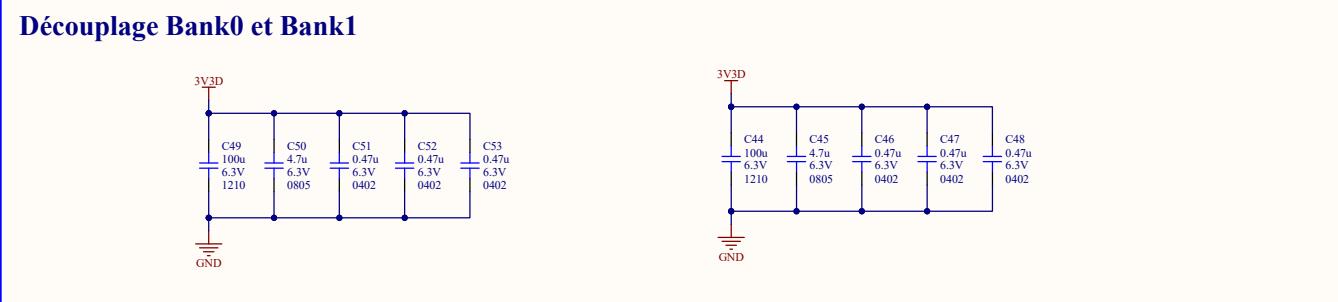
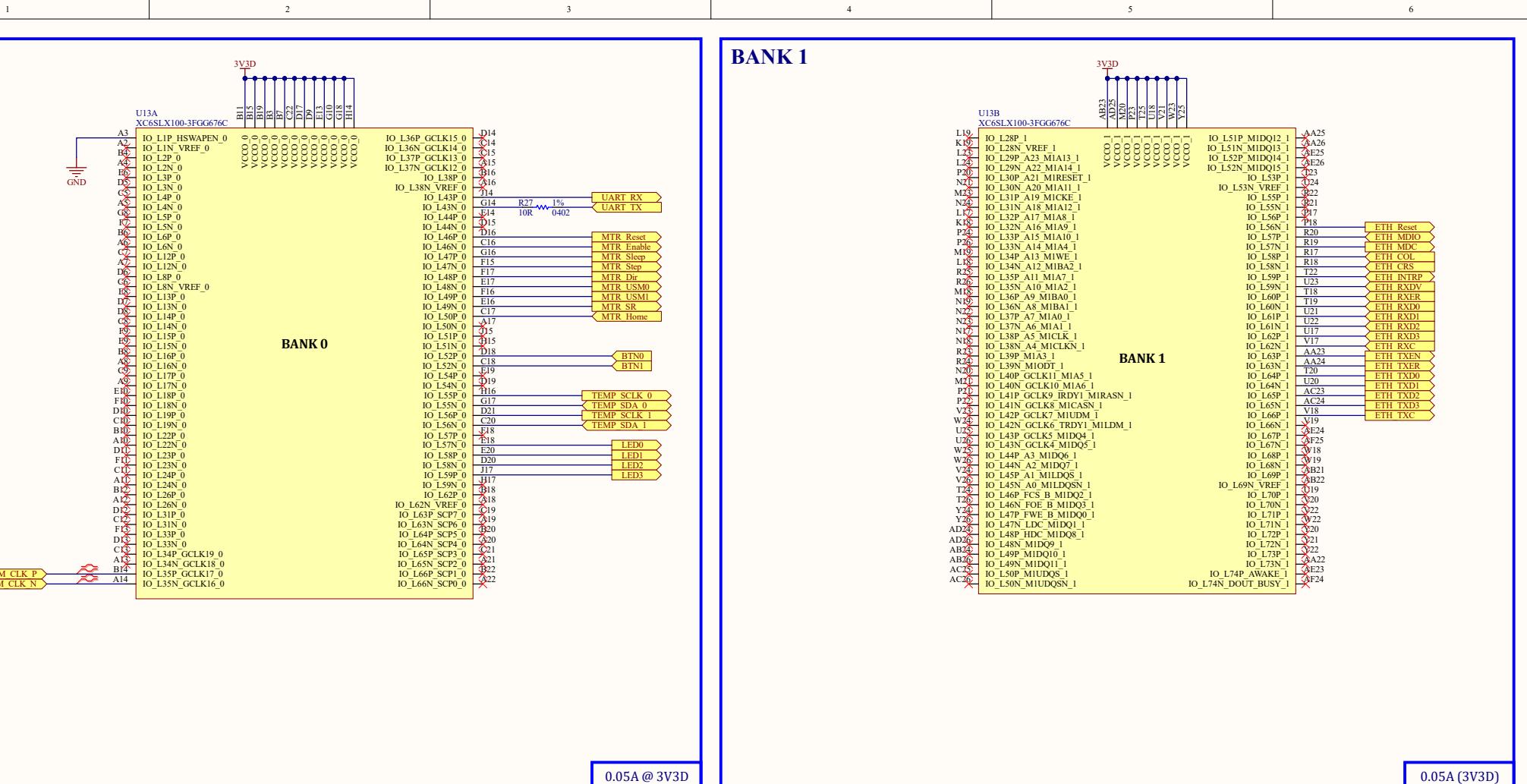
0.87 A @ 5.8V

3 A @ 1.2V

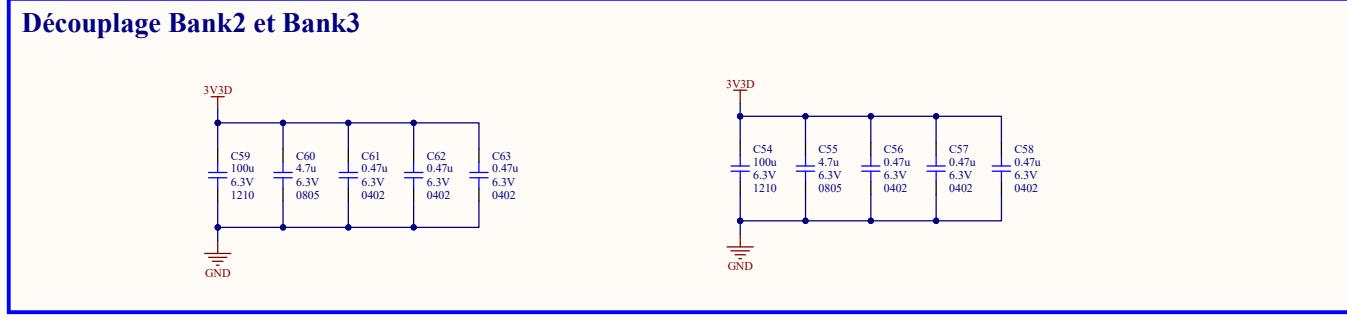
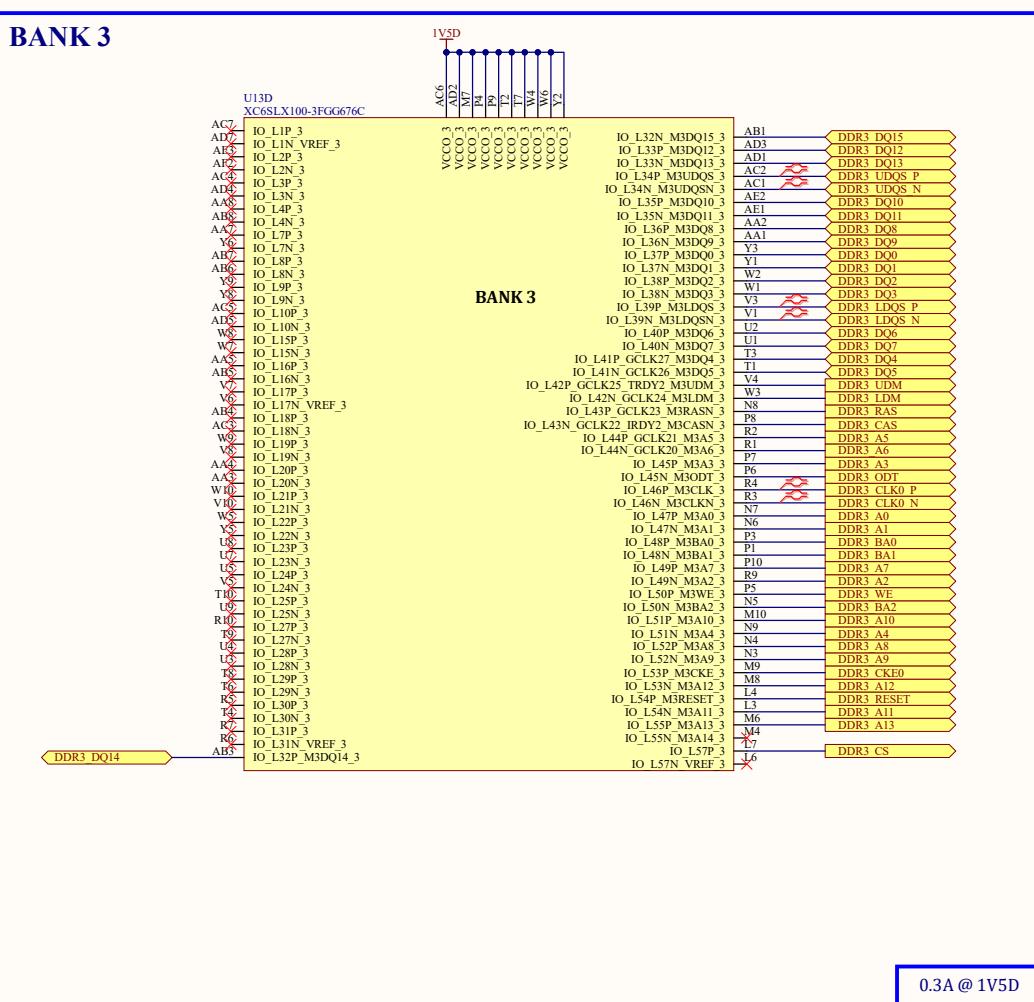
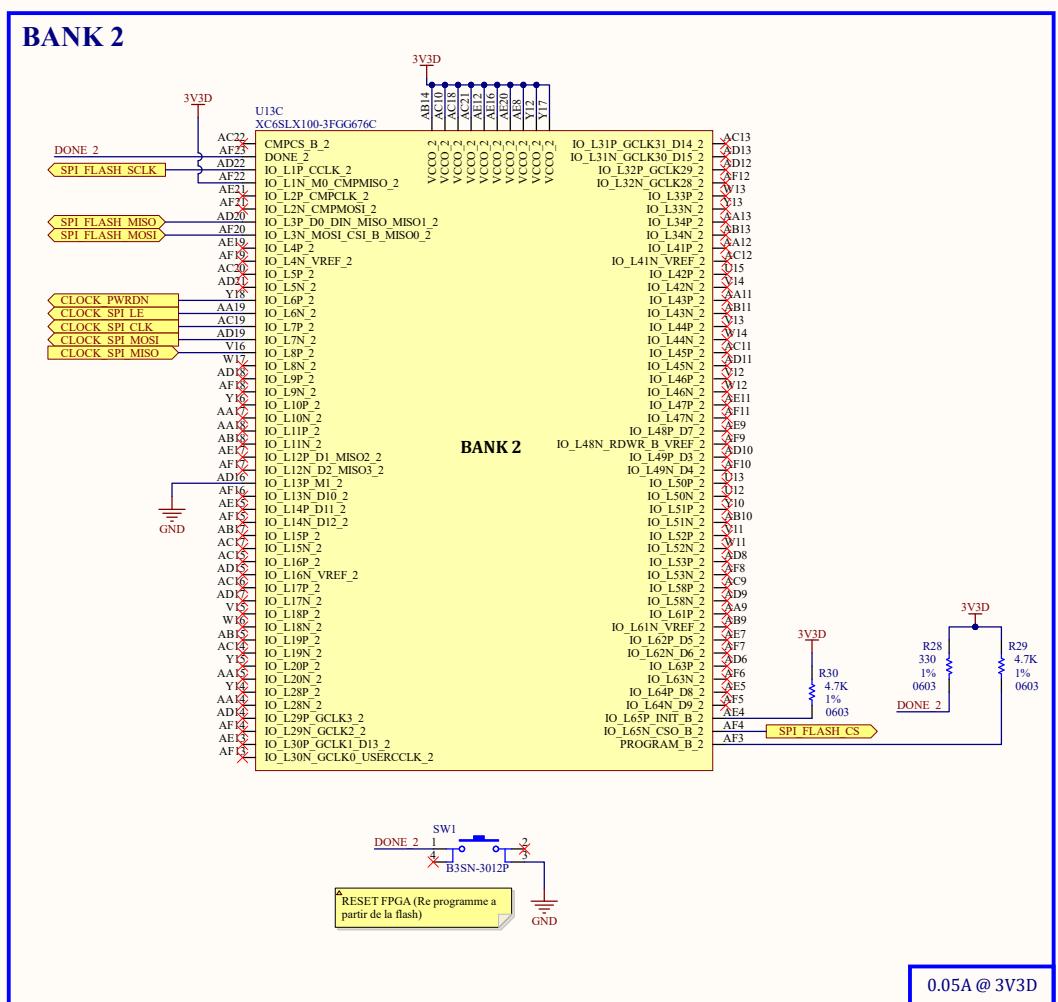
POWER 1Project Title **S7CAS-PLEIDES-CARTE-MERE_P06**Global Project **S7APP1-2**Size **11x17** Group **P-06** Revision **1.00**Date **2026-01-21** Sheet **4** of **18**Filename **S7CAS-PLEIDES-CARTE-MERE_P06_POWER1.SCHDOC** Designers **Étienne Provencher
Antoine Allard**



Sheet Name	POWER 2		
Project Title	S7CAS-PLEIDES-CARTE-MERE_P06		
Global Project	S7APP1-2		
Size	11x17	Group	P-06
Revision	1.00		
Date	2026-01-21		
Sheet	5	of	18
Filename	S7CAS-PLEIDES-CARTE-MERE_P06_POWER2.SCHDOC		
Designers	Étienne Provencher Antoine Allard		

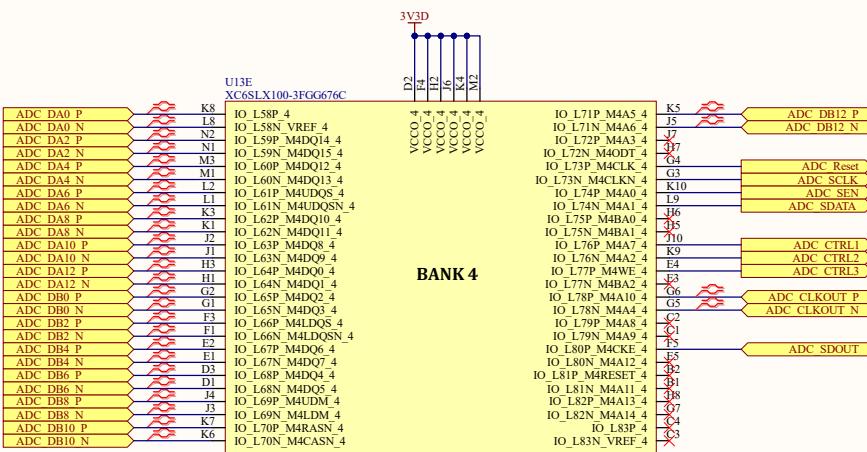


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Project Title	S7CAS-PLEIDES-CARTE-MERE_P06		
Global Project	S7APP1-2		
Size 11x17	Group P-06	Revision 1.00	
Date 2026-01-21	Sheet 6	of 18	
Filename S7CAS-PLEIADES-CARTE-MERE_P06_FPGA1.SCHDOC	Designers Étienne Provencher Antoine Allard		



Sheet Name			
FPGA2			
Project Title	S7CAS-PLEIDES-CARTE-MERE_P06		
Global Project	S7APP1-2		
Size 11x17	Group	P-06	Revision 1.00
Date 2026-01-21	Sheet	7	of 18
Filename S7CAS-PLEIDES-CARTE-MERE_P06_FPGA2.SCHDOC		Designers Étienne Provencher Antoine Allard	

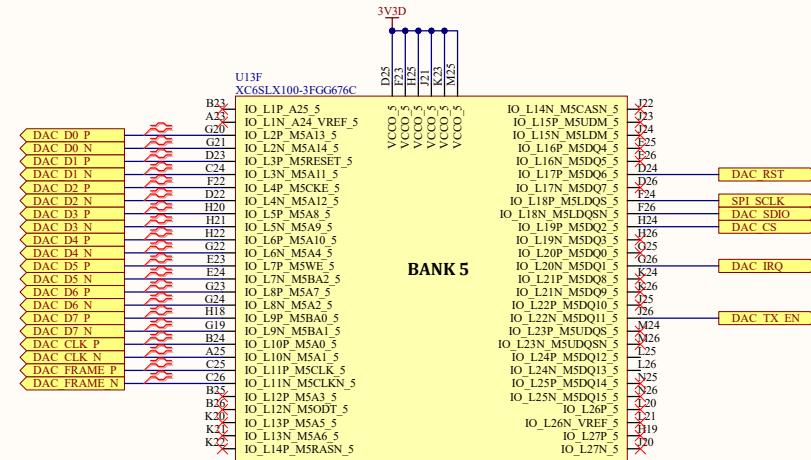
BANK 4



BANK 4

0.1A @ 3V3

BANK 5



BANK

0.05A @ 3V3

Découplage Bank4 et Bank5



Sheet Nam

FPGA3

S7CAS-PLEIDES-CARTE-MERE P06

Global Project

S7APP1-2

Size

11x17 P-06 1.00

P-06 | 1.00

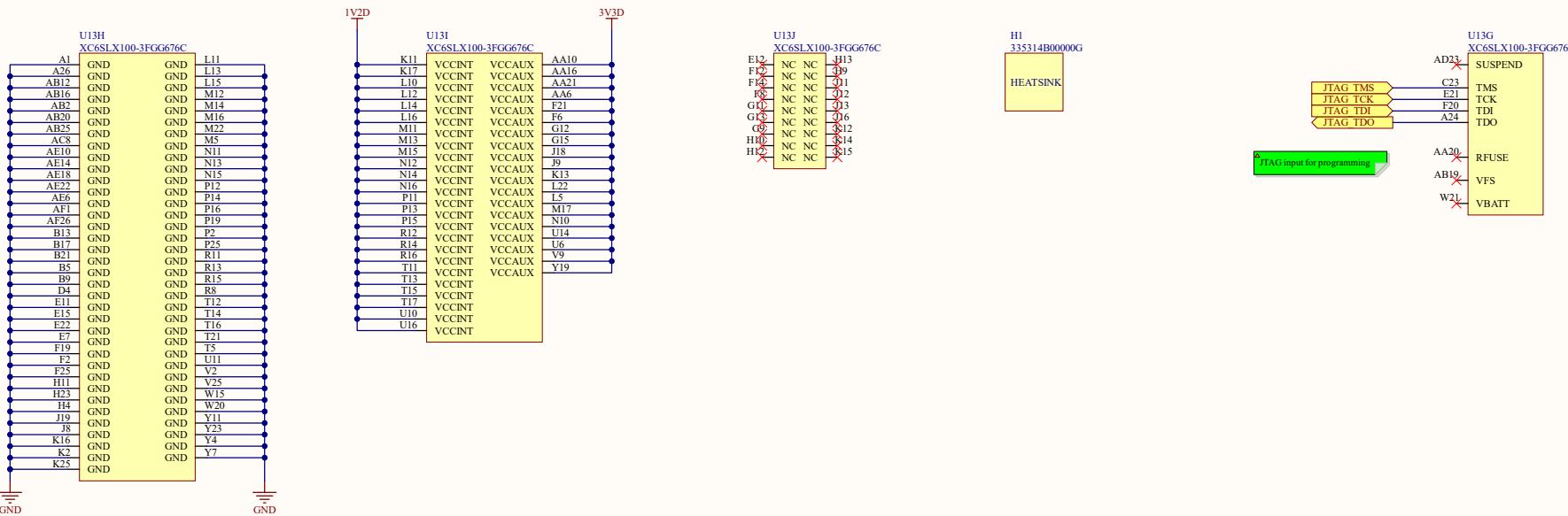
Date 2026-01-2

Sheet 8 of 18

SZGAS_BIPLAIDES_CARTE_MERE_P06_EPG423 SCHD0

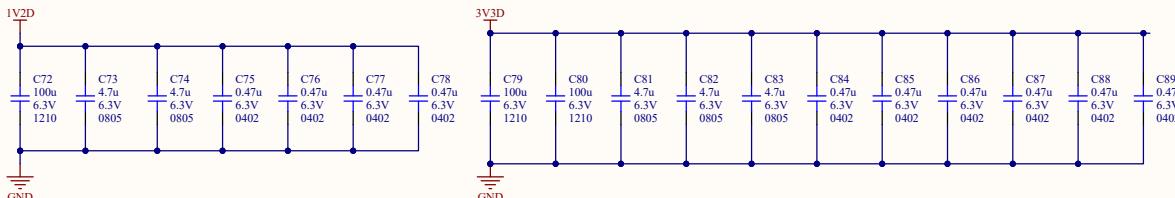
signers
Étienne Provencher
Antoine Allard

FPGA Power and JTAG

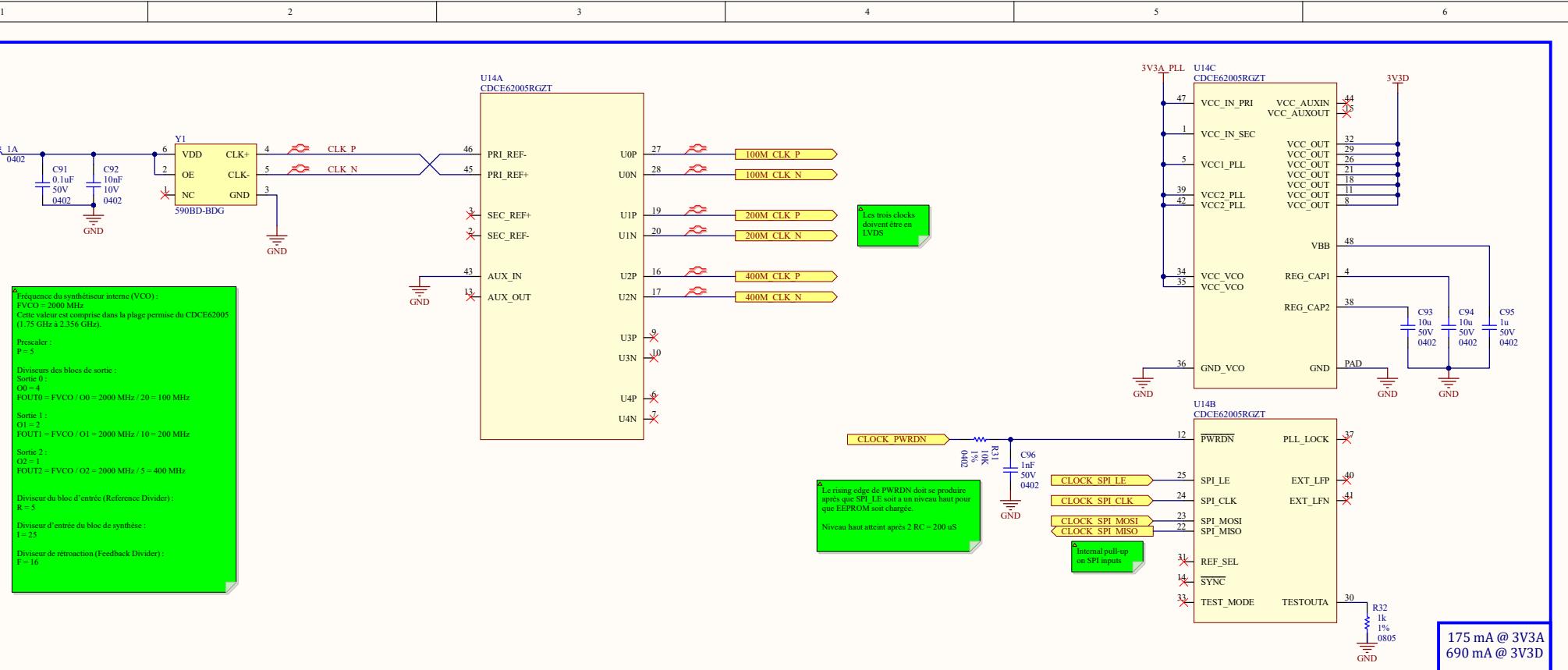


3A @ 1V2D
0.25A @ 3V3D

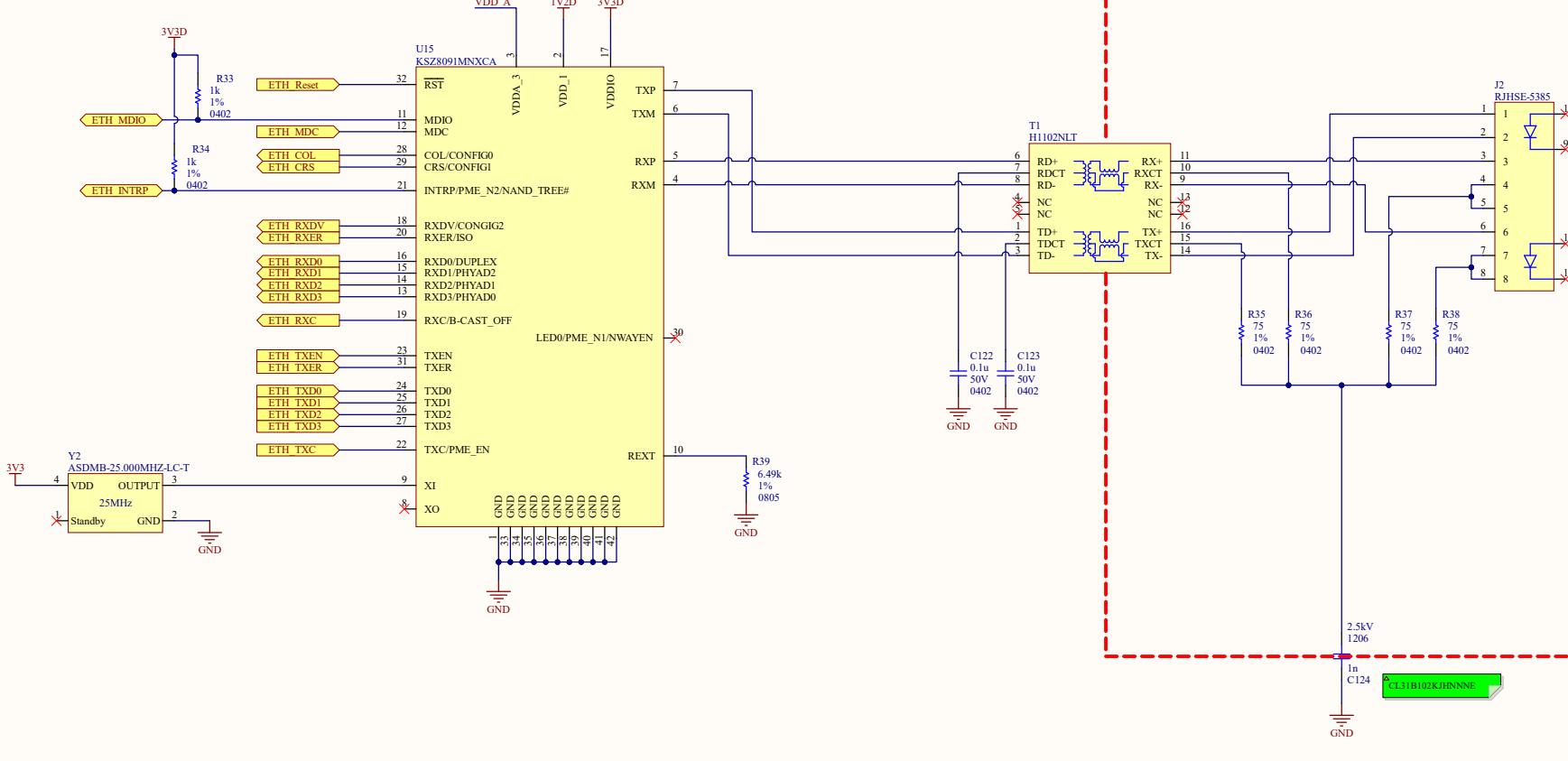
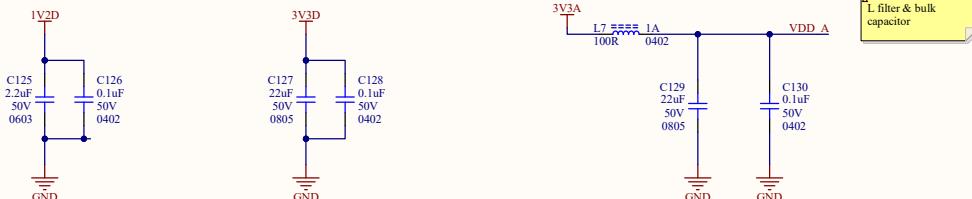
Découplage général FPGA



Sheet Name	FPGA4		
Project Title	S7CAS-PLEIDES-CARTE-MERE_P06		
Global Project	S7APP1-2		
Size 11x17	Group	P-06	Revision 1.00
Date 2026-01-21	Sheet 9	of 18	
Filename S7CAS-PLEIDES-CARTE-MERE_P06_FPGA4.SCHDOC	Designers Étienne Provencher Antoine Allard		



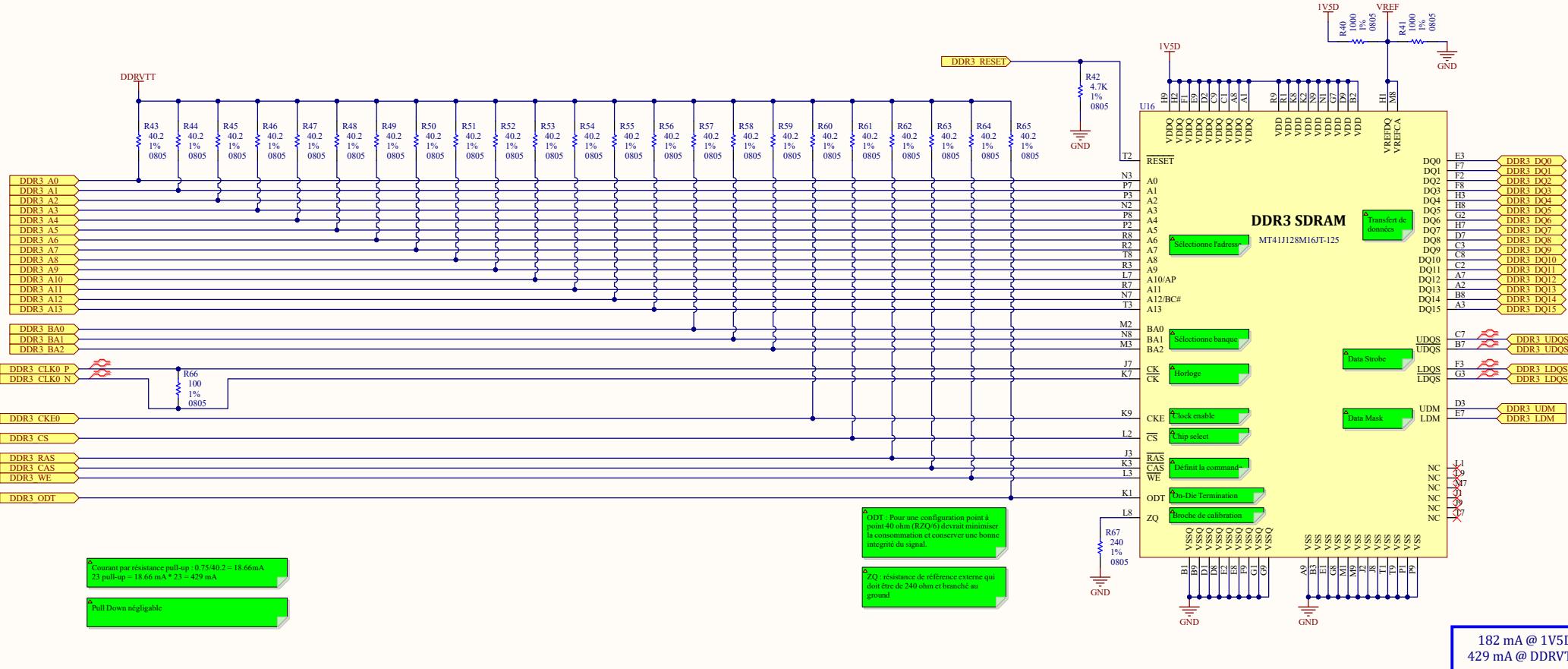
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Global Project	S7APP1-2		
Size	11x17	Group	Revision
		P-06	1.00
Date	2026-01-21	Sheet	10 of 18
Filename	S7CAS-PLEIDES-CARTE-MERE_P06_CLOCK.SchDoc		Designers Étienne Provencher Antoine Allard

Ethernet**Découplage Ethernet et filtres**

Sheet Name		ETHERNET	
Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size	11x17	Group	Revision
		P-06	1.00
Date	2026-01-21	Sheet	11 of 18
Filename	S7CAS-PLEIDES-CARTE-MERE_P06_ETHERNETSCHDOC		Designers
	Étienne Provencher Antoine Allard		

DDR3

A



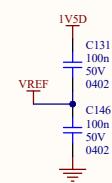
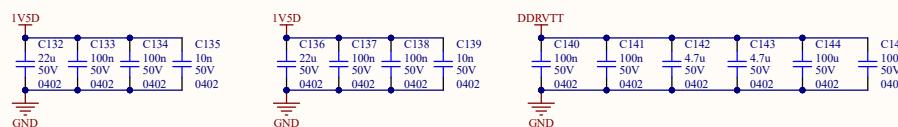
B

B

C

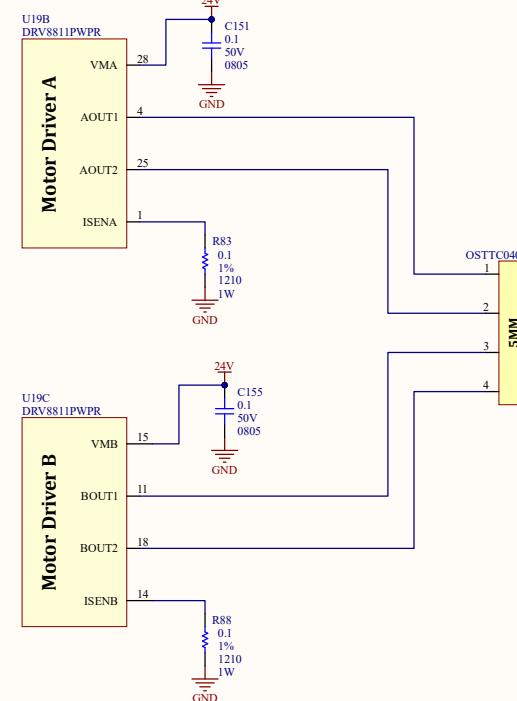
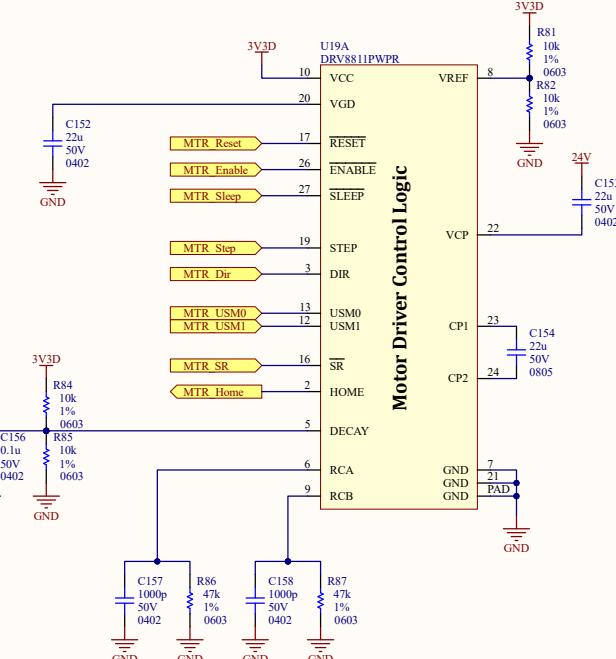
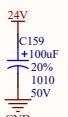
D

Découplage DDR3

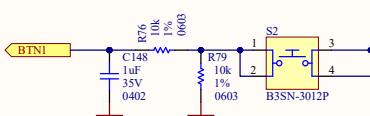
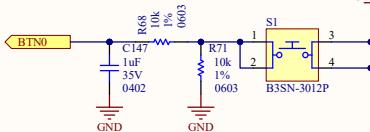
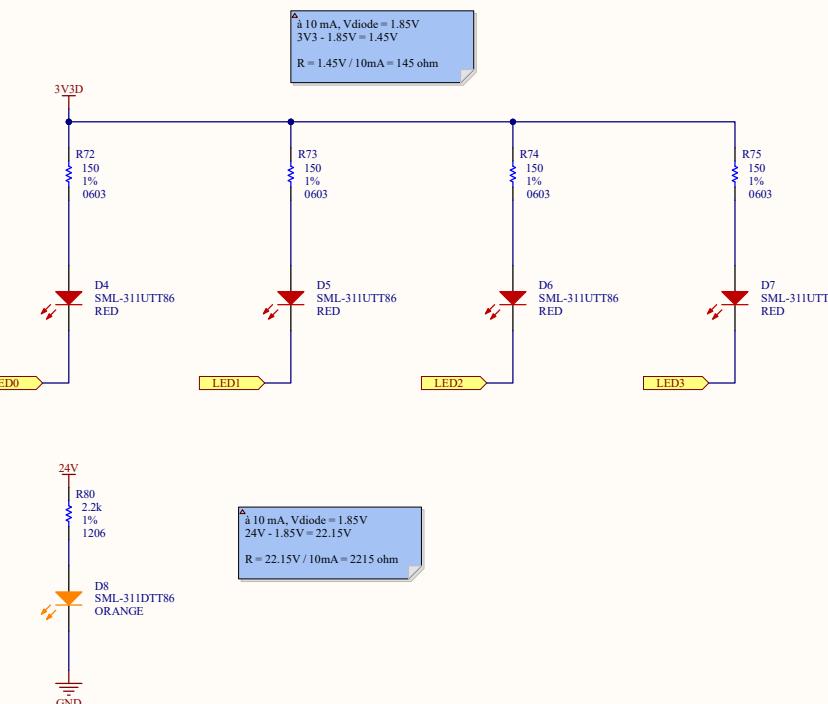


Sheet Name

DDR3Project Title **S7CAS-PLEIDES-CARTE-MERE_P06**Global Project **S7APP1-2**Size **11x17** Group **P-06** Revision **1.00**Date **2026-01-21** Sheet **12** of **18**Filename **S7CAS-PLEIDES-CARTE-MERE_P06_DDR3.SCHDOC** Designers **Étienne Provencher
Antoine Allard**

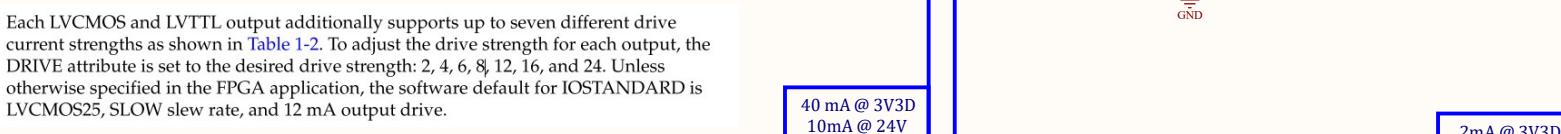
MOTEUR3.8 A @ 24V
4 mA @ 3V3D**Découplage MOTEUR**

Sheet Name		MOTOR	
Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size	11x17	Group	Revision
		P-06	1.00
Date	2026-01-21	Sheet	13 of 18
Filename	S7CAS-PLEIDES-CARTE-MERE_P06_MOTOR.SCHDOC		Designers
	Étienne Provencher Antoine Allard		

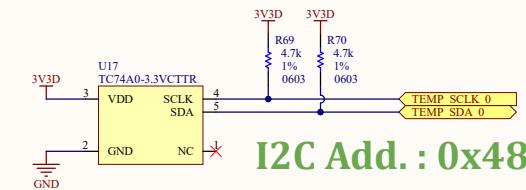
Buttons**LEDS**

Each LVCMOS and LVTTL output additionally supports up to seven different drive current strengths as shown in Table 1-2. To adjust the drive strength for each output, the DRIVE attribute is set to the desired drive strength: 2, 4, 6, 8, 12, 16, and 24. Unless otherwise specified in the FPGA application, the software default for IOSTANDARD is LVCMOS25, SLOW slew rate, and 12 mA output drive.

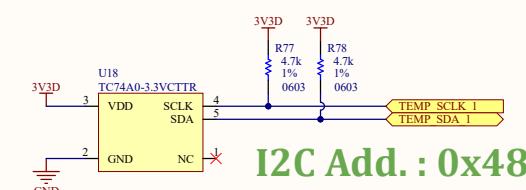
40 mA @ 3V3D
10mA @ 24V



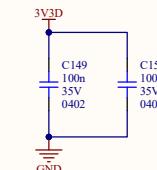
La carte doit contenir 3 boutons-poussoirs (Reset FPGA et 2 entrées au FPGA), 4 DEL servant au déverminage du FPGA, une DEL indiquant que l'alimentation 24 V est fonctionnelle ainsi que 2 senseurs de température de type TC74.

Temp sensors

I2C Add. : 0x48



I2C Add. : 0x48



2mA @ 3V3D

Sheet Name

MISC

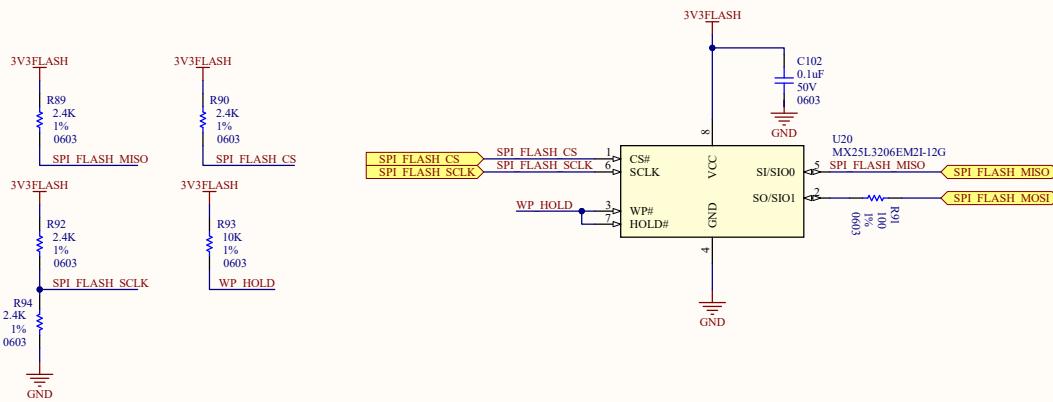
Project Title **S7CAS-PLEIDES-CARTE-MERE_P06**

Global Project **S7APP1-2**

Size 11x17	Group P-06	Revision 1.00
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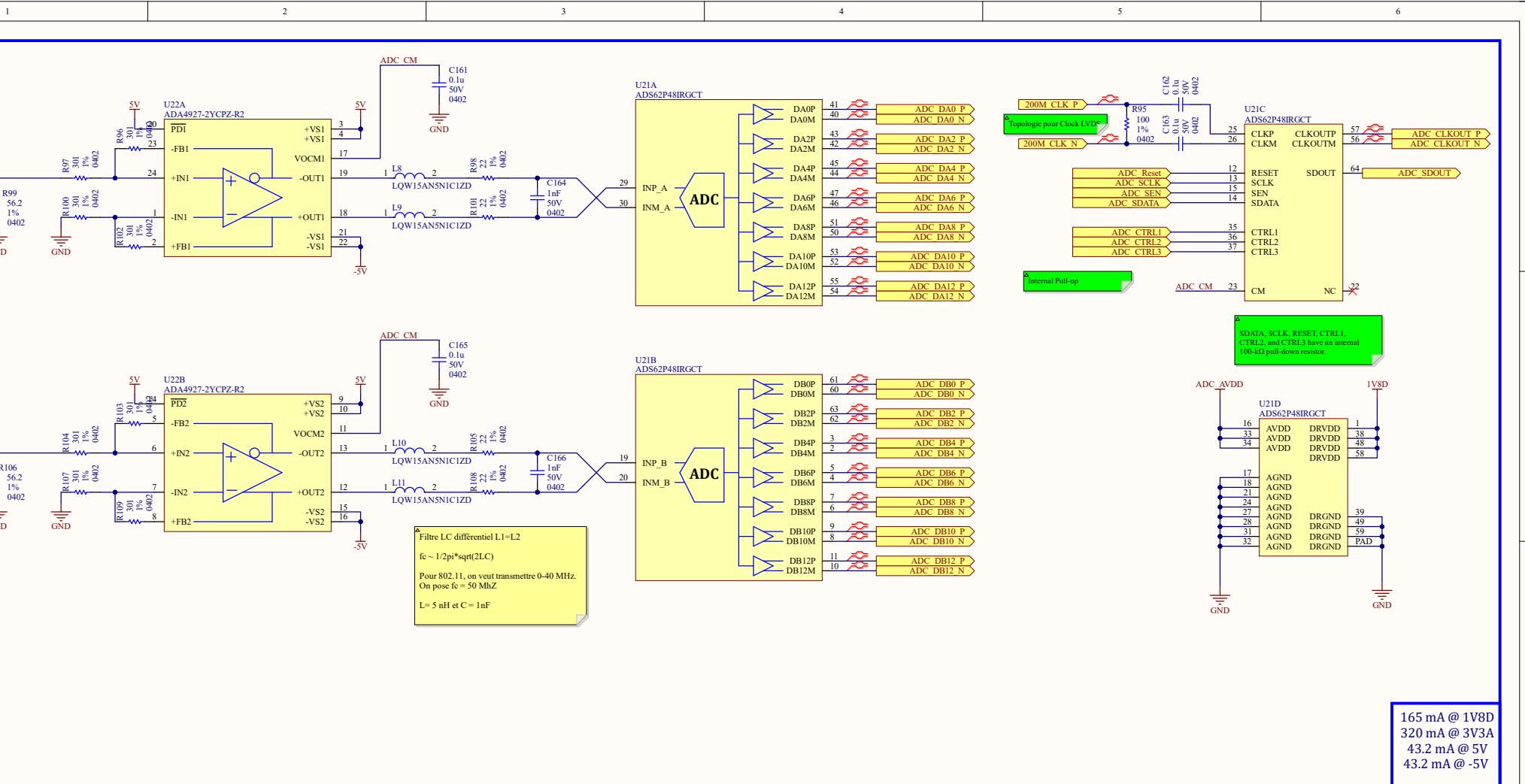
Date 2026-01-21	Sheet 14 of 18
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Filename S7CAS-PLEIDES-CARTE-MERE_P06_MISC.SchDoc	Designers Étienne Provencher Antoine Allard
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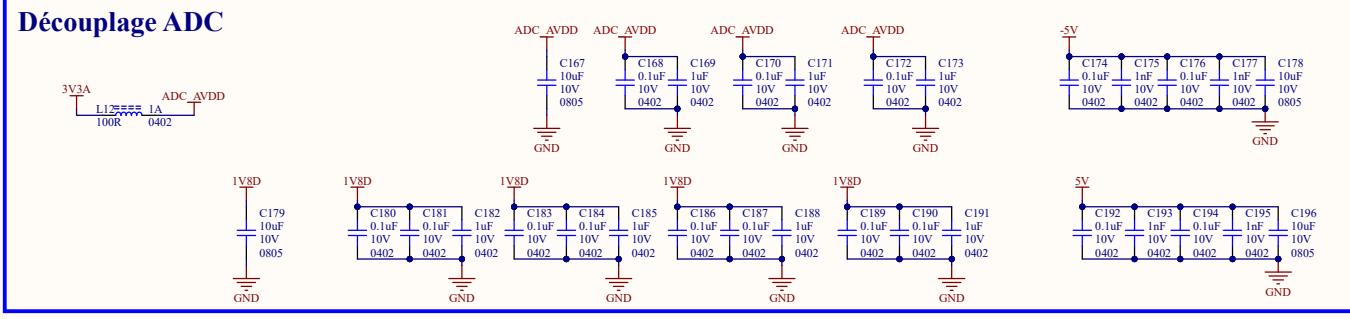
FLASH

25 mA @ 3V3D

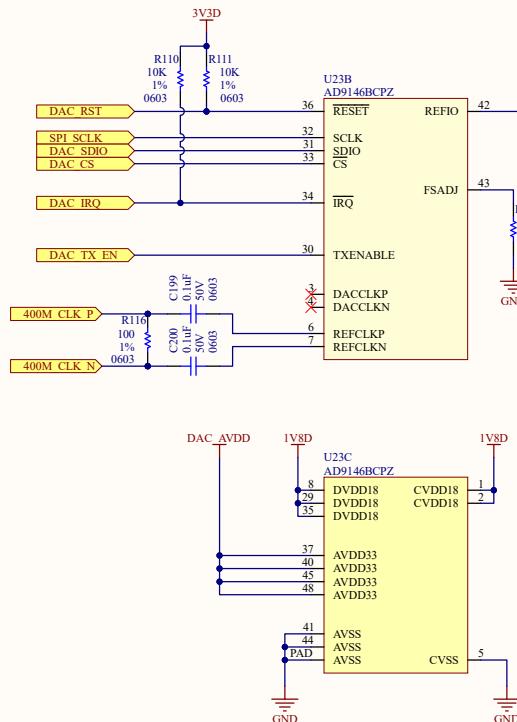
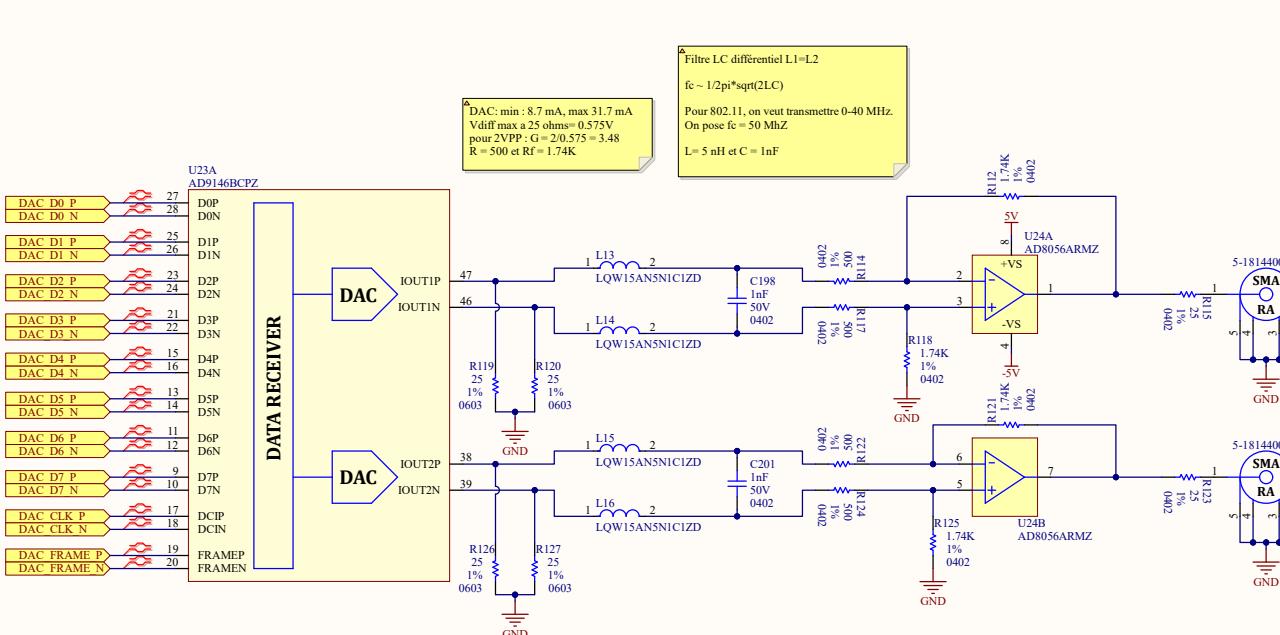
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Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size 11x17	Group	P-06	Revision 1.00
Date 2026-01-21	Sheet	15	of 18
Filename S7CAS-PLEIDES-CARTE-MERE_P06_FLASH.SCHDOC		Designers Étienne Provencher Antoine Allard	



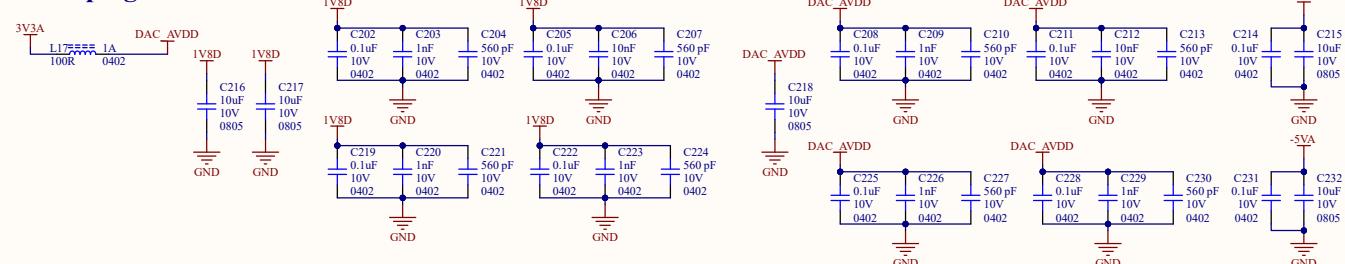
Découplage ADC



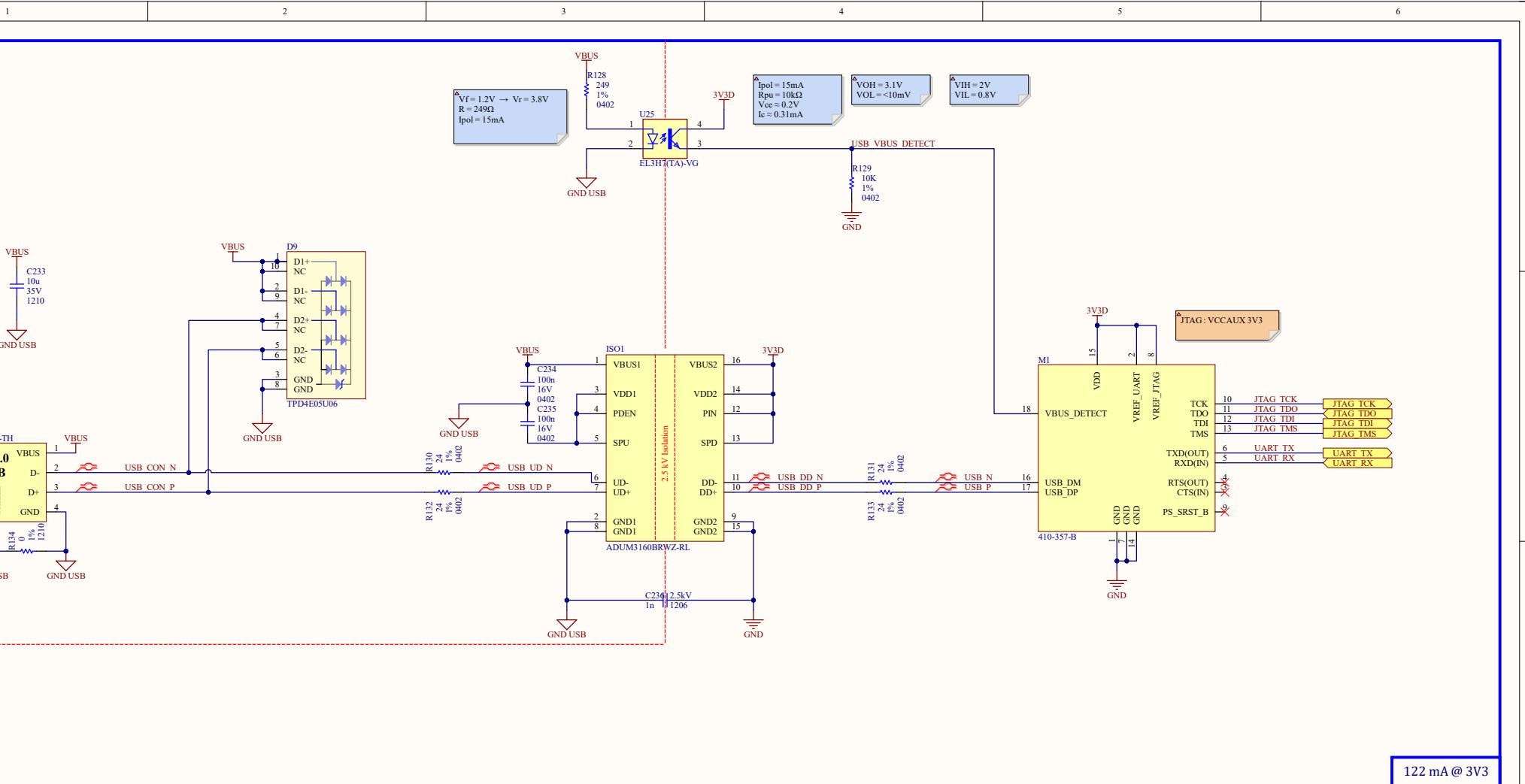
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Global Project		S7APP1-2	
Size	11x17	Group	Revision 1.00
Date	2026-01-21	Sheet	16 of 18
Filename	S7CAS-PLEIDES-CARTE-MERE_P06_ADC.SchDoc		Designers Étienne Provencher Antoine Allard

DAC

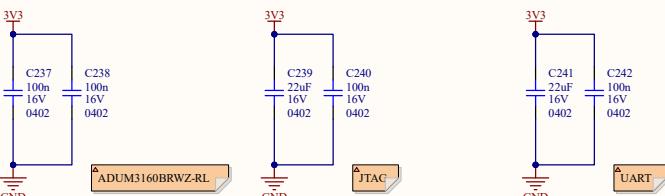
401 mA @ 1V8D
56 mA @ 3V3A
13.3 mA @ 5V
13.3 mA @ -5V

Découplage DAC

Sheet Name	DAC		
Project Title	S7CAS-PLEIDES-CARTE-MERE_P06		
Global Project	S7APP1-2		
Size	11x17	Group	Revision 1.00
Date	2026-01-21	Sheet	17 of 18
Filename	S7CAS-PLEIDES-CARTE-MERE_P06_DAC.SchDoc		Designers Étienne Provencher, Antoine Allard



Découplage USB



Sheet Name		USB_PROGRAMMER	
Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size 11x17	Group	P-06	Revision 1.00
Date 2026-01-21	Sheet 18 of 18		
Filename S7CAS-PLEIDES-CARTE-MERE_P06_USB_PROGRAMMER.SCHDOC	Designers Étienne Provencher Antoine Allard		