S7CAS-PLEIDES-CARTE-MERE_P06

S7APP1-2

Dream Team

Revision 1.00

Date : 2026-01-21

Revision history	

Package size conversion	
Metric	*Imperial*
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

Project Title: S7CAS-PLEIDES-CARTE-MERE_P06		
Global Project: *S7APP1-2*		
Size: 11x17	Group: Dream Team	Revision: 1.00
Date: 2026-01-21	Sheet: 1 of 18	
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_TITLE.SchDoc	Designers: Étienne Provencher, Antoine Allard	

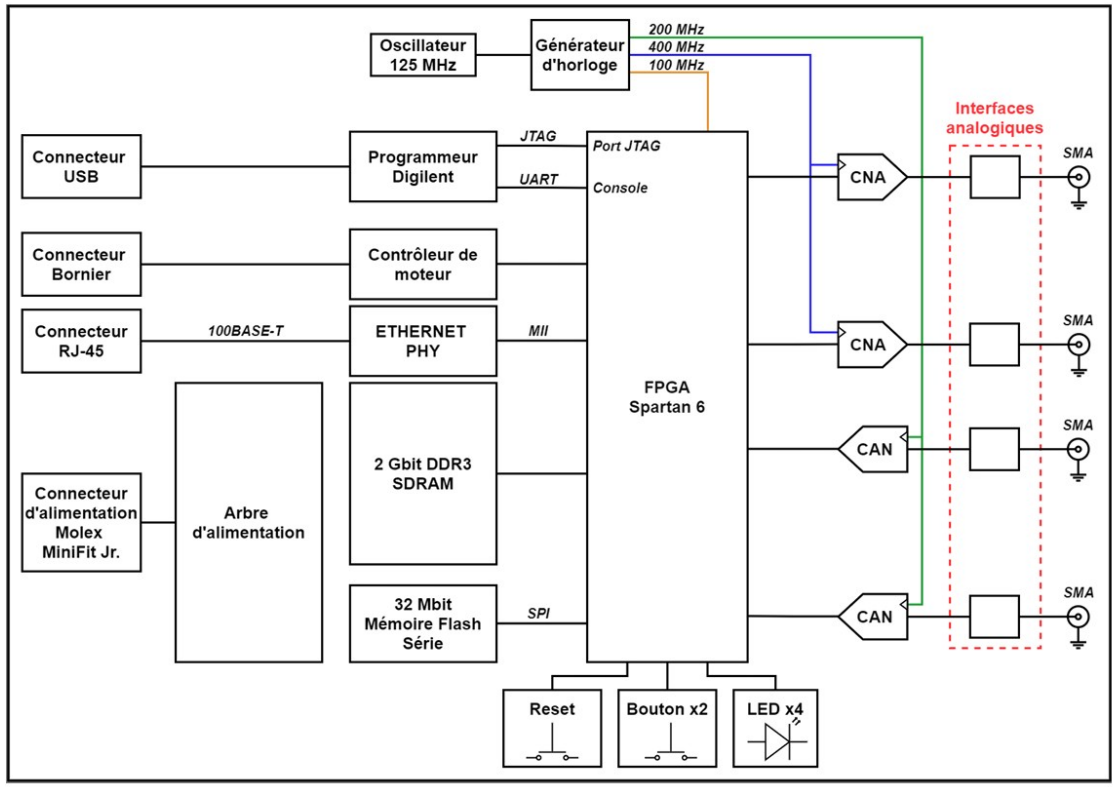
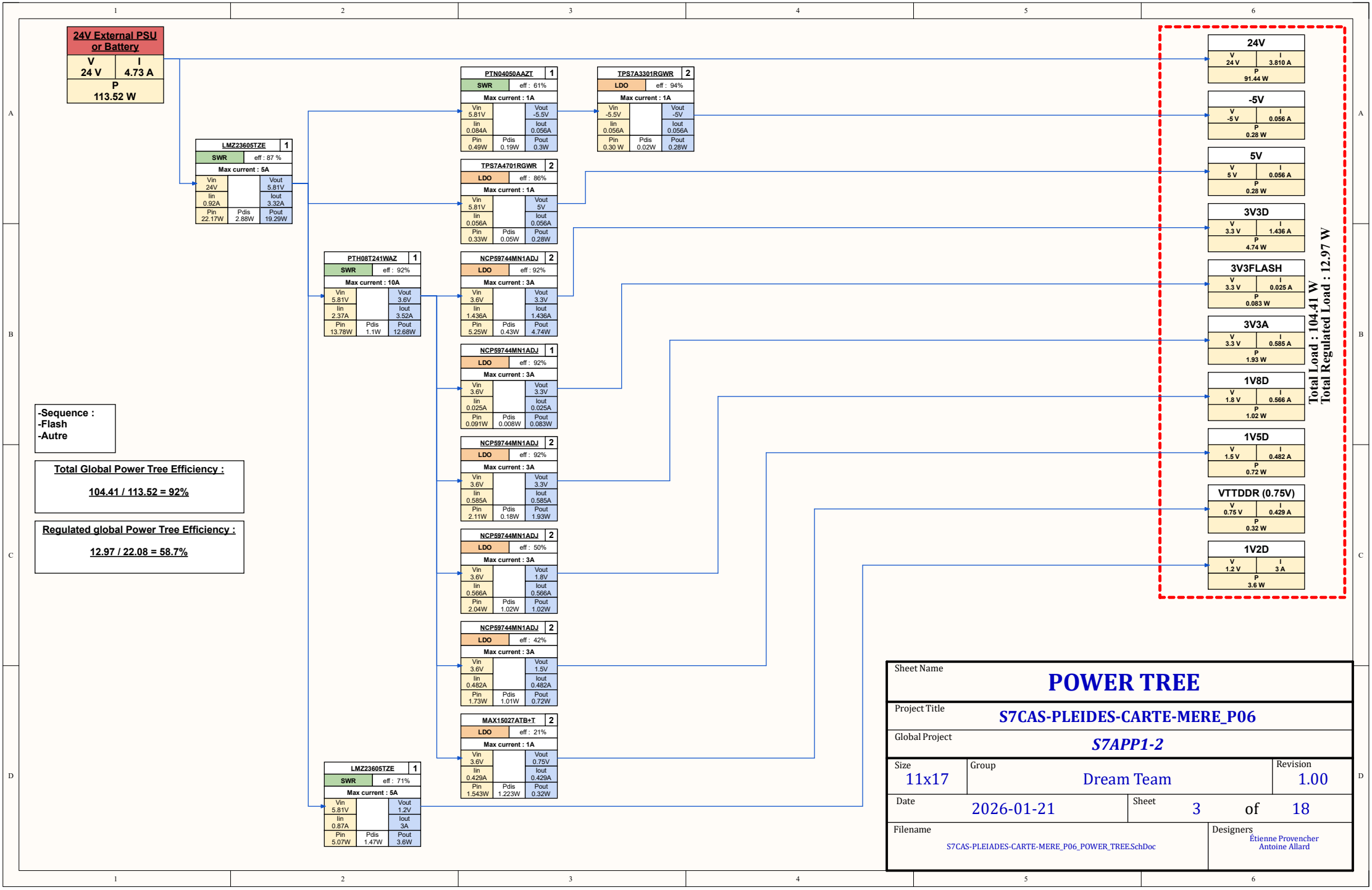


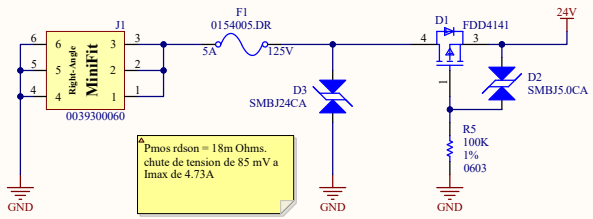
Figure 2 : Diagramme fonctionnel de la carte *Pléiades*

Sheet Name	**BLOCK DIAGRAM**		
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**		
Global Project	***S7APP1-2***		
Size: 11x17	Group: Dream Team		Revision: 1.00
Date: 2026-01-21	Sheet: 2 of 18		
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_BLOCK_DIAGRAM.SchDoc		Designers: Étienne Provencher, Antoine Allard	



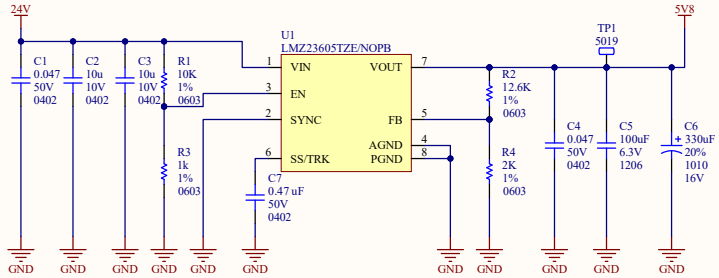
Sheet Name	**POWER TREE**
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size	11x17
Group	Dream Team
Revision	1.00
Date	2026-01-21
Sheet	3 of 18
Filename	S7CAS-PLEIADES-CARTE-MERE_P06_POWER_TREE.SchDoc
Designers	Étienne Provencher Antoine Allard

Power input & Protections



4.73 A @ 24V

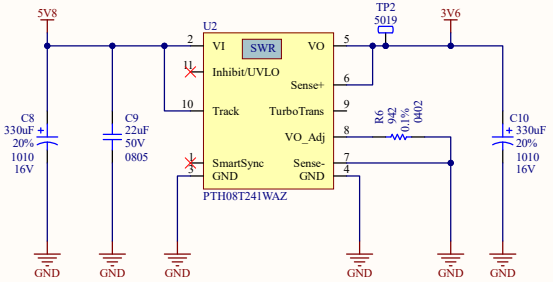
Bucks 24V à 5.8V



0.92 A @ 24V

3.39 A @ 5.81V

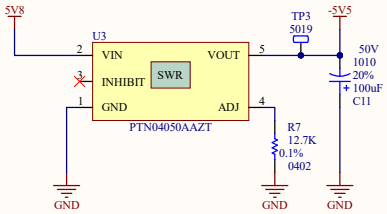
Bucks 5.8 à 3.6



2.37 A @ 5.8V

3.52 A @ 3.6V

Bucks 5.8 à -5.5



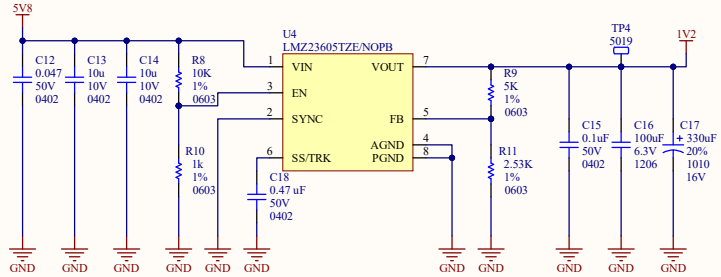
0.084 A @ 5.8V

0.056 A @ -5.5V

Power table

Sheet	Absolute maximum									
	Current @ 24V	Current @ 5V	Current @ -5V	Current @ 3V3D	Current @ 3V3FLASH	Current @ 3V3A	Current @ 1V8D	Current @ 1V5D	Current @ 1V2D	Current @ VTTDDR (0.75V)
FPGA1	0 mA	0 mA	0 mA	0.1 A	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FPGA2	0 mA	0 mA	0 mA	0.05 A	0 mA	0 mA	0 mA	0.3 A	0 mA	0 mA
FPGA3	0 mA	0 mA	0 mA	0.15 A	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FPGA4	0 mA	0 mA	0 mA	0.25 A	0 mA	0 mA	0 mA	0 mA	3 A	0 mA
CLOCK	0 mA	0 mA	0 mA	690 mA	0 mA	175 mA	0 mA	0 mA	0 mA	0 mA
ETHERNET	0 mA	0 mA	0 mA	28 mA	0 mA	34 mA	0 mA	0 mA	0 mA	0 mA
DDR3	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	182 mA	0 mA	429 mA
MISC	10 mA	0 mA	0 mA	42 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
MOTOR	3.8 A	0 mA	0 mA	4 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FLASH	0 mA	0 mA	0 mA	0 mA	25 mA	0 mA	0 mA	0 mA	0 mA	0 mA
ADC	0 mA	43.2 mA	43.2 mA	0 mA	0 mA	320 mA	165 mA	0 mA	0 mA	0 mA
DAC	0 mA	13.3 mA	13.3 mA	0 mA	0 mA	56 mA	401 mA	0 mA	0 mA	0 mA
USB_PROG	0 mA	0 mA	0 mA	122 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
Total	**3.810 A**	**0.056 A**	**0.056 A**	**1.436 A**	**0.025 A**	**0.585 A**	**0.566 A**	**0.482 A**	**3.000 A**	**0.429 A**

Bucks 5.8V à 1.2V



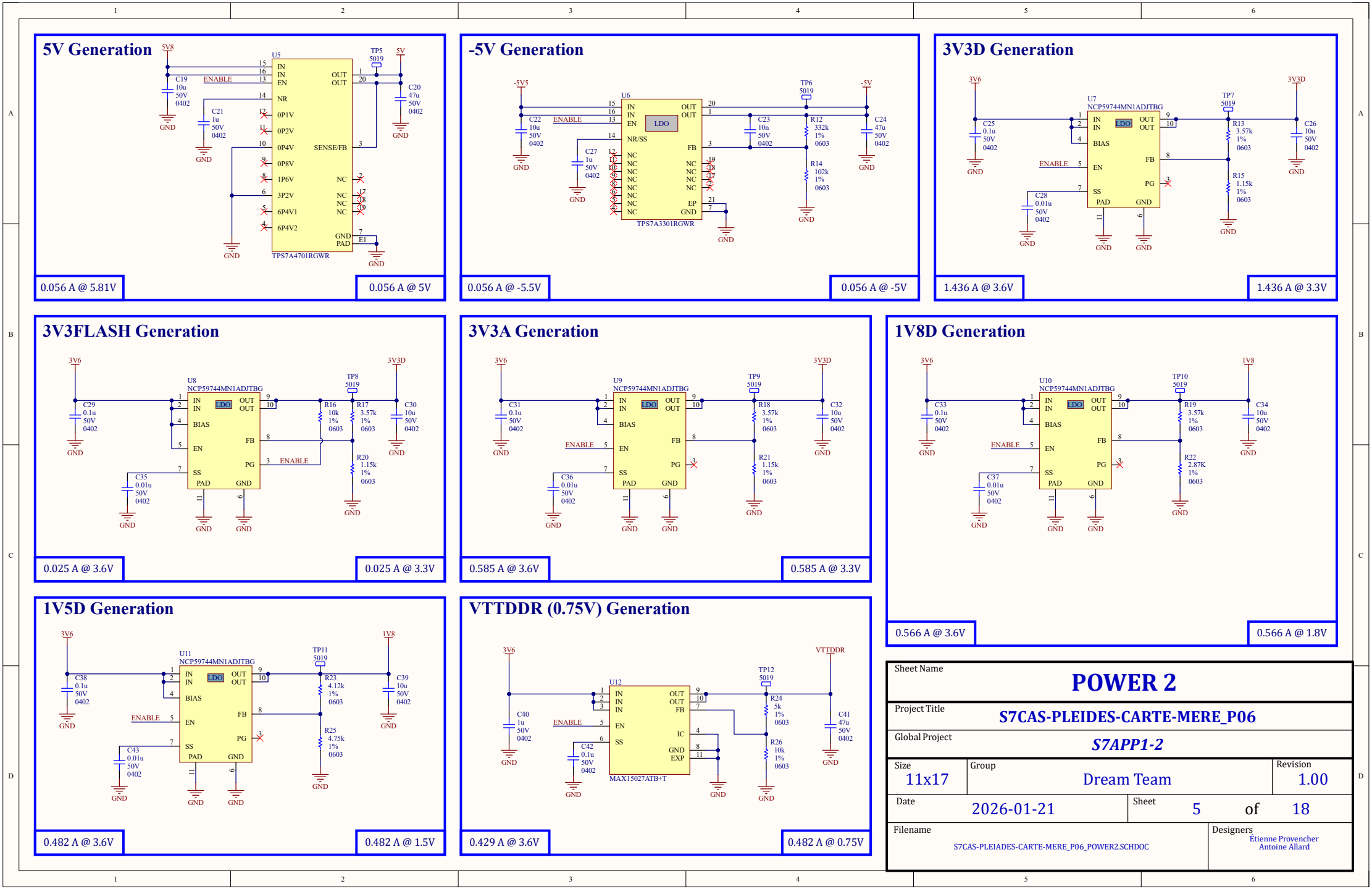
0.87 A @ 5.8V

3 A @ 1.2V

Sheet Name	**POWER 1**
Project Title	**S7CAS-PLEIADES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size: 11x17	Group: Dream Team — Revision: 1.00
Date: 2026-01-21	Sheet: 4 of 18
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_POWER1.SCHDOC	Designers: Étienne Provencher, Antoine Allard

–24	1.15 MΩ	59	19.84	±(1.5% + 0.21%)

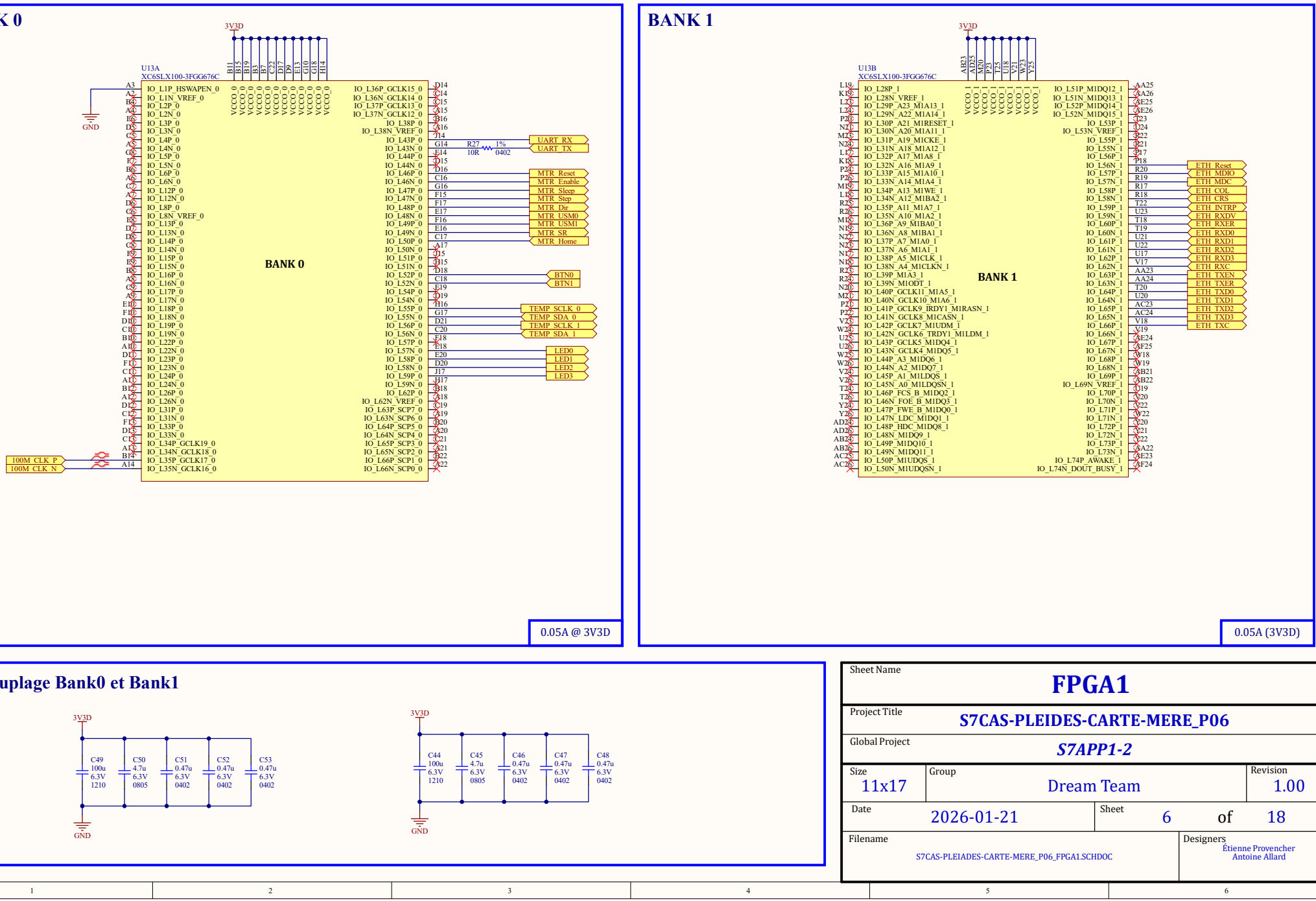
Figure 24. Typical Application, V_{OUT} = 3.3 V



Typical Operating Circuits

Programming the Output Voltage

The MAX15027/MAX15028 feature an adjustable output



Sheet Name	**FPGA1**
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size	11x17
Group	Dream Team
Revision	1.00
Date	2026-01-21
Sheet	6 of 18
Filename	S7CAS-PLEIADES-CARTE-MERE_P06_FPGA1.SCHDOC
Designers	Étienne Provencher Antoine Allard

Table 2-1: **Required PCB Capacitor Quantities per Device[1][3] *(Continued)***

Table 2-2: **PCB Capacitor Specifications**

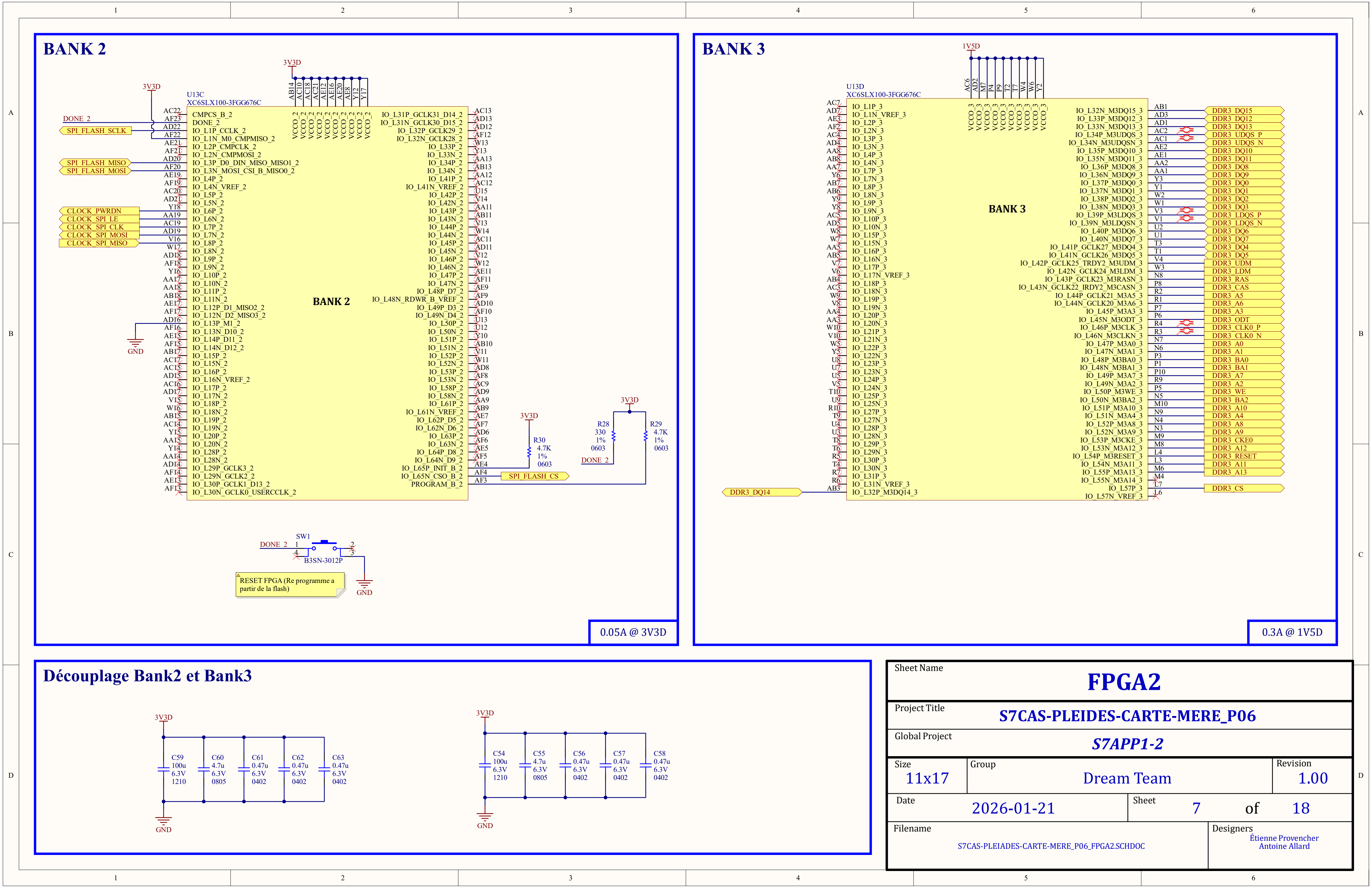
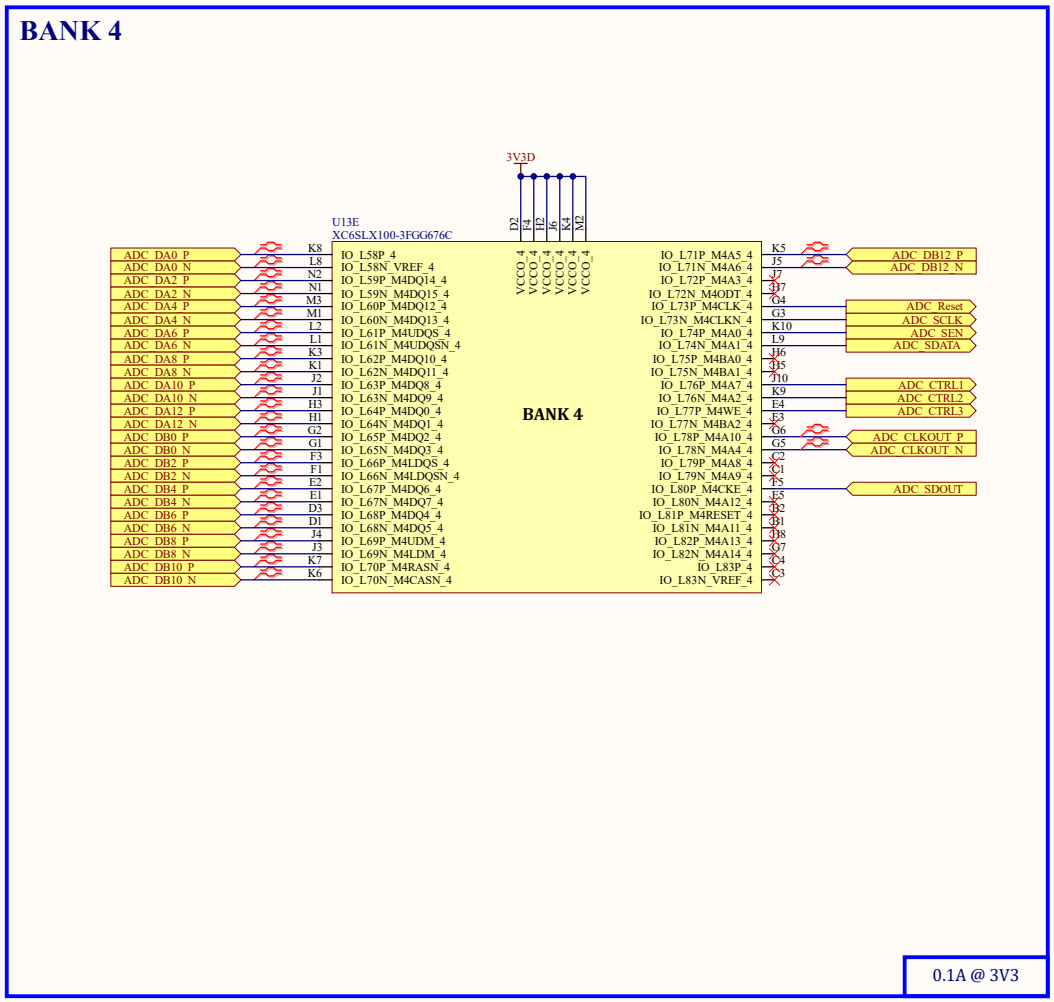
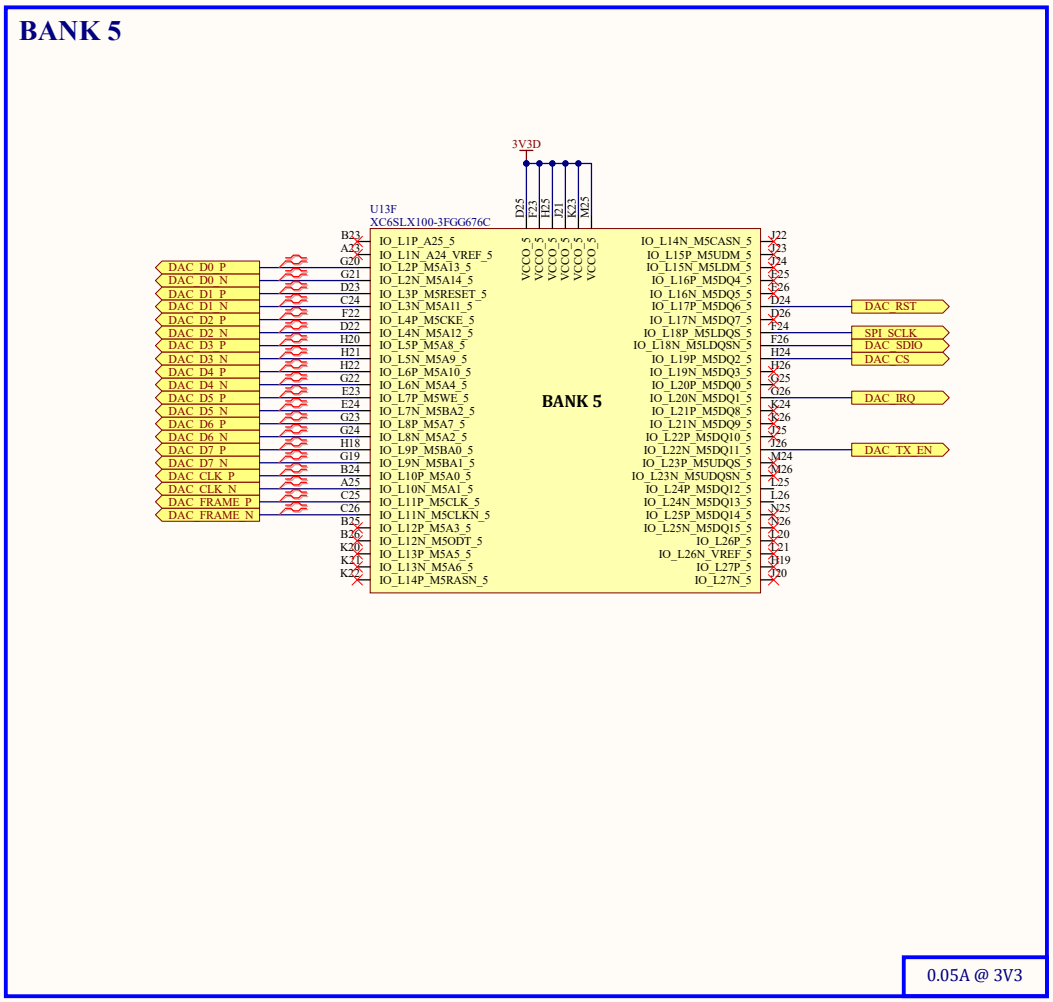
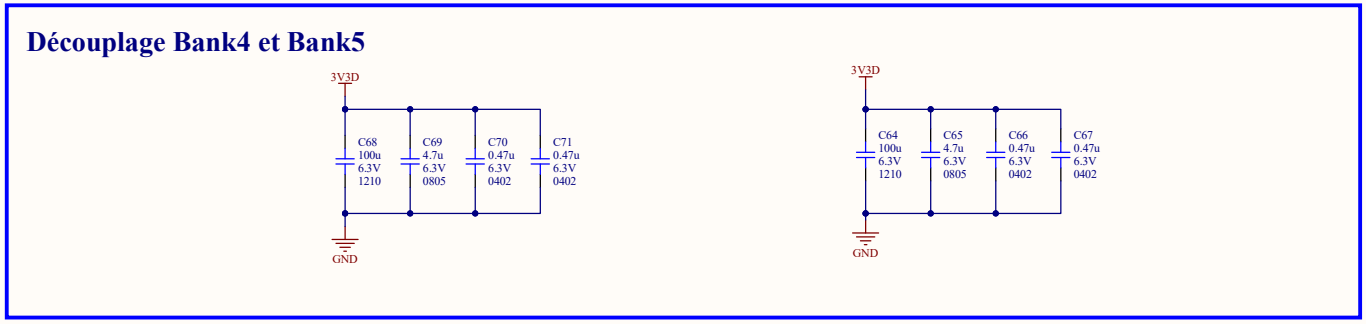


Table 2-1: **Required PCB Capacitor Quantities per Device**[1][3] ***(Continued)***

Table 2-2: **PCB Capacitor Specifications**





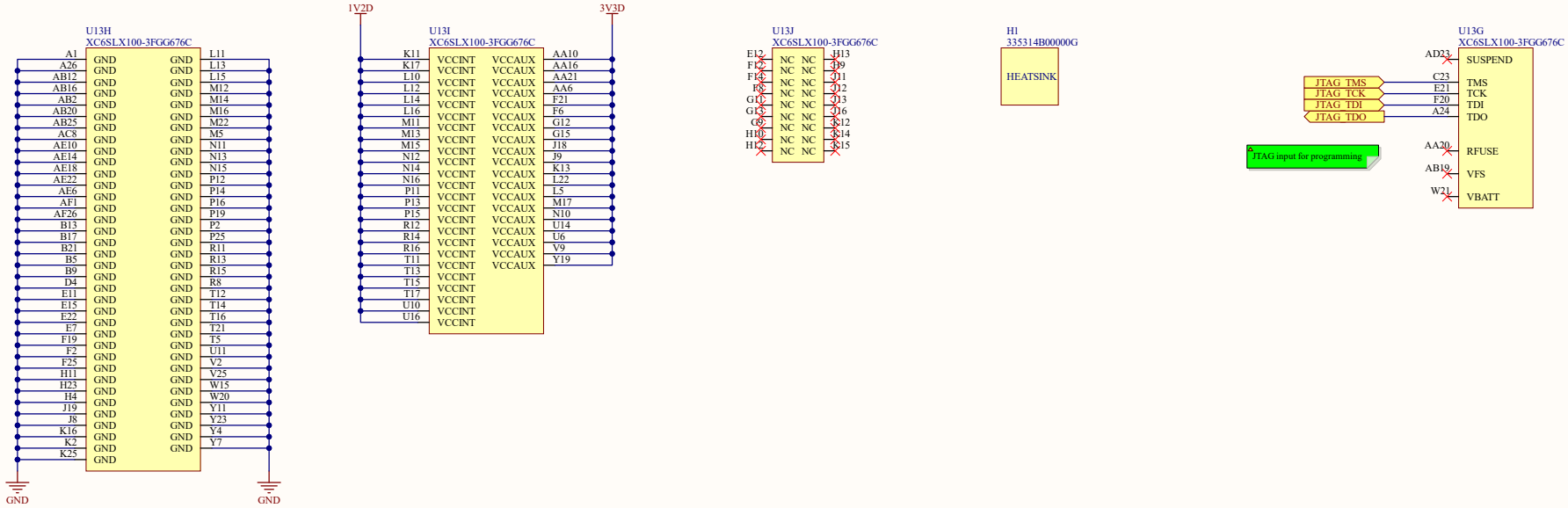


Sheet Name	**FPGA3**
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size: 11x17 / Group: Dream Team / Revision: 1.00	
Date: 2026-01-21 / Sheet: 8 of 18	
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_FPGA3.SCHDOC	Designers: Étienne Provencher, Antoine Allard

Table 2-1: **Required PCB Capacitor Quantities per Device[1][3] *(Continued)***

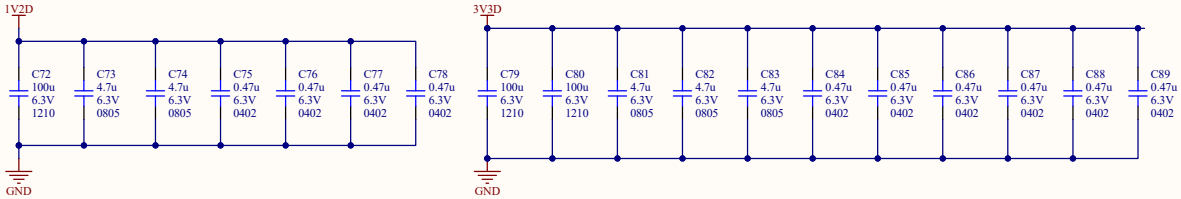
Table 2-2: **PCB Capacitor Specifications**

FPGA Power and JTAG



3A @ 1V2D
0.25A @ 3V3D

Découplage général FPGA



Sheet Name	**FPGA4**
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size: 11x17 / Group: Dream Team / Revision: 1.00	
Date: 2026-01-21 / Sheet: 9 of 18	
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_FPGA4.SCHDOC	Designers: Étienne Provencher, Antoine Allard

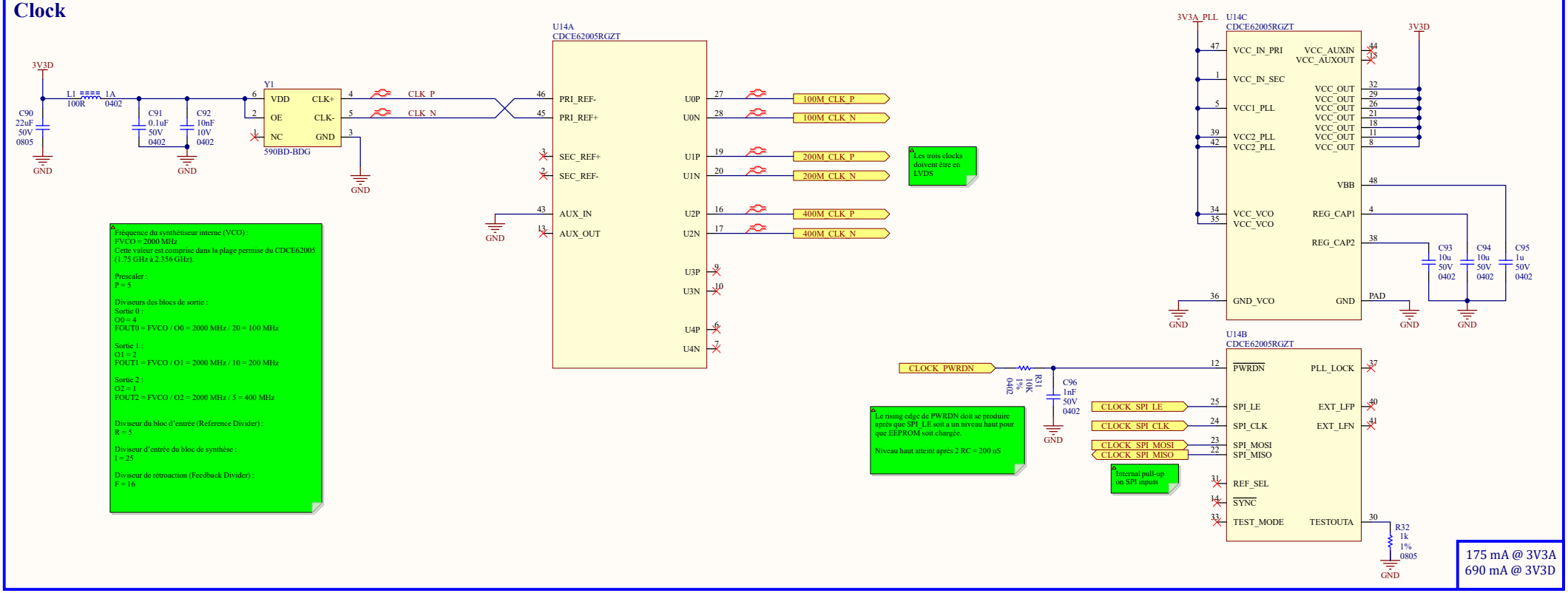
Table 2-1: **Required PCB Capacitor Quantities per Device[1][3]** ***(Continued)***

			V_{CCO}	V_{CCO}	V_{CCO}	V_{CCO}	V_{CCO}	V_{CCO}	

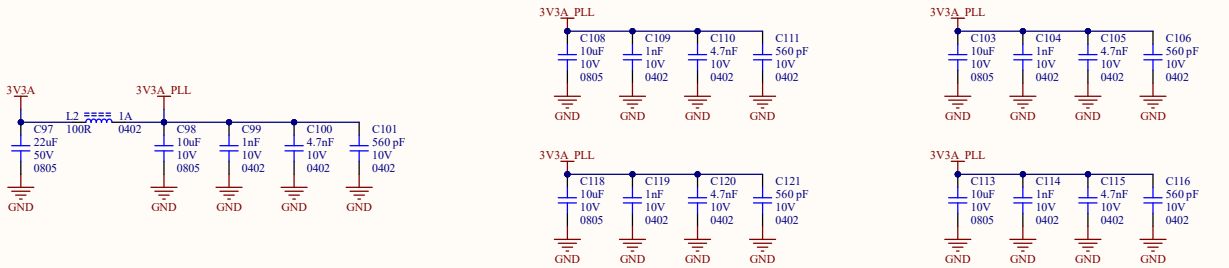
Table 2-2: **PCB Capacitor Specifications**

Ideal	Value	Body		ESL		Voltage	Suggested

Clock



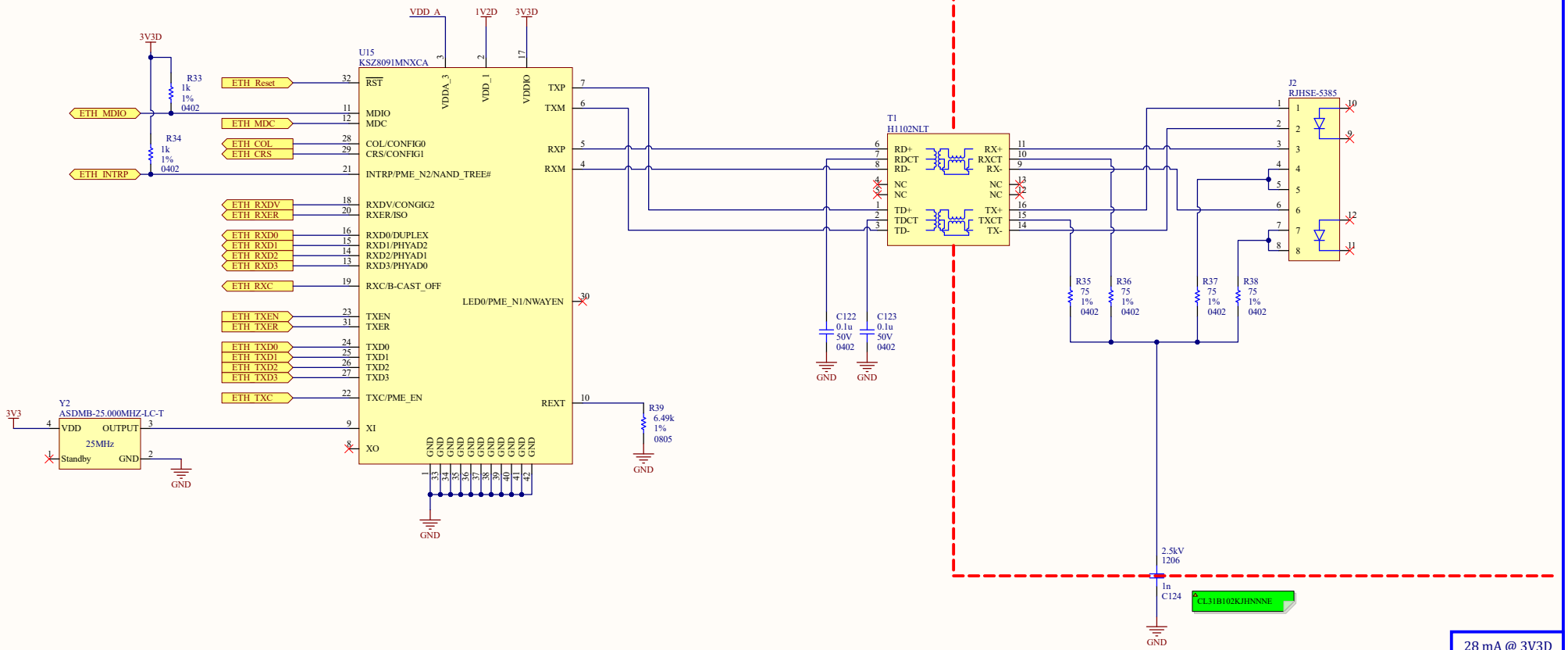
Découplage Clock & Filtre



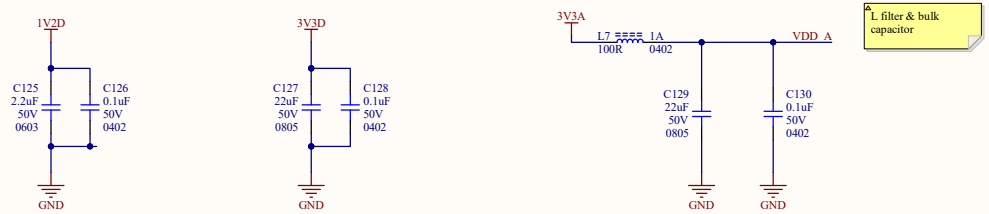
Sheet Name	**CLOCK**	
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**	
Global Project	***S7APP1-2***	
Size: 11x17	Group: Dream Team	Revision: 1.00
Date: 2026-01-21	Sheet: 10 of 18	
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_CLOCK.SchDoc	Designers: Étienne Provencher, Antoine Allard	

Assuming a 3.3-V board supply, the ferrite bead maximum dc resistance for each VCC_PLL can be 3 Ω; for each VCC_IN, the resistance can be 12 Ω each; for VCC_VCO, the resistance can be 6 Ω each; and

Ethernet



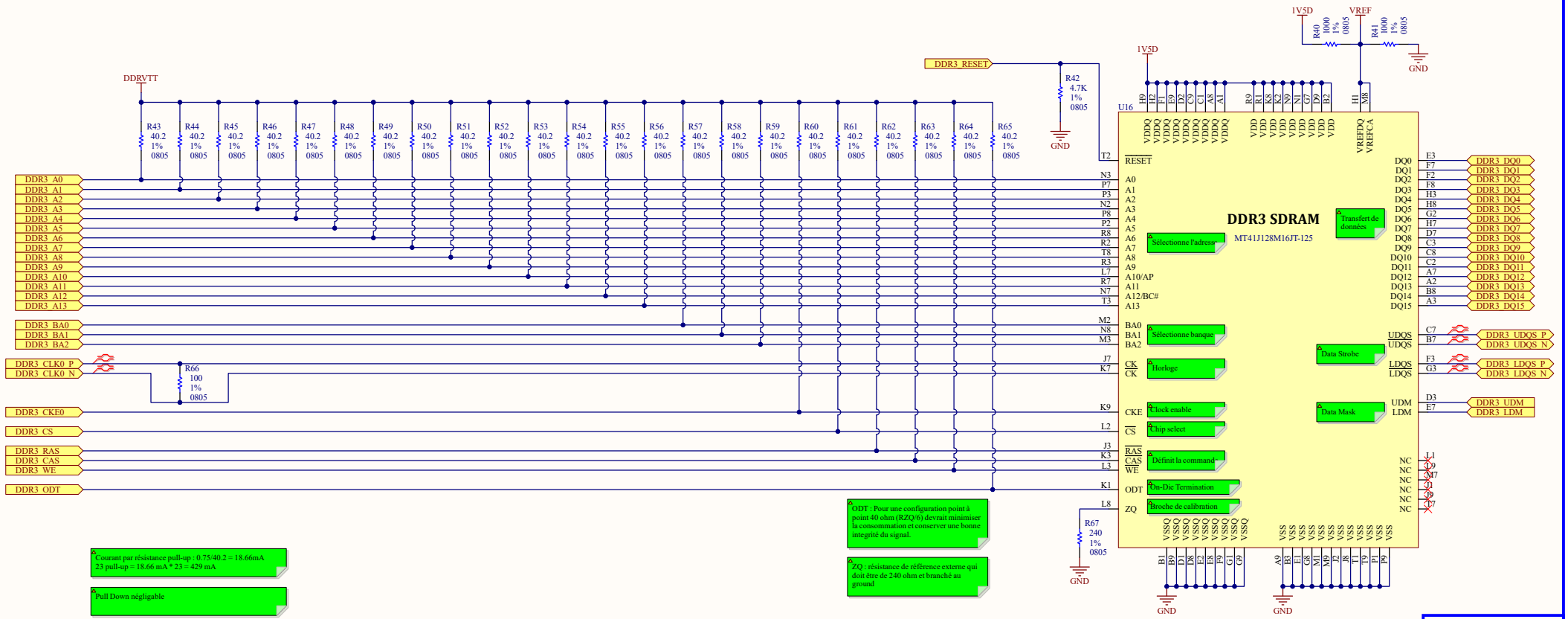
Découplage Ethernet et filtres



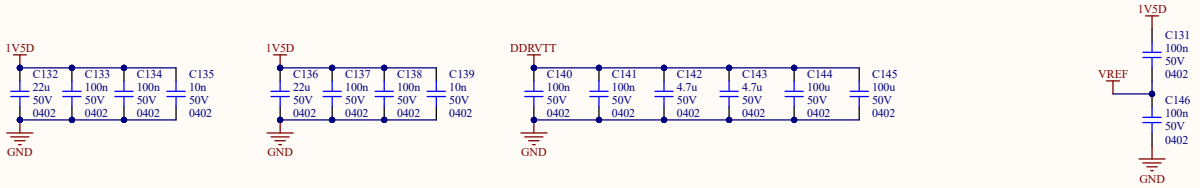
Sheet Name	**ETHERNET**
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size: 11x17	Group: Dream Team — Revision: 1.00
Date: 2026-01-21	Sheet: 11 of 18
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_ETHERNET.SCHDOC	Designers: Étienne Provencher, Antoine Allard

t_{REFI}	Average periodic refresh cycle time	7,8	µs
$t_{CK\ (MIN)}$	Minimum t_{CK} cycle rate	1,25	ns

DDR3



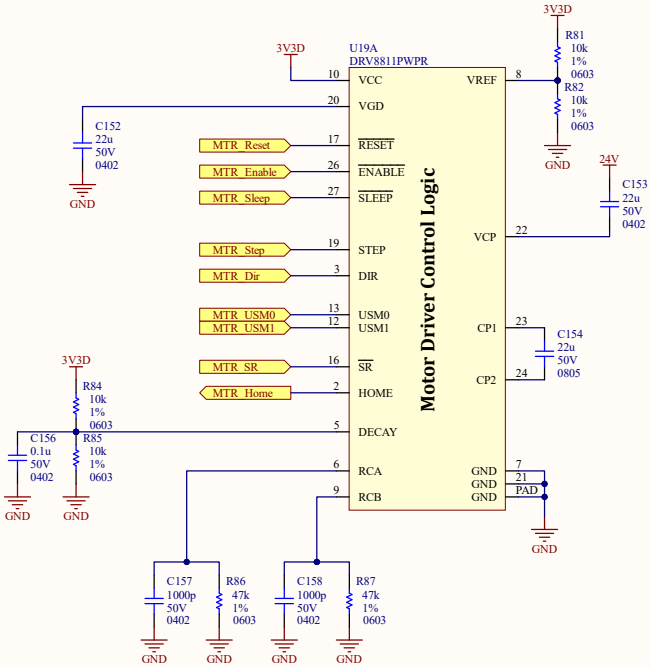
Découplage DDR3

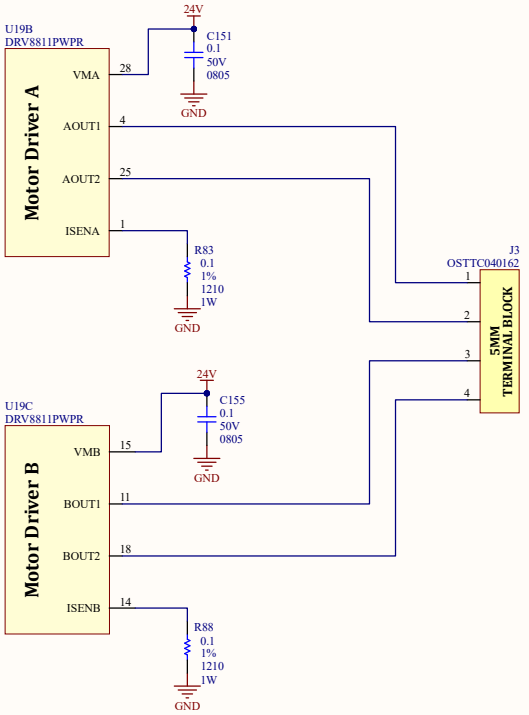


Sheet Name	**DDR3**		
Project Title	**S7CAS-PLEIADES-CARTE-MERE_P06**		
Global Project	***S7APP1-2***		
Size: 11x17	Group: Dream Team		Revision: 1.00
Date: 2026-01-21	Sheet: 12 of 18		
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_DDR3.SCHDOC		Designers: Étienne Provencher, Antoine Allard	

Type de condensateur ↓ \ Alimentation → V

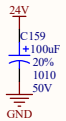
MOTEUR





3.8 A @ 24V
4 mA @ 3V3D

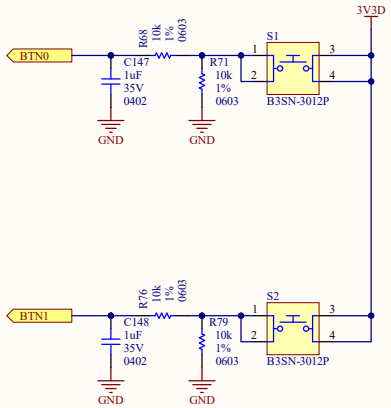
Découplage MOTEUR



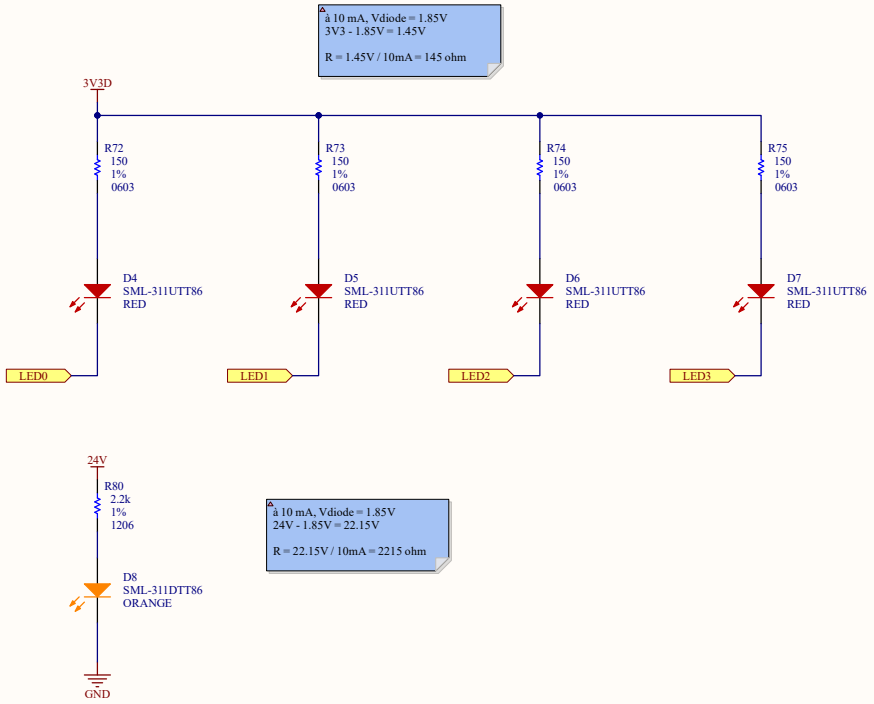
Sheet Name	**MOTOR**
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size: 11x17	Group: Dream Team — Revision: 1.00
Date: 2026-01-21	Sheet: 13 of 18
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_MOTOR.SCHDOC	Designers: Étienne Provencher, Antoine Allard

Il faut aussi prévoir un contrôleur de moteur pas-à-pas basé sur un circuit intégré DRV8811 de Texas

Buttons



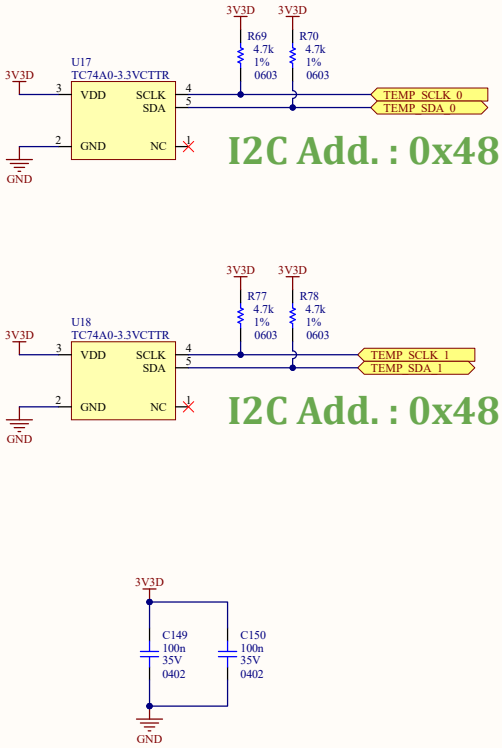
LEDS



Each LVCMOS and LVTTL output additionally supports up to seven different drive current strengths as shown in Table 1-2. To adjust the drive strength for each output, the DRIVE attribute is set to the desired drive strength: 2, 4, 6, 8, 12, 16, and 24. Unless otherwise specified in the FPGA application, the software default for IOSTANDARD is LVCMOS25, SLOW slew rate, and 12 mA output drive.

40 mA @ 3V3D
10mA @ 24V

Temp sensors

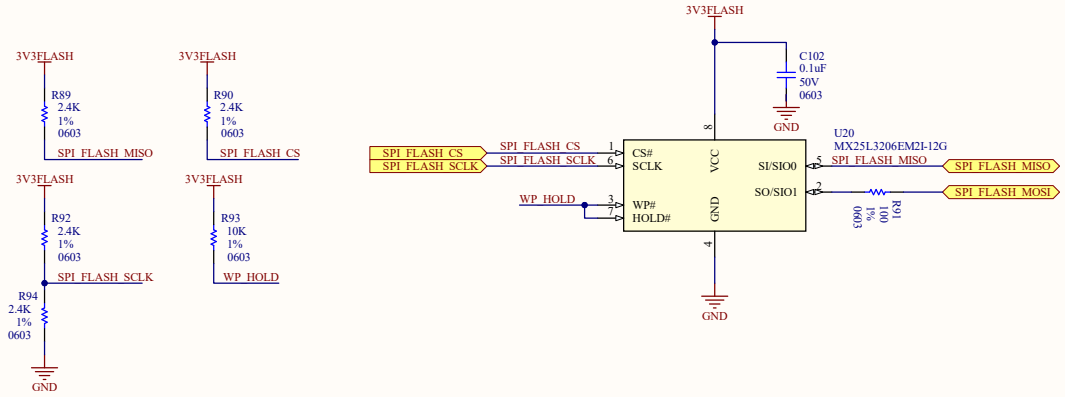


2mA @ 3V3D

La carte doit contenir 3 boutons-poussoirs (Reset FPGA et 2 entrées au FPGA), 4 DEL servant au déverminage du FPGA, une DEL indiquant que l'alimentation 24 V est fonctionnelle ainsi que 2 senseurs de température de type TC74.

Sheet Name	**MISC**	
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**	
Global Project	***S7APP1-2***	
Size: 11x17	Group: Dream Team	Revision: 1.00
Date: 2026-01-21	Sheet: 14 of 18	
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_MISC.SchDoc	Designers: Étienne Provencher, Antoine Allard	

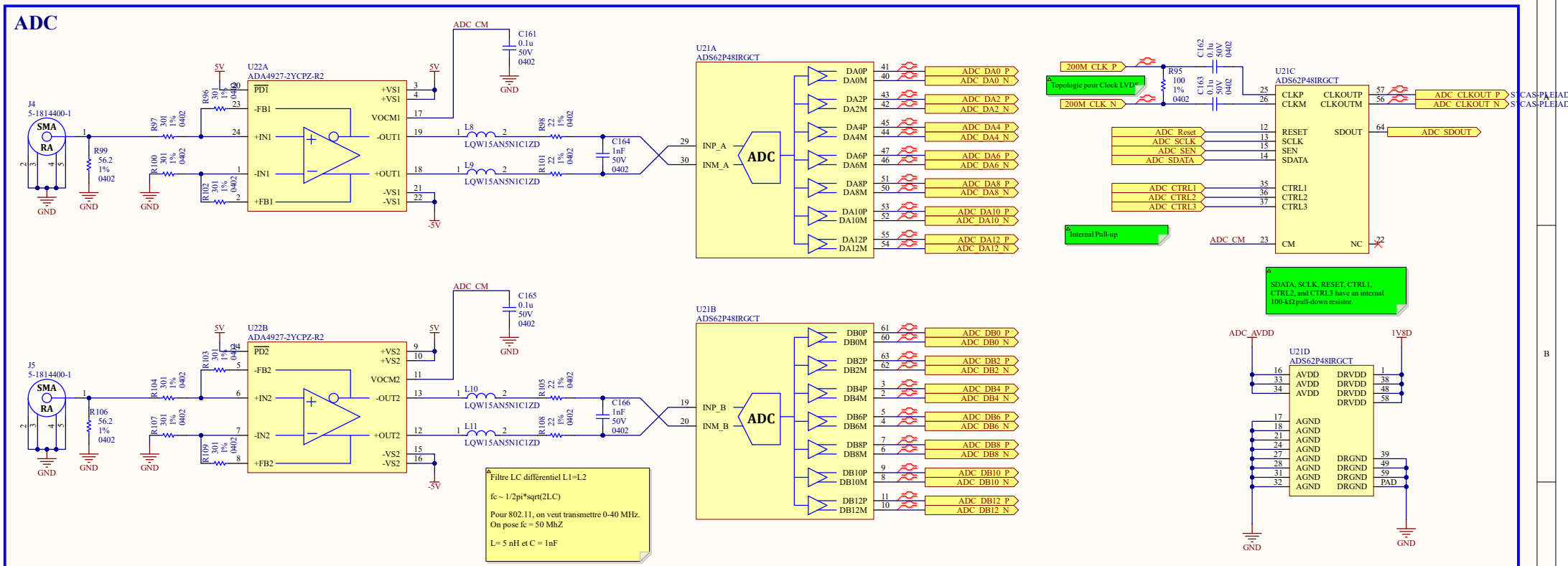
FLASH



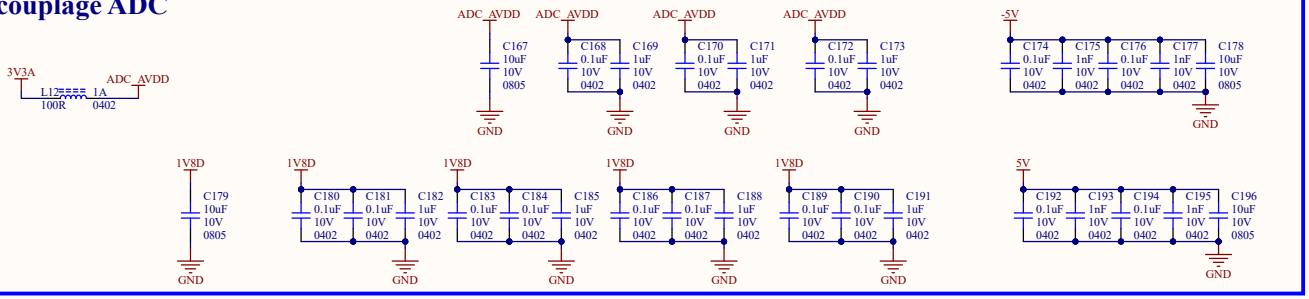
25 mA @ 3V3D

Sheet Name	**FLASH**	
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**	
Global Project	***S7APP1-2***	
Size: 11x17	Group: Dream Team	Revision: 1.00
Date: 2026-01-21	Sheet: 15 of 18	
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_FLASH.SCHDOC	Designers: Étienne Provencher, Antoine Allard	

ADC



Découplage ADC

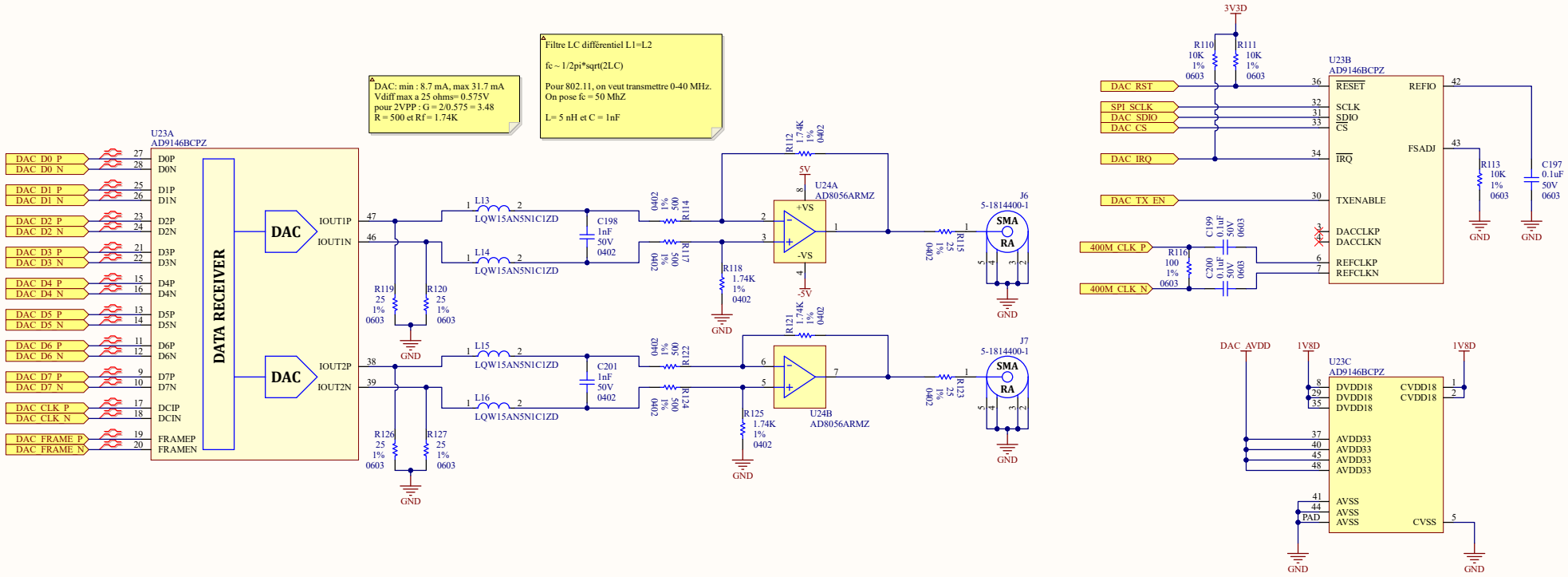


Sheet Name	**ADC**
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size: 11x17	Group: Dream Team
Revision: 1.00	
Date: 2026-01-21	Sheet: 16 of 18
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_ADC.SchDoc	Designers: Étienne Provencher, Antoine Allard

Supply Decoupling

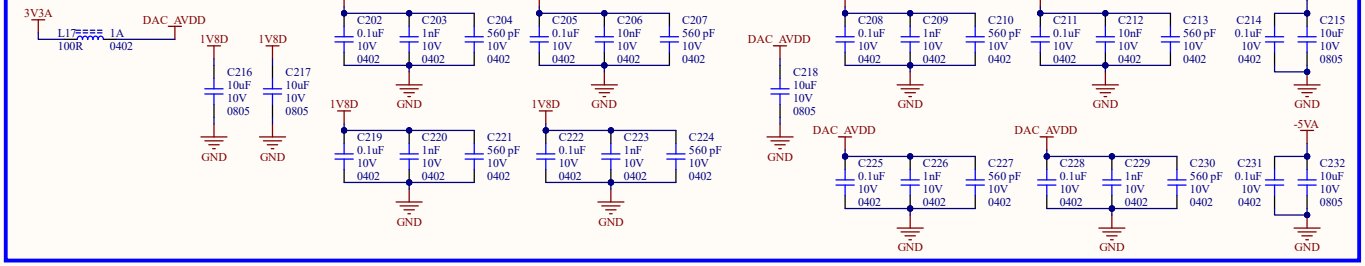
As ADS62Px9/x8 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum

DAC

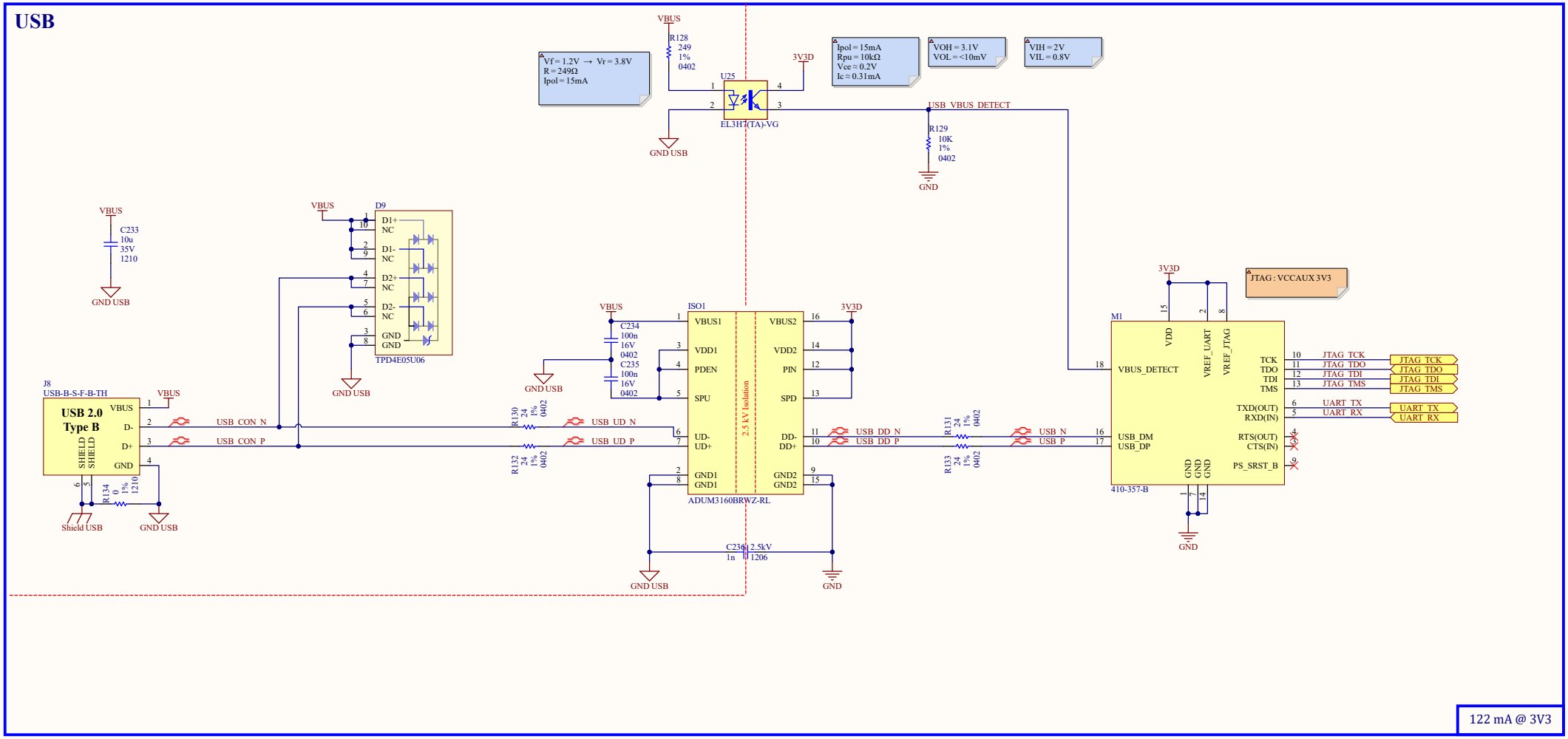


401 mA @ 1V8D
56 mA @ 3V3A
13.3 mA @ 5V
13.3 mA @ -5V

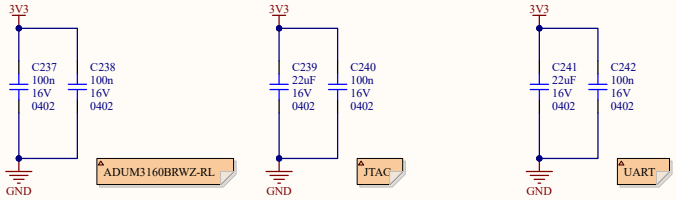
Découplage DAC



Sheet Name	**DAC**
Project Title	**S7CAS-PLEIADES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size: 11x17	Group: Dream Team — Revision: 1.00
Date: 2026-01-21	Sheet: 17 of 18
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_DAC.SchDoc	Designers: Étienne Provencher, Antoine Allard



Découplage USB



Sheet Name	**USB_PROGRAMMER**
Project Title	**S7CAS-PLEIDES-CARTE-MERE_P06**
Global Project	***S7APP1-2***
Size: 11x17	Group: Dream Team — Revision: 1.00
Date: 2026-01-21	Sheet: 18 of 18
Filename: S7CAS-PLEIADES-CARTE-MERE_P06_USB_PROGRAMER.SCHDOC	Designers: Étienne Provencher, Antoine Allard