

# S7CAS-PLEIDES-CARTE-MERE\_P06

## S7APP1-2

*Dream Team*

*Revision 1.00*

*Date : 2026-01-21*

### Revision history


### Package size conversion

Metric	Imperial
1005	0402
1608	0603
2012	0805
3216	1206
3225	1210
6432	2512

Project Title

**S7CAS-PLEIDES-CARTE-MERE\_P06**

Global Project

**S7APP1-2**

Size

**11x17**

Group

**Dream Team**

Revision

**1.00**

Date

**2026-01-21**

Sheet

**1**

of

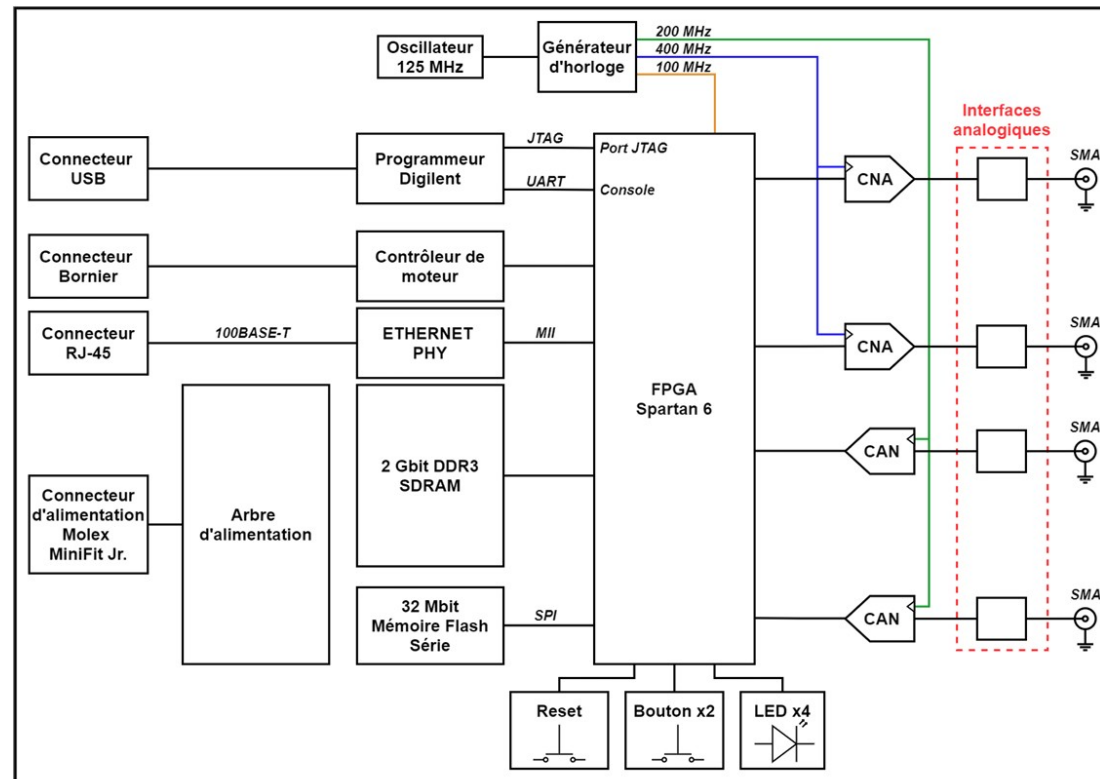
**18**

Filename

S7CAS-PLEIADES-CARTE-MERE\_P06\_TITLE.SchDoc

Designers

**Étienne Provencher**  
**Antoine Allard**



**Figure 2 :** Diagramme fonctionnel de la carte *Pléiades*

Sheet Name		<b>BLOCK DIAGRAM</b>	
Project Title		<b>S7CAS-PLEIDES-CARTE-MERE_P06</b>	
Global Project		<b>S7APP1-2</b>	
Size	Group	Revision	
<b>11x17</b>	<b>Dream Team</b>	<b>1.00</b>	
Date	<b>2026-01-21</b>	Sheet	<b>2 of 18</b>
Filename		Designers	
<b>S7CAS-PLEIADES-CARTE-MERE_P06_BLOCK_DIAGRAM.SchDoc</b>		<b>Etienne Provencher Antoine Allard</b>	

24V External PSU or Battery		
V	I	
24 V	4.73 A	
P		
113.52 W		

LMZ23605TZE 1		
SWR	eff	
	87 %	
Max current : 5A		
Vin	Vout	
24V	5.81V	
Iin	Iout	
0.92A	3.32A	
Pin	Pdis	Pout
22.17W	2.88W	19.29W

PTH08T241WAZ 1		
SWR	eff	
	92%	
Max current : 10A		
Vin	Vout	
5.81V	3.6V	
Iin	Iout	
2.37A	3.52A	
Pin	Pdis	Pout
13.78W	1.1W	12.68W

PTN04050AAZT 1		
SWR	eff	
	61%	
Max current : 1A		
Vin	Vout	
5.81V	-5.5V	
Iin	Iout	
0.056A	0.056A	
Pin	Pdis	Pout
0.49W	0.19W	0.3W

TPS7A3301RGWR 2		
LDO	eff	
	94%	
Max current : 1A		
Vin	Vout	
-5.5V	-5V	
Iin	Iout	
0.056A	0.056A	
Pin	Pdis	Pout
0.30 W	0.02W	0.28W

TPS7A4701RGWR 2		
LDO	eff	
	86%	
Max current : 1A		
Vin	Vout	
5.81V	5V	
Iin	Iout	
0.056A	0.056A	
Pin	Pdis	Pout
0.33W	0.05W	0.28W

NCP59744MN1ADJ 2		
LDO	eff	
	92%	
Max current : 3A		
Vin	Vout	
3.6V	3.3V	
Iin	Iout	
1.436A	1.436A	
Pin	Pdis	Pout
5.25W	0.43W	4.74W

NCP59744MN1ADJ 1		
LDO	eff	
	92%	
Max current : 3A		
Vin	Vout	
3.6V	3.3V	
Iin	Iout	
0.025A	0.025A	
Pin	Pdis	Pout
0.091W	0.008W	0.083W

NCP59744MN1ADJ 2		
LDO	eff	
	92%	
Max current : 3A		
Vin	Vout	
3.6V	3.3V	
Iin	Iout	
0.585A	0.585A	
Pin	Pdis	Pout
2.11W	0.18W	1.93W

NCP59744MN1ADJ 2		
LDO	eff	
	50%	
Max current : 3A		
Vin	Vout	
3.6V	1.8V	
Iin	Iout	
0.596A	0.596A	
Pin	Pdis	Pout
2.04W	1.02W	1.02W

NCP59744MN1ADJ 2		
LDO	eff	
	42%	
Max current : 3A		
Vin	Vout	
3.6V	1.5V	
Iin	Iout	
0.482A	0.482A	
Pin	Pdis	Pout
1.73W	1.01W	0.72W

MAX1502ATB+T 2		
LDO	eff	
	21%	
Max current : 1A		
Vin	Vout	
3.6V	0.75V	
Iin	Iout	
0.429A	0.429A	
Pin	Pdis	Pout
1.543W	1.223W	0.32W

LMZ23605TZE 1		
SWR	eff	
	71%	
Max current : 5A		
Vin	Vout	
5.81V	1.2V	
Iin	Iout	
0.87A	3A	
Pin	Pdis	Pout
5.07W	1.47W	3.6W

24V		
V	I	
24 V	3.810 A	
P		
91.44 W		

-5V		
V	I	
-5 V	0.056 A	
P		
0.28 W		

5V		
V	I	
5 V	0.056 A	
P		
0.28 W		

3V3D		
V	I	
3.3 V	1.436 A	
P		
4.74 W		

3V3FLASH		
V	I	
3.3 V	0.025 A	
P		
0.083 W		

3V3A		
V	I	
3.3 V	0.585 A	
P		
1.93 W		

1V8D		
V	I	
1.8 V	0.566 A	
P		
1.02 W		

1V5D		
V	I	
1.5 V	0.482 A	
P		
0.72 W		

VTTDDR (0.75V)		
V	I	
0.75 V	0.429 A	
P		
0.32 W		

1V2D		
V	I	
1.2 V	3 A	
P		
3.6 W		

Total Load : 104.41 W  
Total Regulated Load : 12.97 W

-Sequence :  
-Flash  
-Autre

Total Global Power Tree Efficiency :

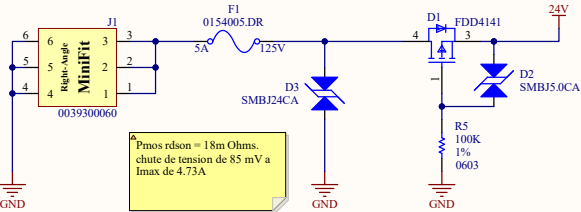
104.41 / 113.52 = 92%

Regulated global Power Tree Efficiency :

12.97 / 22.08 = 58.7%

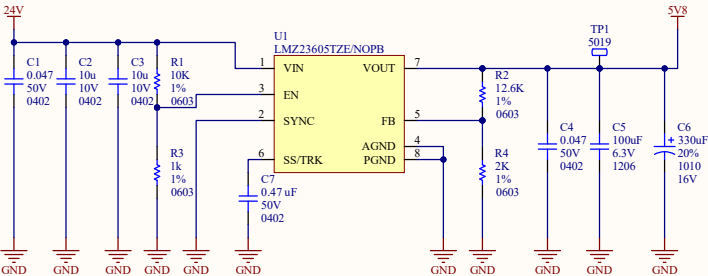
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POWER TREE			
Project Title			
S7CAS-PLEIDES-CARTE-MERE_P06			
Global Project			
S7APP1-2			
Size	Group	Revision	
11x17	Dream Team	1.00	
Date	Sheet	of	
2026-01-21	3	18	
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P06_POWER_TREE.SchDoc		Etienne Provencher Antoine Allard	

Power input & Protections



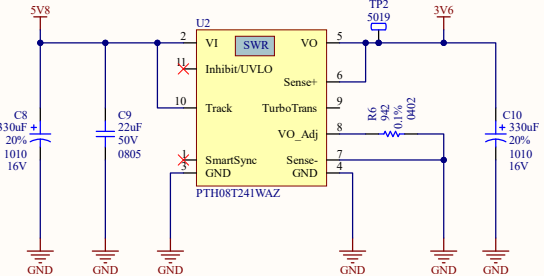
4.73 A @ 24V

Bucks 24V à 5.8V



3.39 A @ 5.81V

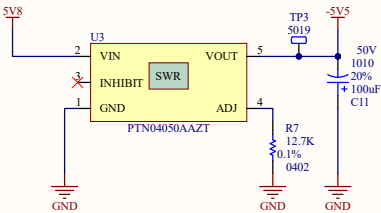
Bucks 5.8 à 3.6



2.37 A @ 5.8V

3.52 A @ 3.6V

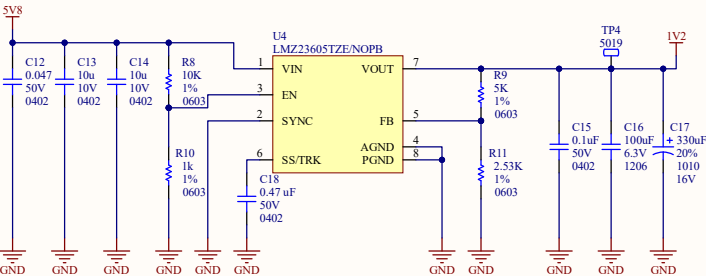
Bucks 5.8 à -5.5



0.084 A @ 5.8V

0.056 A @ -5.5V

Bucks 5.8V à 1.2V



0.87 A @ 5.8V

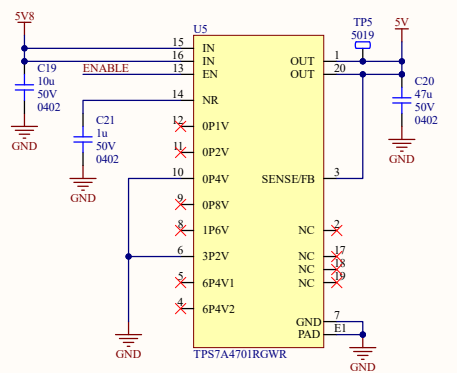
3 A @ 1.2V

Power table										
Sheet	Absolute maximum									
	Current @ 24V	Current @ 5V	Current @ -5V	Current @ 3V3D	Current @ 3V3FLASH	Current @ 3V3A	Current @ 1V8D	Current @ 1V5D	Current @ 1V2D	Current @ VTDDR (0.75V)
FPGA1	0 mA	0 mA	0 mA	0.1 A	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FPGA2	0 mA	0 mA	0 mA	0.05 A	0 mA	0 mA	0 mA	0.3 A	0 mA	0 mA
FPGA3	0 mA	0 mA	0 mA	0.15 A	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FPGA4	0 mA	0 mA	0 mA	0.25 A	0 mA	0 mA	0 mA	0 mA	3 A	0 mA
CLOCK	0 mA	0 mA	0 mA	690 mA	0 mA	175 mA	0 mA	0 mA	0 mA	0 mA
ETHERNET	0 mA	0 mA	0 mA	28 mA	0 mA	34 mA	0 mA	0 mA	0 mA	0 mA
DDR3	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA	182 mA	0 mA	429 mA	0 mA
MISC	10 mA	0 mA	0 mA	42 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
MOTOR	3.8 A	0 mA	0 mA	4 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
FLASH	0 mA	0 mA	0 mA	0 mA	25 mA	0 mA	0 mA	0 mA	0 mA	0 mA
ADC	0 mA	43.2 mA	43.2 mA	0 mA	0 mA	320 mA	165 mA	0 mA	0 mA	0 mA
DAC	0 mA	13.3 mA	13.3 mA	0 mA	0 mA	56 mA	401 mA	0 mA	0 mA	0 mA
USB_PROG	0 mA	0 mA	0 mA	122 mA	0 mA	0 mA	0 mA	0 mA	0 mA	0 mA
Total	3.810 A	0.056 A	0.056 A	1.436 A	0.025 A	0.585 A	0.566 A	0.482 A	3.000 A	0.429 A

Sheet Name		<b>POWER 1</b>	
Project Title		<b>S7CAS-PLEIDES-CARTE-MERE_P06</b>	
Global Project		<b>S7APP1-2</b>	
Size	Group	Revision	
11x17	Dream Team	1.00	
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Filename		Designers	
S7CAS-PLEIADDES-CARTE-MERE_P06_POWER1.SCHDOC		Etienne Provencher Antoine Allard	

Figure 24. Typical Application,  $V_{OUT} = 3.3\text{ V}$

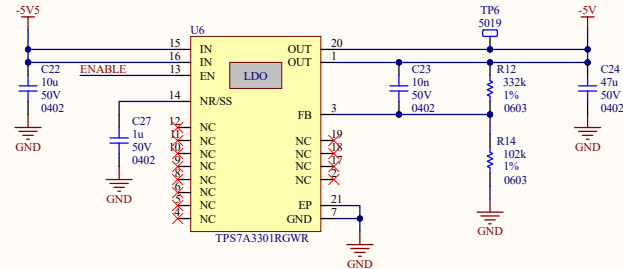
### 5V Generation



0.056 A @ 5.81V

0.056 A @ 5V

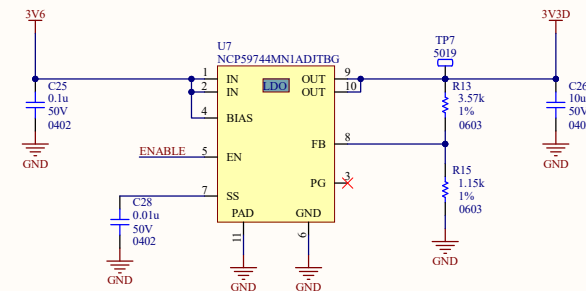
### -5V Generation



0.056 A @ -5.5V

0.056 A @ -5V

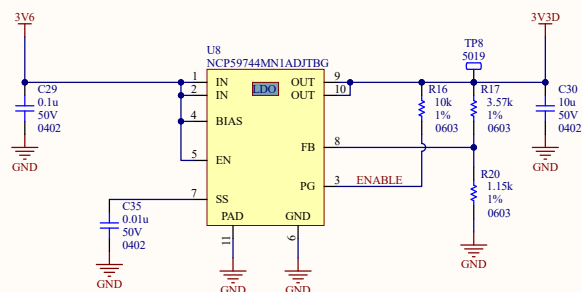
### 3V3D Generation



1.436 A @ 3.6V

1.436 A @ 3.3V

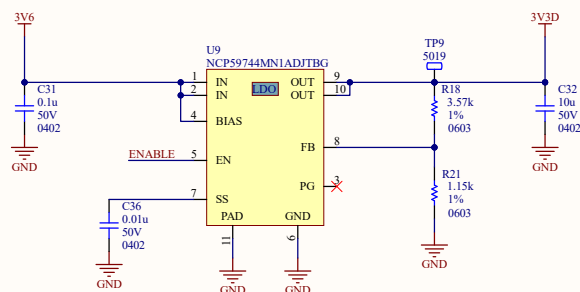
### 3V3FLASH Generation



0.025 A @ 3.6V

0.025 A @ 3.3V

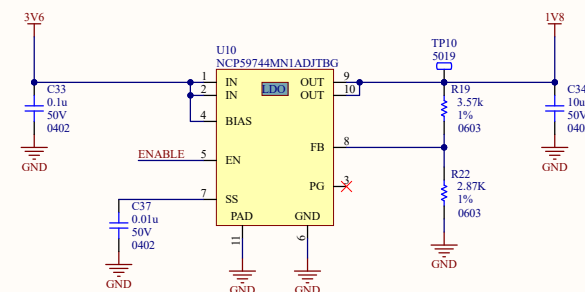
### 3V3A Generation



0.585 A @ 3.6V

0.585 A @ 3.3V

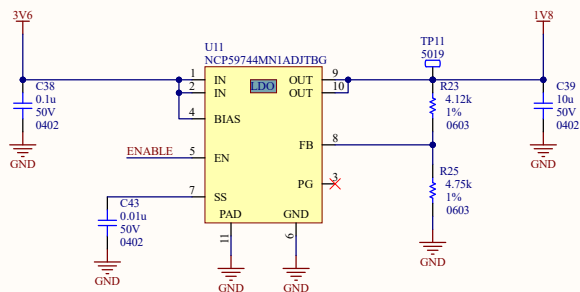
### 1V8D Generation



0.566 A @ 3.6V

0.566 A @ 1.8V

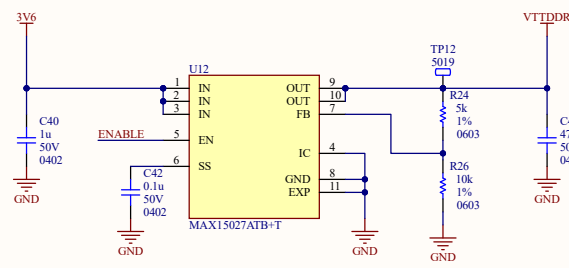
### 1V5D Generation



0.482 A @ 3.6V

0.482 A @ 1.5V

### VTDDR (0.75V) Generation



0.429 A @ 3.6V

0.482 A @ 0.75V

Sheet Name

**POWER 2**

Project Title

**S7CAS-PLÉIDES-CARTE-MERE\_P06**

Global Project

**S7APP1-2**

Size

**11x17**

Group

**Dream Team**

Revision

**1.00**

Date

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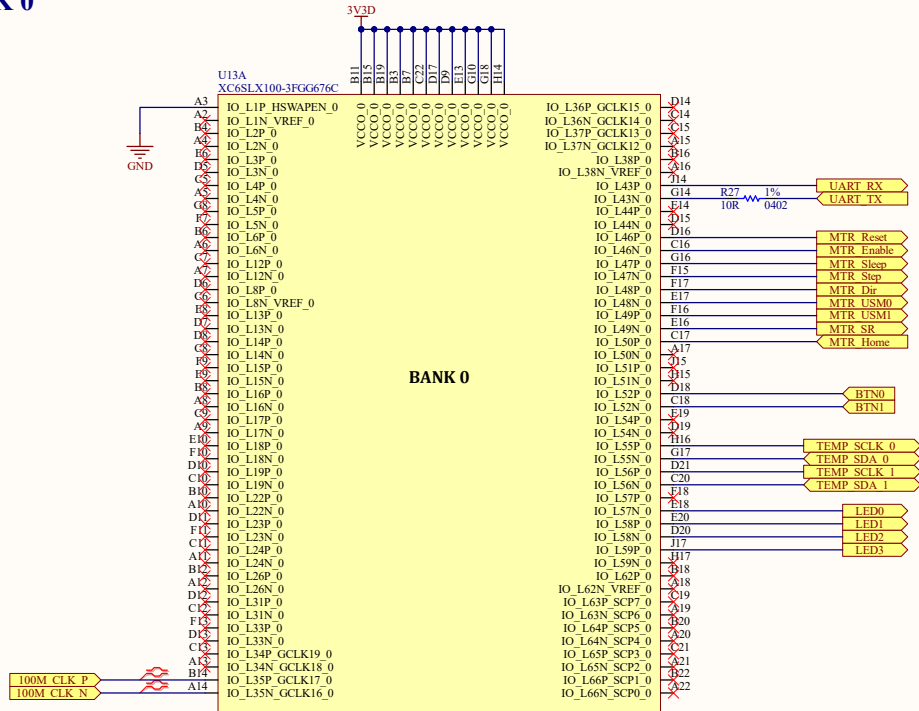
Filename

S7CAS-PLÉIDES-CARTE-MERE\_P06\_POWER2.SCHDOC

Designers

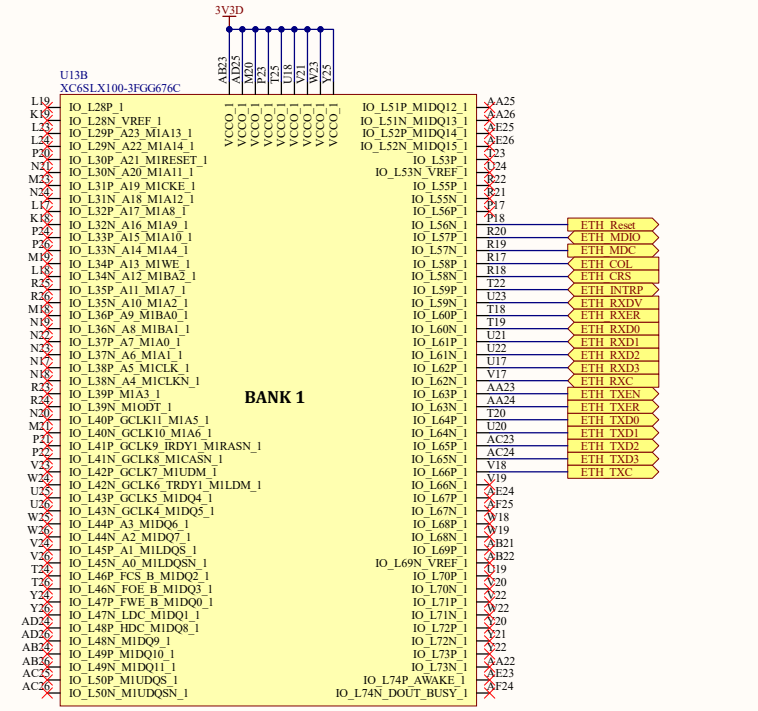
Étienne Provencher  
Antoine Allard

## BANK 0



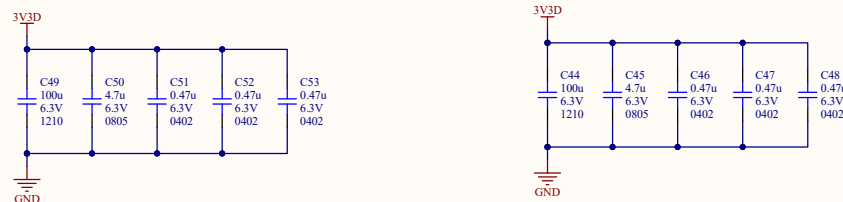
0.05A @ 3V3D

## BANK 1



0.05A (3V3D)

## Découplage Bank0 et Bank1

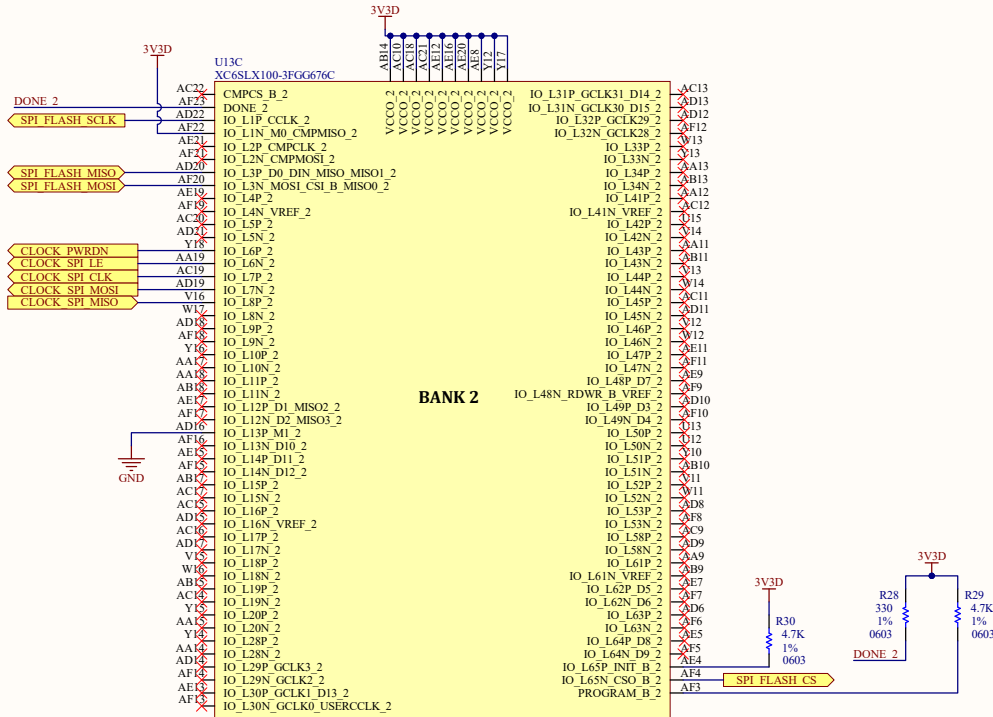


Sheet Name		FPGA1	
Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size	Group	Revision	
11x17	Dream Team	1.00	
Date	2026-01-21	Sheet	6 of 18
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P06_FPGA1.SCHDOC		Etienne Provencher Antoine Allard	

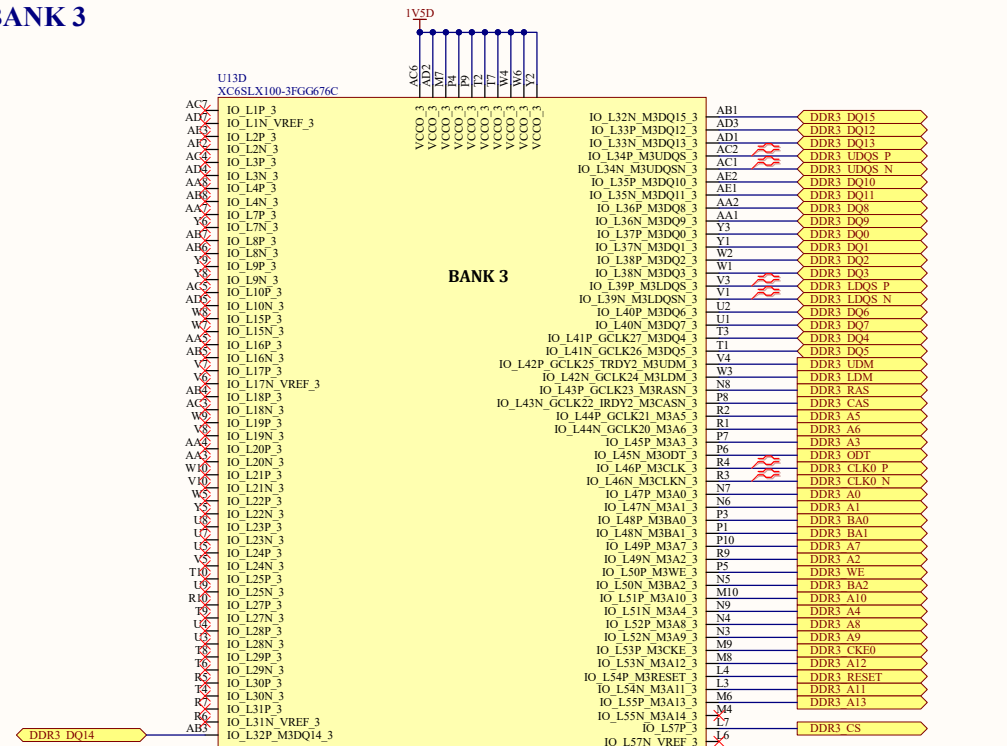
Table 2-1: Required PCB Capacitor Quantities per Device<sup>(1)(3)</sup> (Continued)

Table 2-2: PCB Capacitor Specifications

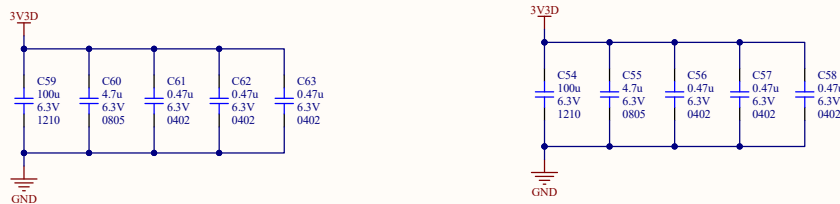
## BANK 2



## BANK 3



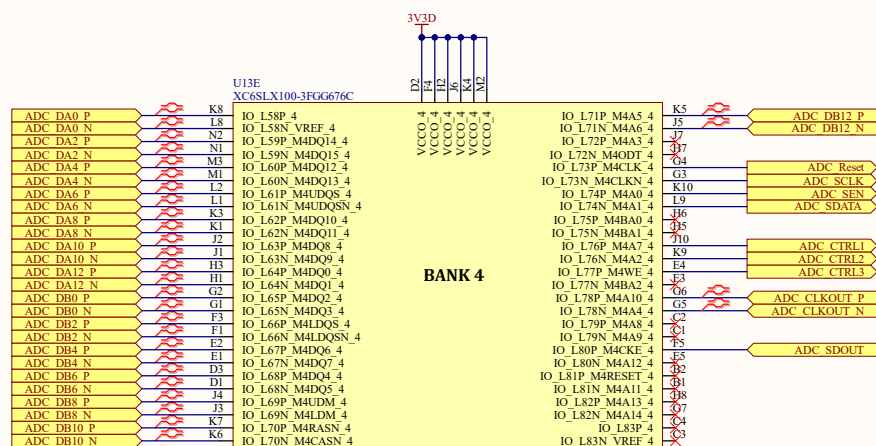
## Découplage Bank2 et Bank3



Sheet Name		FPGA2	
Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size	Group	Revision	
11x17	Dream Team	1.00	
Date	2026-01-21	Sheet	7 of 18
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P06_FPGA2.SCHDOC		Etienne Provencher Antoine Allard	

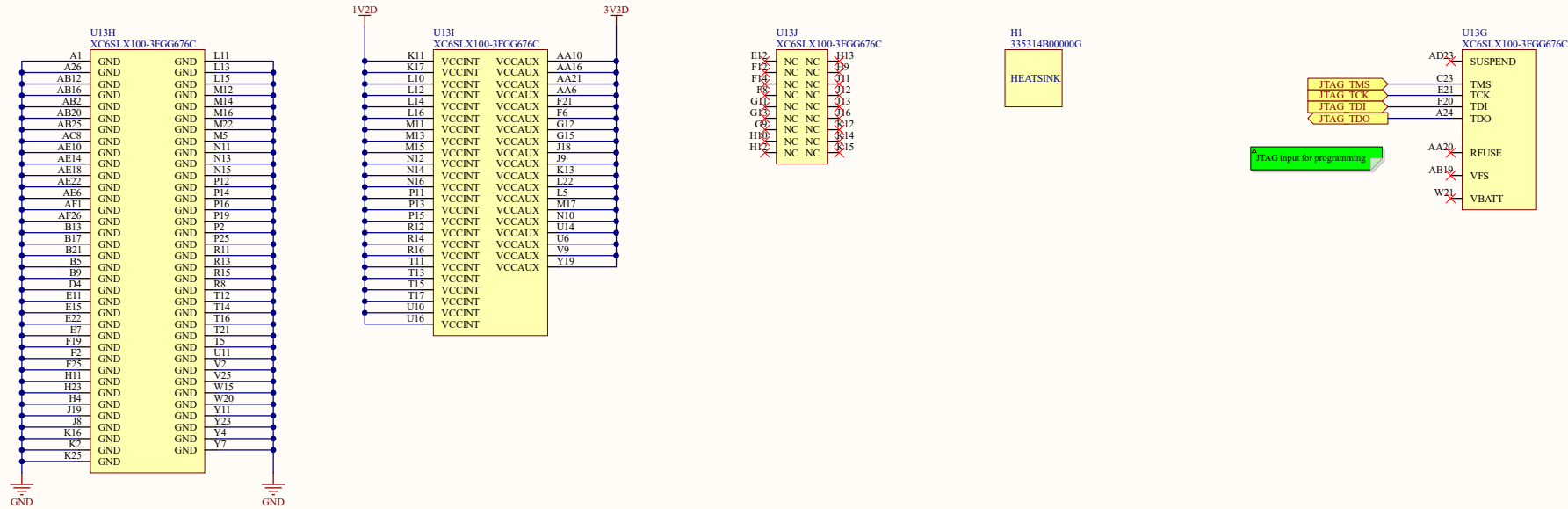
Table 2-1: Required PCB Capacitor Quantities per Device<sup>(1)(3)</sup> (Continued)

Table 2-2: PCB Capacitor Specifications

[illegible]

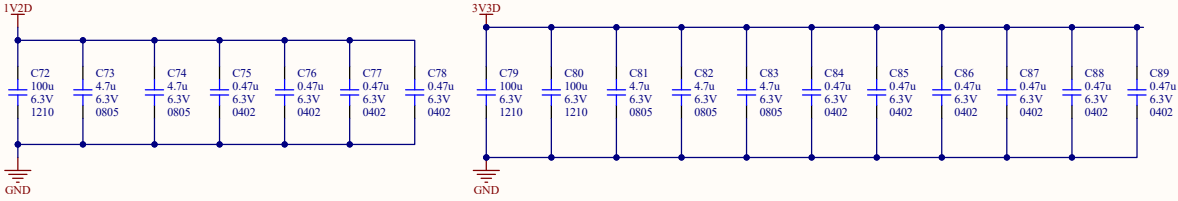


FPGA Power and JTAG



3A @ 1V2D  
0.25A @ 3V3D

Découplage général FPGA



Sheet Name		FPGA4	
Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size	Group	Revision	
11x17	Dream Team	1.00	
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Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P06_FPGA4.SCHDOC		Etienne Provencher Antoine Allard	

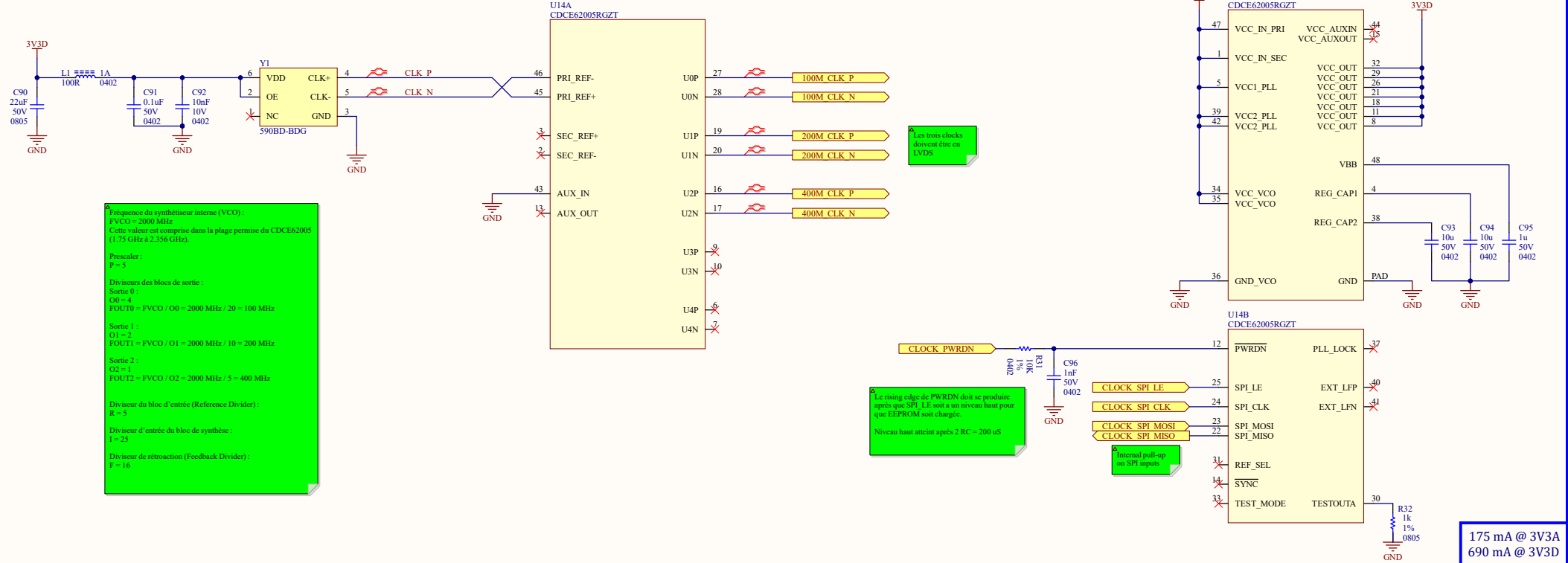
Table 2-1: Required PCB Capacitor Quantities per Device<sup>(1)(3)</sup> (Continued)

	V	V	V <sub>CC0</sub>	V <sub>CC0</sub>	V <sub>CC0</sub>	V <sub>CC0</sub>	V <sub>CC0</sub>	V <sub>CC0</sub>	V <sub>CC0</sub>
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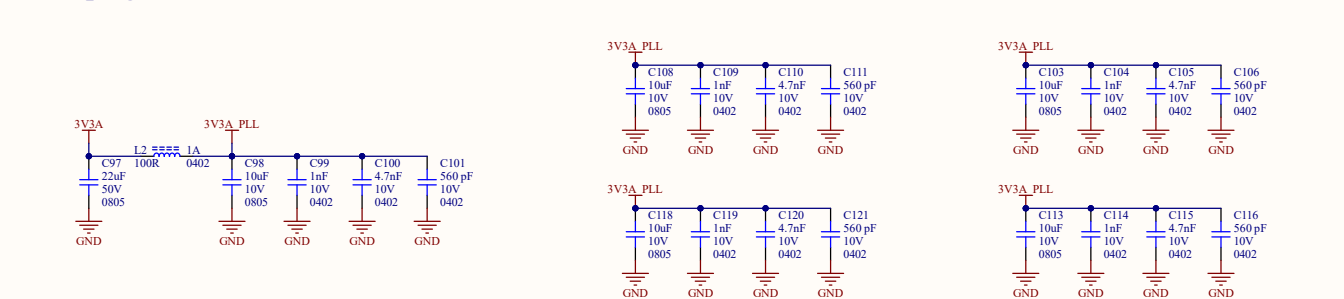
Table 2-2: PCB Capacitor Specifications

	Ideal	Value	Body		ESL		Voltage	Suggested
--	-------	-------	------	--	-----	--	---------	-----------

## Clock



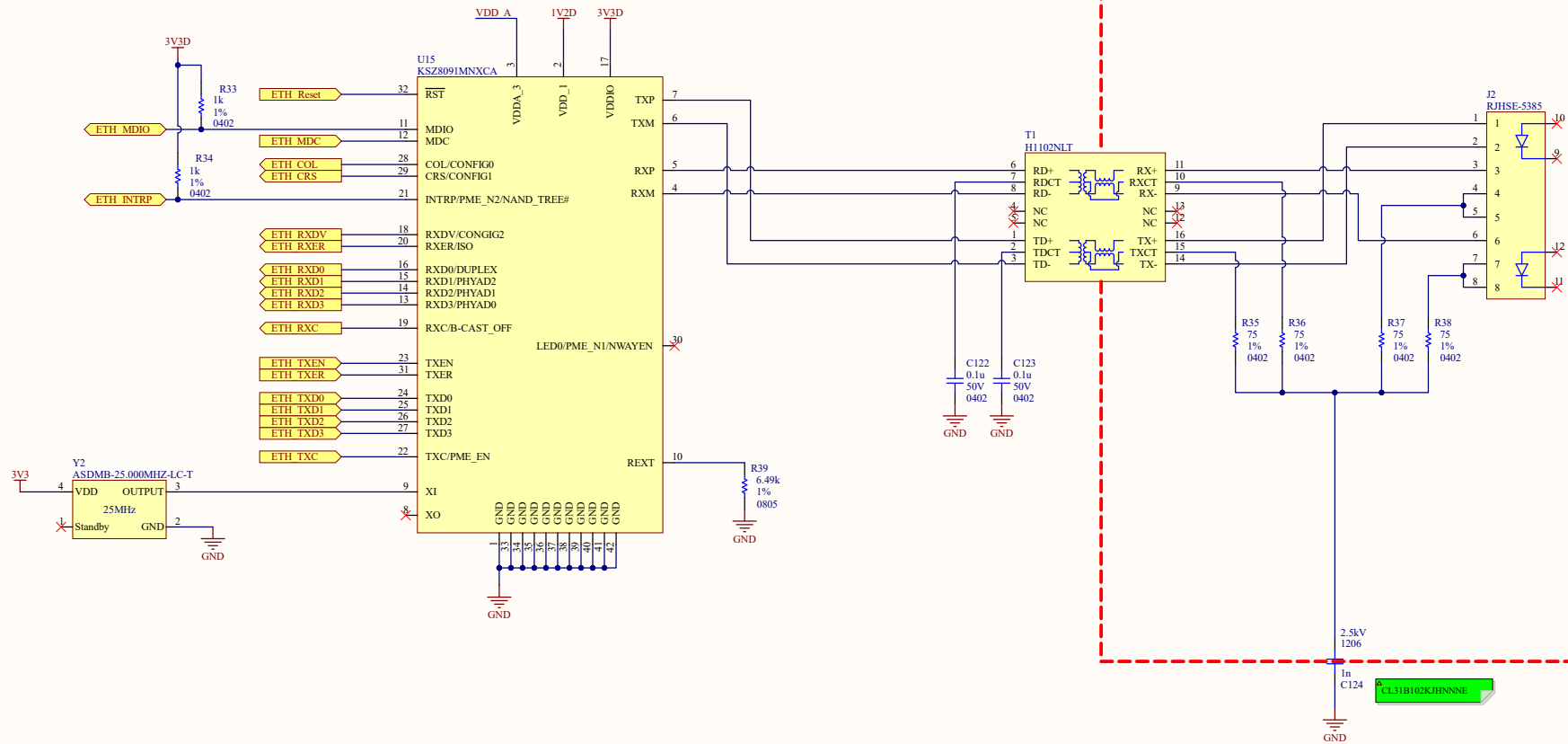
## Découplage Clock & Filtre



Sheet Name			
CLOCK			
Project Title			
S7CAS-PLEIDES-CARTE-MERE_P06			
Global Project			
S7APP1-2			
Size	Group		Revision
11x17	Dream Team		1.00
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S7CAS-PLEIADES-CARTE-MERE_P06_CLOCK.SchDoc		Étienne Provencher Antoine Allard	

Assuming a 3.3-V board supply, the ferrite bead maximum dc resistance for each VCC\_PLL can be 3 Ω; for each VCC\_IN, the resistance can be 12 Ω each; for VCC\_VCO, the resistance can be 6 Ω each; and

## Ethernet



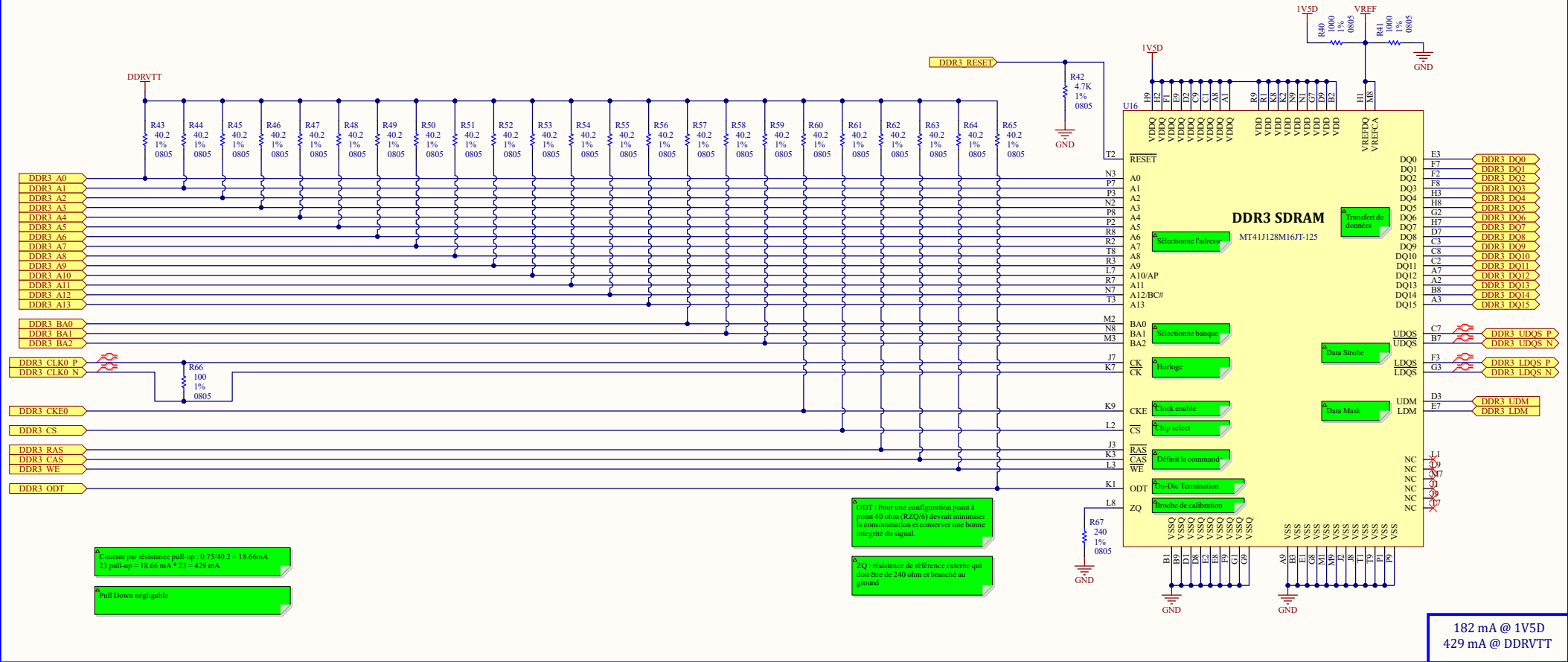
## Découplage Ethernet et filtres



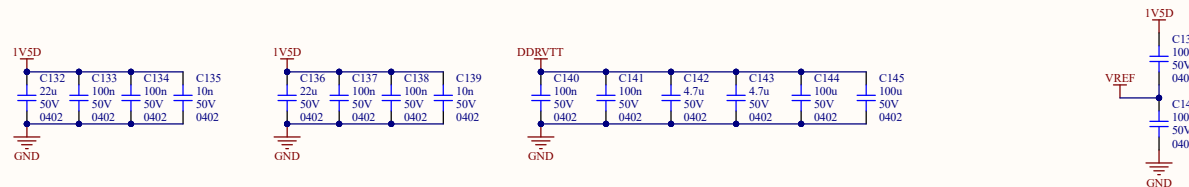
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ETHERNET			
Project Title			
S7CAS-PLEIDES-CARTE-MERE_P06			
Global Project			
S7APP1-2			
Size	Group		Revision
11x17	Dream Team		1.00
Date	2026-01-21	Sheet 11 of 18	
Filename			Designers
S7CAS-PLEIADES-CARTE-MERE_P06_ETHERNETSCHDOC			Etienne Provencher Antoine Allard

'CK (MIN)	Average period between cycle time	1.25	ns
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## DDR3

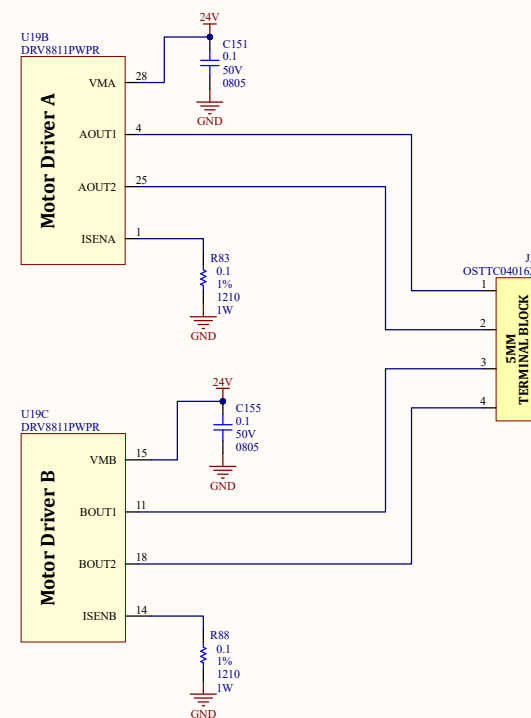
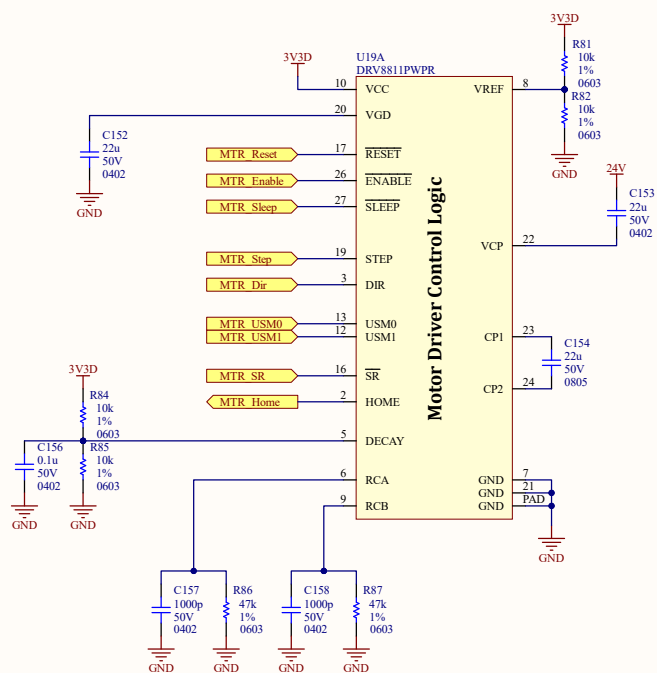


## Découplage DDR3



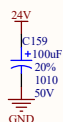
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Project Title				<b>S7CAS-PLEIDES-CARTE-MERE_P06</b>	
Global Project				<b>S7APP1-2</b>	
Size	11x17	Group	Dream Team		Revision
Date	2026-01-21	Sheet	12	of	18
Filename				Designers	
S7CAS-PLEIDES-CARTE-MERE_P06_DDR3.SCHDOC				Étienne Provencher Antoine Allard	

## MOTEUR



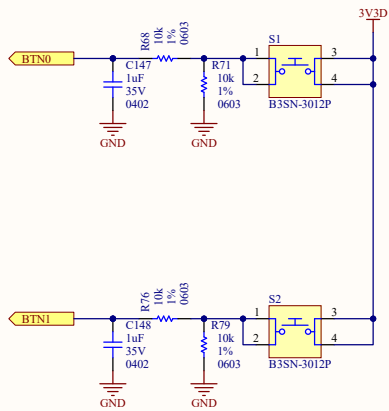
3.8 A @ 24V  
4 mA @ 3V3D

## Découplage MOTEUR

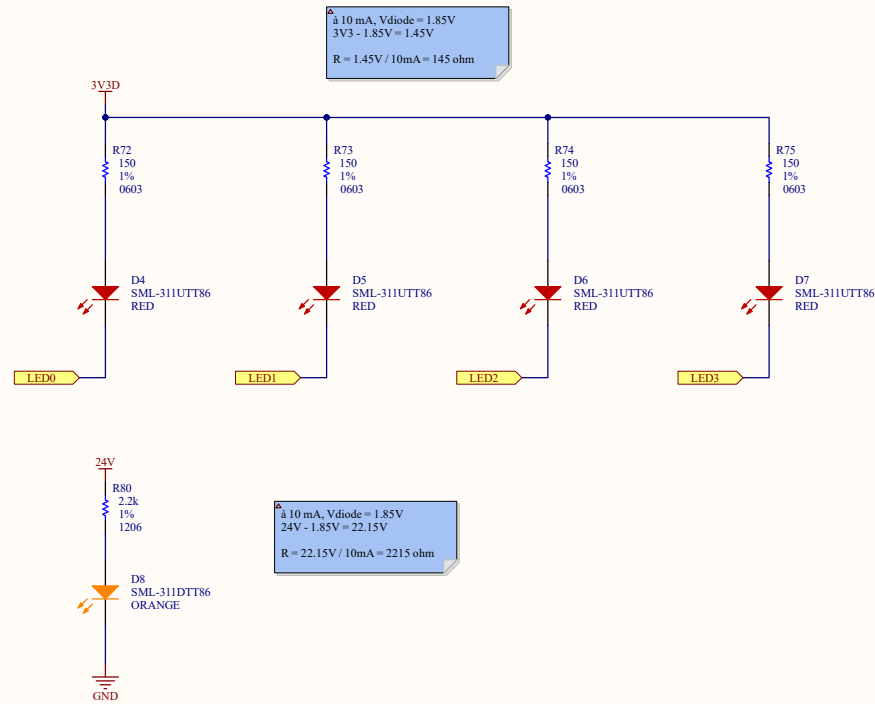


Sheet Name		<b>MOTOR</b>	
Project Title		<b>S7CAS-PLEIDES-CARTE-MERE_P06</b>	
Global Project		<b>S7APP1-2</b>	
Size	Group	Revision	
<b>11x17</b>	<b>Dream Team</b>	<b>1.00</b>	
Date	Sheet		
<b>2026-01-21</b>	<b>13</b>	<b>of 18</b>	
Filename		Designers	
<b>S7CAS-PLEIADES-CARTE-MERE_P06_MOTOR.SCHDOC</b>		<b>Etienne Provencer Antoine Allard</b>	

## Buttons



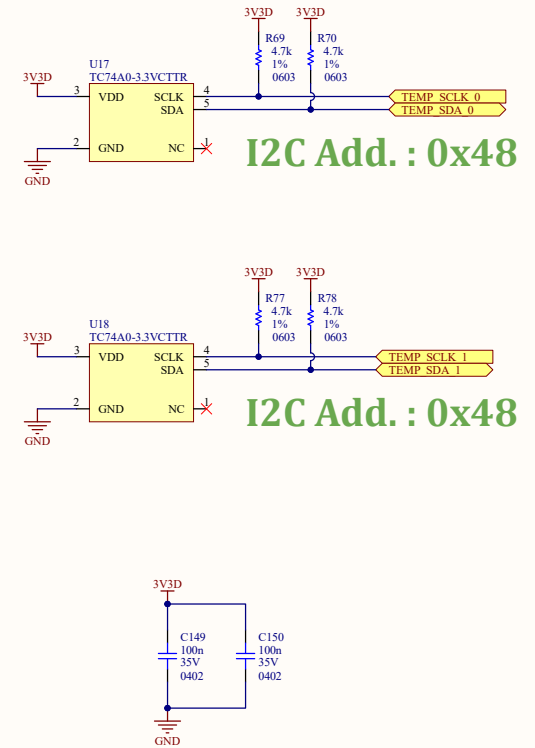
## LEDS



Each LVCMOS and LVTTTL output additionally supports up to seven different drive current strengths as shown in Table 1-2. To adjust the drive strength for each output, the DRIVE attribute is set to the desired drive strength: 2, 4, 6, 8, 12, 16, and 24. Unless otherwise specified in the FPGA application, the software default for IOSTANDARD is LVCMOS25, SLOW slew rate, and 12 mA output drive.

40 mA @ 3V3D  
10mA @ 24V

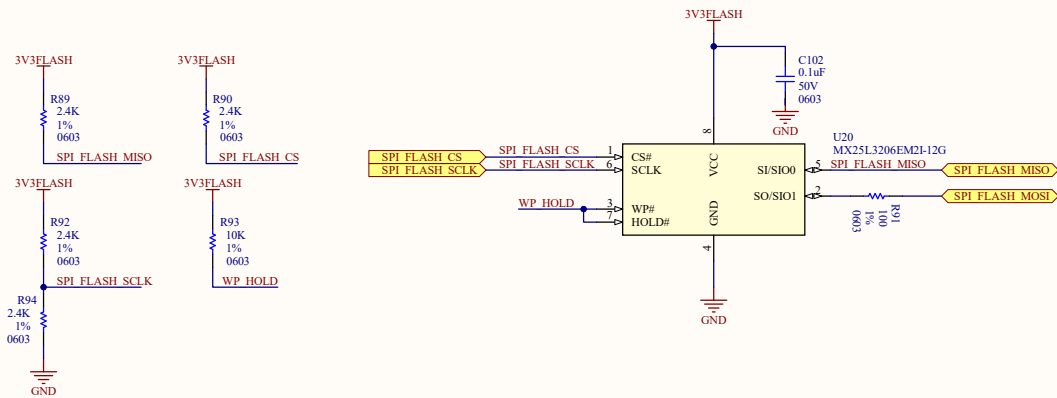
## Temp sensors



La carte doit contenir 3 boutons-poussoirs (Reset FPGA et 2 entrées au FPGA), 4 DEL servant au déverminage du FPGA, une DEL indiquant que l'alimentation 24 V est fonctionnelle ainsi que 2 senseurs de température de type TC74.

Sheet Name		MISC	
Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size	Group	Revision	
11x17	Dream Team	1.00	
Date		Sheet	of
2026-01-21		14	18
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P06_MISC.SchDoc		Etienne Provencher Antoine Allard	

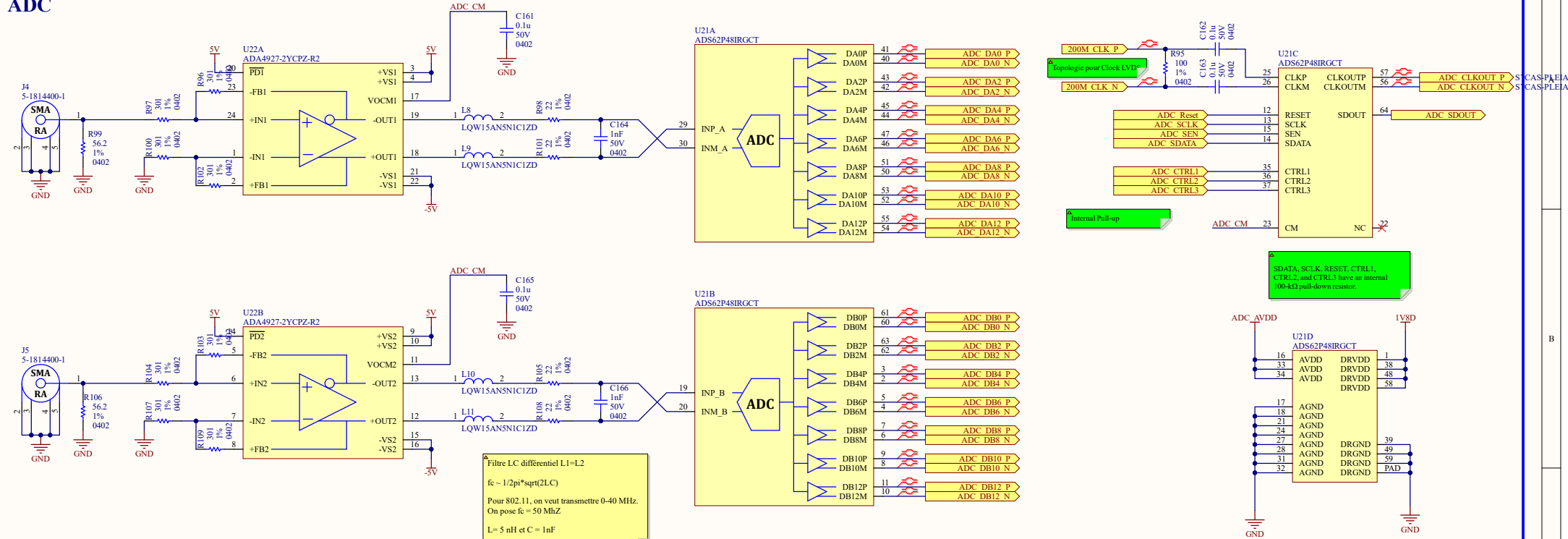
FLASH



25 mA @ 3V3D

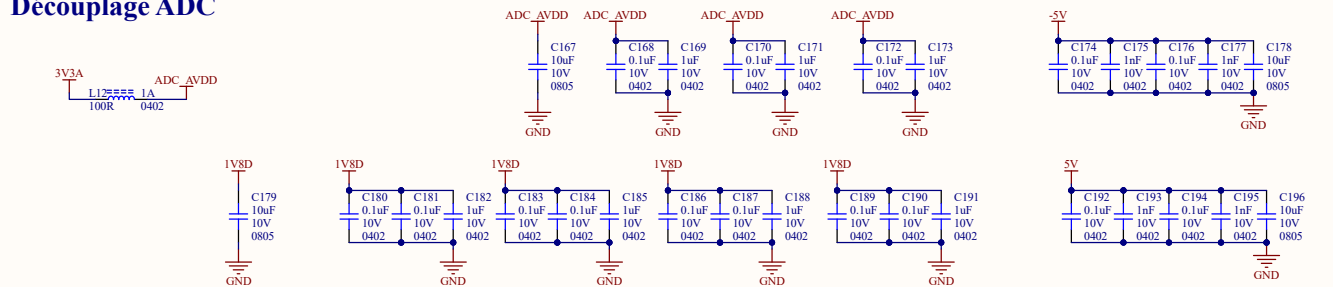
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Global Project		S7APP1-2	
Size	Group	Revision	
11x17	Dream Team	1.00	
Date	2026-01-21	Sheet	15 of 18
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P06_FLASH.SCHDOC		Étienne Provencher Antoine Allard	

## ADC



165 mA @ 1V8D  
320 mA @ 3V3A  
43.2 mA @ 5V  
43.2 mA @ -5V

## Découplage ADC



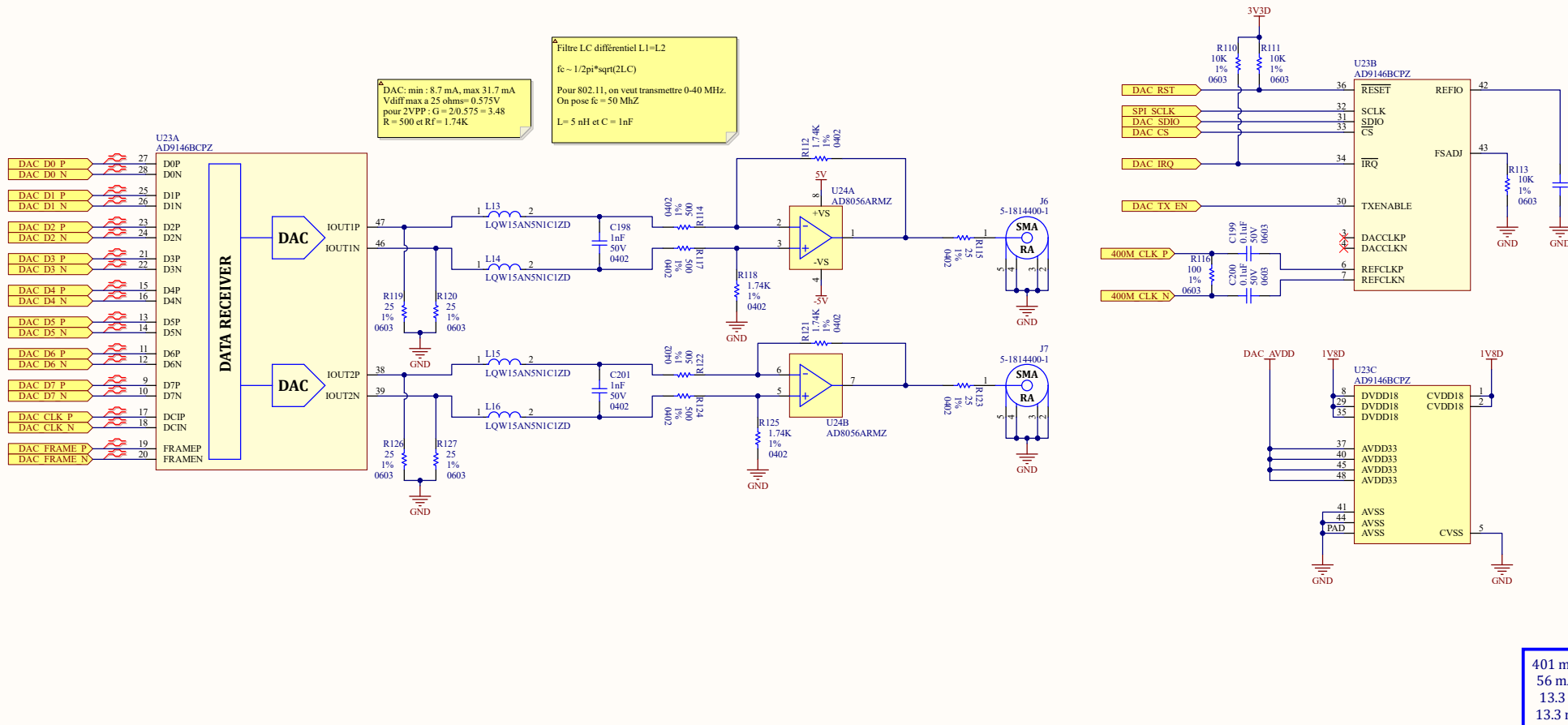
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Project Title		<b>S7CAS-PLEIDES-CARTE-MERE_P06</b>	
Global Project		<b>S7APP1-2</b>	
Size	11x17	Group	Dream Team
Date	2026-01-21	Sheet	16 of 18
Filename		S7CAS-PLEIADES-CARTE-MERE_P06_ADC.SchDoc	
Designers		Étienne Provencher Antoine Allard	

### Supply Decoupling

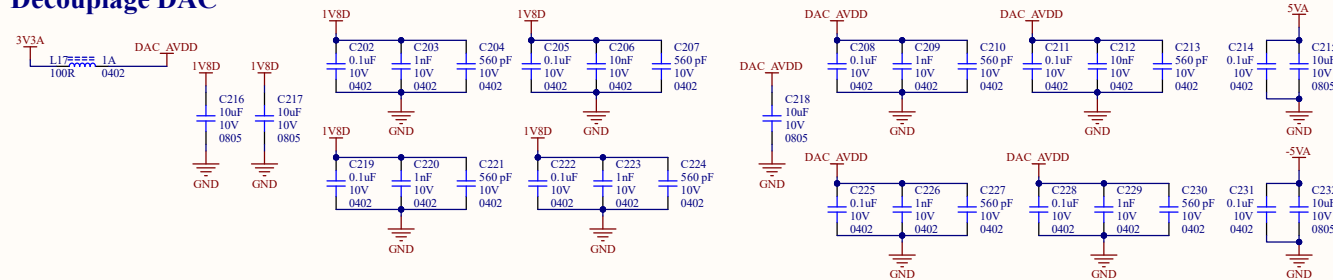
As ADS62Px9/x8 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum



# DAC

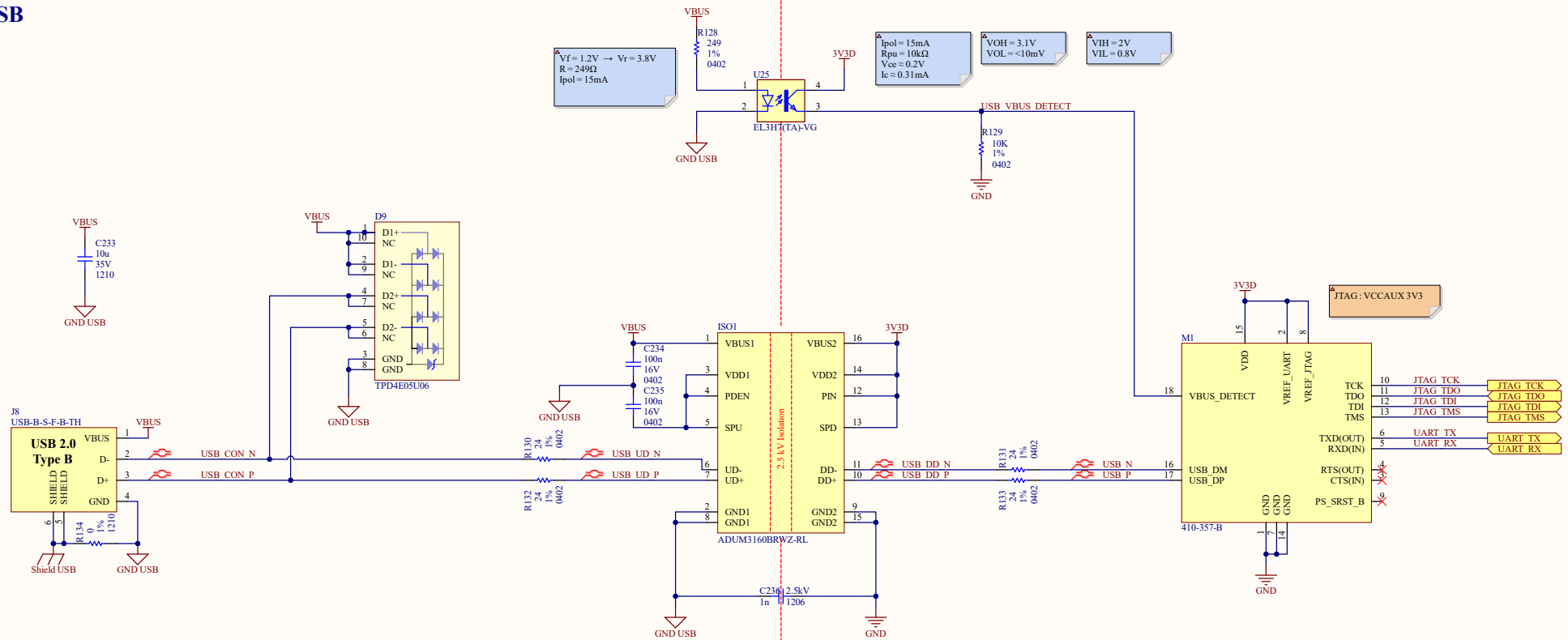


## Découplage DAC



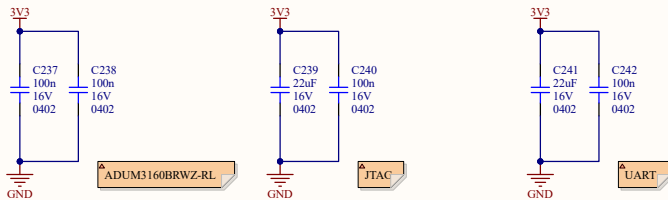
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Global Project		S7APP1-2	
Size	Group	Revision	
11x17	Dream Team	1.00	
Date	2026-01-21	Sheet	17 of 18
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P06_DAC.SchDoc		Etienne Provencher Antoine Allard	

## USB



122 mA @ 3V3

## Découplage USB



Sheet Name		USB_PROGRAMMER	
Project Title		S7CAS-PLEIDES-CARTE-MERE_P06	
Global Project		S7APP1-2	
Size	Group	Revision	
11x17	Dream Team	1.00	
Date	2026-01-21	Sheet	18 of 18
Filename		Designers	
S7CAS-PLEIADES-CARTE-MERE_P06_USB_PROGRAMER.SCHDOC		Etienne Provencher Antoine Allard	