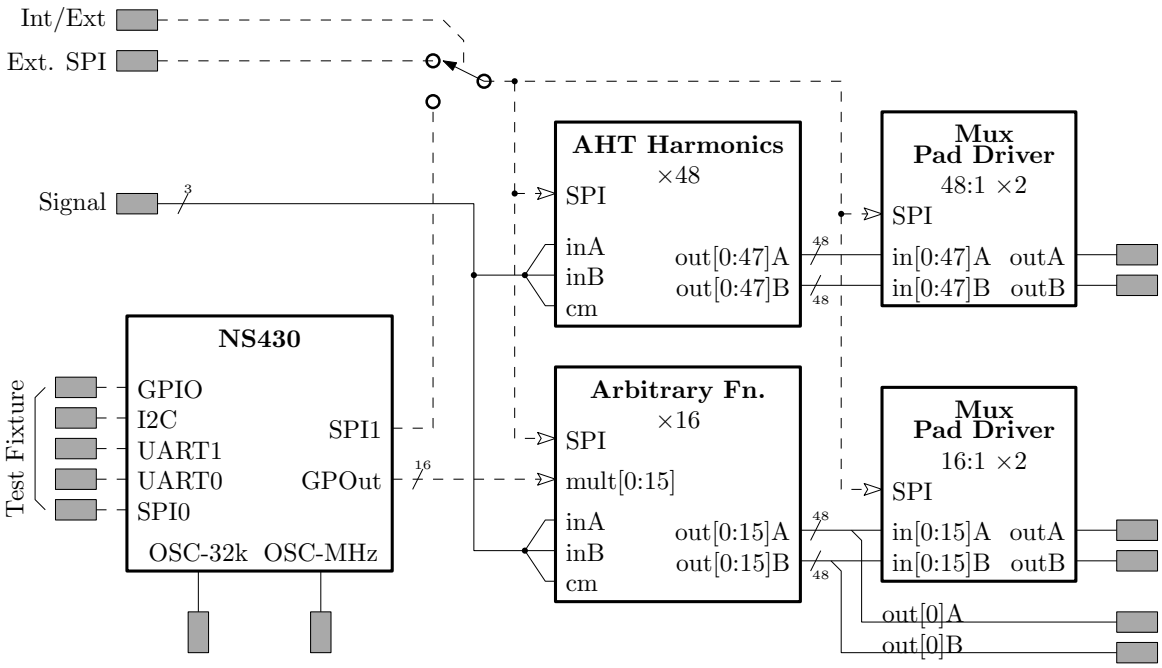

Figure 4.2: Prototype chip block diagram and internal interconnections. Filled rectangles represent functional pads for connecting signals on/off-chip, not necessarily individual package pins. Dashed lines are digital signals for control and basis functions while solid lines are analog signal paths.

4.3 Prototype chip architecture

A prototype chip was created to evaluate the hardware-level performance of the AHT system, its sub-parts had several features to enable testing. A functional block view of the chip is shown in Figure 4.2.

A 0.13 µm mixed-signal CMOS process from IBM, "8RF," was used for the prototype. The initial part of the design effort was to update the UNL Advanced Chip Design Group's portfolio of capabilities to include this process. Prior to this project, the most advanced process available for research prototyping was the previous-generation IBM 0.18 µm CMOS process, "7RF."

Critical to configuring the software environment for the new process design kit

(PDK) was verifying the proper setup to integrate both full-custom schematic and hand layout with an automated digital design flow. Some differing conventions between the full-custom and digital portions of the PDK were un-documented and found to be in error. These errors were fixed to bring the PDK configuration in line with IBM's master process documentation.

Finally, the design rule checking scripts provided in the PDK were inconsistent with the published design rules. One such configuration error caused the digital design flow to generate artwork guaranteed to fail the design rule checks. Another necessary change was the addition of rules to properly check layouts which included black-box intellectual property (IP) cells whose complete layout was not available.

After the PDK setup and validation with this project, the IBM "8RF" process is available for other advanced prototype chip designs. For example, this accelerated the design of the "PIRANHA" imager with focal-plane digital processing. This design is inherently an analog/digital hybrid and therefore required a PDK with consistent and correct checking and setup.

The core of the design is the "AHT Harmonics" block which contains a parallel bank of 48 quadrature harmonic paths. These, and the other bank, share a common differential input, *inA / inB*, and common-mode input, *cm*. The architecture and design of this module is described in later Sections 4.4, 4.5, and 4.6. Analog coefficient signal outputs from each of the integrators is applied to a multiplexer and buffered by a pad driver for off-chip measurements.

A second bank of 16 projection channels is included as "Arbitrary Fn." For these channels, the internal digital NCO basis function generator is disconnected from the multiplier. The multiplier inputs are provided from the on-chip micro-

processor to use arbitrary ±1 functions besides the AHT's 50% duty-cycle quadrature square waves. Also, two of the integrator outputs are routed to both the multiplexer and directly to pads. This allows observation signals before the multiplexer, bypassing the pad drivers.

Block "NS430" is a custom micro-processor which is code-compatible with the TI MSP430 family of commercial micro-controllers. Through a switch, it can control the rest of the chip via SPI, a serial data connection. Section 4.7 describes the processor in more detail.

4.4 AHT System Architecture

Figure 4.3 shows the AHT system architecture implemented in the hardware, first shown in Figure 3.6. The basis function projection blocks represent the majority of the system design work. For the prototype, the Input Amplifier and signal preprocessing functions are performed off-chip and the Main Control is implemented in software with a serial communication link to the controlled projection blocks.

4.5 Basis Function Projection

Each quadrature projection section consists of a local digital block and two identical multiply-integrate channels. The digital section uses the 1.2 V nominal digital supply while the channels operate from the 2.5 V nominal analog supply rail. Logical control signals cross the boundary through a level translator block.

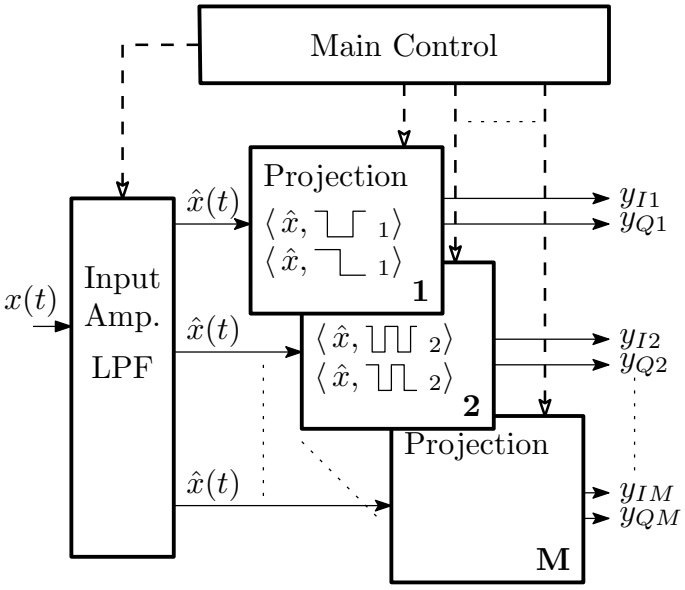

Figure 4.3: Analog projection system block diagram. The Input Amplifier and low-pass filter (LPF) block is not integrated into the prototype chip but is provided by the test fixture.

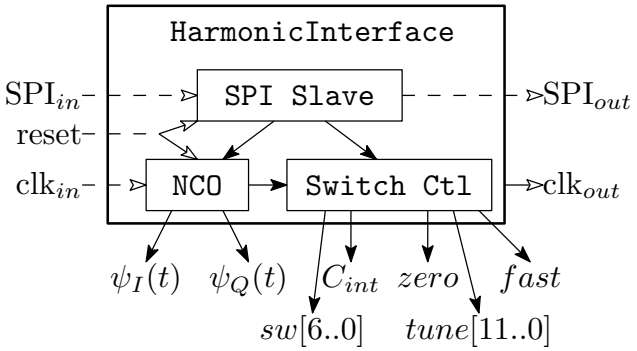

Figure 4.4: Quadrature harmonic projection digital architecture.

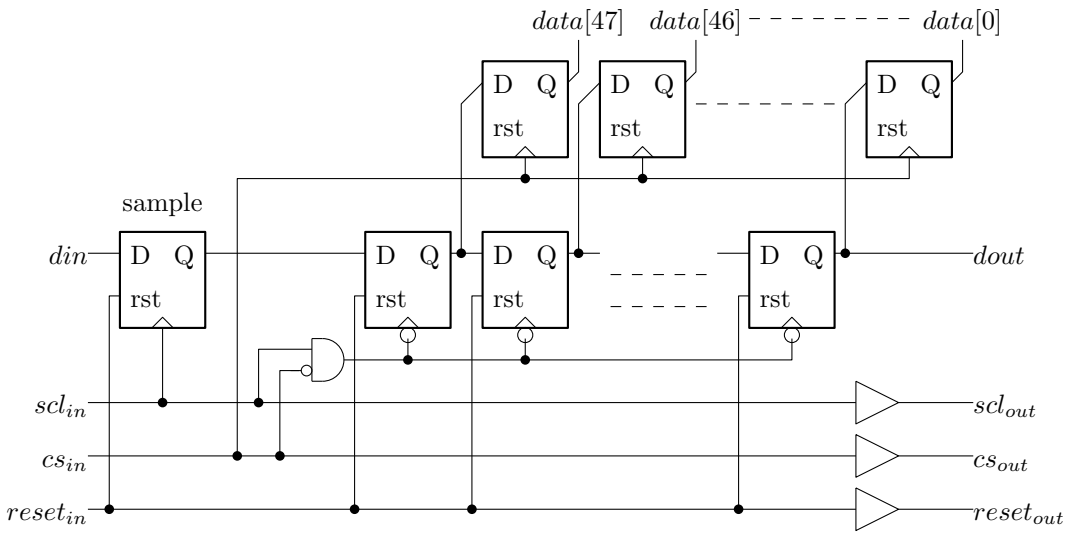

Figure 4.5: SPI architecture showing latched data output, rising-edge sample, falling-edge shift, and buffered through signals.

4.5.1 Local Digital and Switching

The digital section contains the quadrature basis function generator, two OTA tuning registers, integrator control, and a serial communication port. Figure 4.4 illustrates the hardware description level (HDL) design hierarchy and inter-connections. These modules used MyHDL [106] as the design input language and made use of the software's automatic Verilog or VHDL output conversion.

All configuration information is passed into the SPI register and distributed to the NCO and switch control. The reference clock for the NCO is separately passed in. To facilitate abutting the harmonic blocks in the circuit layout, the SPI and NCO clock signals pass through each block on opposite edges. The following sections describe the digital sub-blocks in more detail.

4.5.1.1 Serial Communication

The serial peripheral interface (SPI) was chosen for simple communication of the harmonic control parameters from the system host processor. It is a serial interface with a dedicated clock signal *scl*, serial data input *din*, active-low chain select *cs*, and serial data output. Daisy-chaining the next harmonic's *din* to the previous' *dout* causes the interface to appear to the processor as a long shift register. The register is 48-bits wide with the logical layout given later in Table 4.1.

Figure 4.5 shows a schematic representation of the serial peripheral interface (SPI) for loading configuration values from the processor. The configuration corresponds to the standard SPI mode denoted by `CPOL=0` and `CPHA=0`, or mode 0. This mode corresponds to the clock line *scl* which idles low (`CPOL=0`), and which samples data on the clock's rising edge while propagating data on the clock's falling edge (`CPHA=0`). Start of a data transfer is indicated by a falling edge on the *cs* line. Data is then applied to the *din* pin synchronized with the *scl* data clock line. When all bits have been shifted in, the controller raises the *cs* line which latches the current state of the shift register into the *data* output storage. This ensures that the data output bits do not change as a new data word is being shifted in.

The relative timing or skew between the SPI signals can degrade as they propagate through a long chain of harmonic sections, possibly violating register setup/hold times at the end of the chain. Also, the clock *scl*, chain-select *cs*, and *reset* signals are common to all sections and could present a large load to the input driver. Buffers inserted in these signal lines minimize the load and allow the signal to propagate evenly down the chain. Finally, the D flip-flop labeled "sample" in Figure 4.5 samples the incoming data bit on the rising edge of *scl* while the data is shifted on the falling edge of *scl*. This bi-phase sample-shift operation ensures there will be

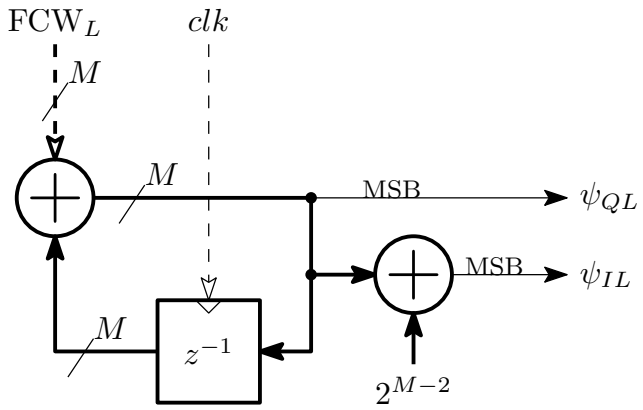

Figure 4.6: Numerically-controlled oscillator with M-bit phase accumulator, M-bit phase increment word, and quadrature output bits.

no skew-related timing errors at any point in the chain if the condition that the *scl* period is longer than twice the longest propagation delay through the entire chain is satisfied — the interface has a maximum shift rate but by design it has no lower rate limit and is inherently immune to timing skew.

Appendix A describes the MyHDL code for the SPI slave module in detail as an example of digital module development using the tool. One advantage with using MyHDL is the ease of implementing test benches for verification of modules. The fact that the tool is written in python, a general-purpose programming language, with features added to describe digital hardware at the register transfer level enables natural description of digital behavior. This is in contrast with the prevailing HDL languages Verilog and VHDL, which must use the limitations of a hardware-oriented language to describe high-level behavior.

4.5.1.2 Basis Function Generator

The quadrature basis function generator is implemented as a numerically-controlled oscillator (NCO). Figure 4.6 shows the functionality of the NCO, consisting of a phase accumulator (PA) register which holds the current phase value, an adder

for incrementing the phase by the value FCW_L, and an adder which increments a static 1/4 of a phase accumulator offset. The most-significant bit of the phase accumulator is used as the quadrature output. Calculation of the in-phase offset in practice does not require a full-width N-bit adder, it only uses a 2-bit adder for the upper two bits of the PA and therefore has little hardware impact.

For a given reference clock frequency f_{ref}, N-bit phase accumulator width, and phase increment FCW, the average output frequency and available frequency resolution are

$$f_{\mathrm{out}} = f_{\mathrm{ref}} \frac{\mathrm{FCW}}{2^N} \tag{4.1}$$

$$\Delta f = \frac{f_{\mathrm{ref}}}{2^N}. \tag{4.2}$$

While the average period of the output signals are as described by Equation (4.1), the instantaneous periods vary between the two integer multiples of the reference clock period f_{ref} on either side of the average value.

4.5.1.3 Tuning and Projection Control

The digital block `SwitchCtl` from Figure 4.4 is a combinational logic block which translates the multiplier command and settings from the SPI register and outputs control signals to the various switches. Table 4.1 describes the bit layout of the 48-bit SPI configuration register. For each quadrature harmonic projection block, there are two instances of projection channels and one digital control block which handles both channels.

Besides the global chip reset, the NCO basis function generator has a reset configuration bit *rst* to ensure all the generators operate with a known phase relationship to other harmonic projection blocks. The projection channels are configured to

bit #	47	[46:32]		[31:16]					[15:0]
block	Ch.-A,B	NCO		Channel-A					Channel-B
name	cal	rst	$FCW_{13:0}$	cintA	zeroA	seA	fastA	$tuneA_{11:0}$	(same)

Table 4.1: Bit layout of the 48-bit SPI register for each harmonic projection.

cal	*se*	Description
0	0	Differential input signal multiplied by basis function. OTA in open-loop.
0	1	*sigA* or *sigB* connected to OTA + input based on *mult* state. OTA in unity-gain feedback.
1	0	Both OTA inputs connected to *CMI*. No feedback.
1	1	*CMI* connected to OTA + input. OTA in unity-gain feedback.

Table 4.2: Projection channel operation mode as a function of the *cal* and *se* configuration bits.

be run in both single-ended and differential input modes during operation according to the state of the *se* bit. Configuration bit *cal* turns on the offset calibration mode. The OTA's switchable mirror ratio discussed in the next section is controlled by the *fast* bit. Finally, bit *Cint* controls whether the integration capacitor is connected to the amplifier output and bit *zero* resets the integration capacitor's voltage to a mid-supply level.

Nine transmission gates switch signals around the OTA and integration capacitor under control of the `SwitchCtl` block according to the selected mode. Table 4.2 describes the four operation modes provided by the *cal* and *se* configuration bits.

Digital offset and gain tuning control for each OTA are provided by the two 12-bit *tuneA* and *tuneB* words. For the current design, the gain and offset tuning code values used 4- and 8-bit resolutions, respectively. This feature is described in more detail later in Section 4.6.1.

Figure 4.7 shows a higher-level overview of the analog portion of the projection

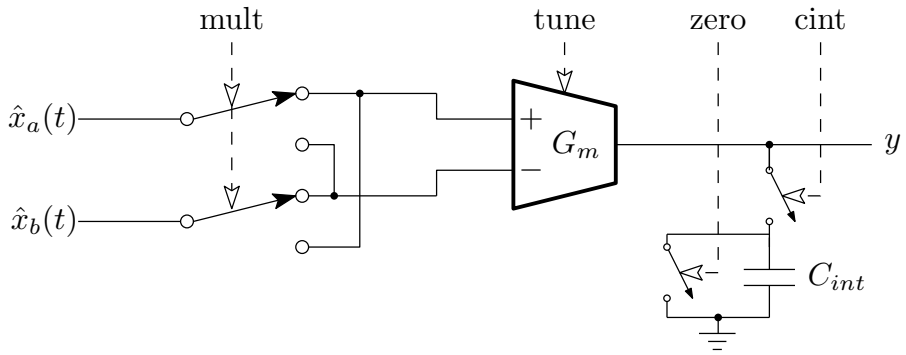

Figure 4.7: Conceptual schematic of analog projection channel showing multiplier, OTA, and integrating capacitor along with control signals.

channel. Two of these channels are included to implement the in-phase and quadrature portions of the harmonic projection. The input signal x is applied differentially as $x = x_a - x_b$, multiplying by ± 1 under control of the *mult* signal. The *zero* and *cint* switches allow disconnection of the integration capacitor from the output node and to reset its voltage to the common-mode voltage (the functional "zero" level for bi-polar integration outputs). Figure 4.8 shows the schematic of the projection channel circuitry with the nine transmission gate switches, OTA, and integration capacitor.

4.5.1.4 Level Translators

The digital portion operates from a nominal 1.2 V supply rail while all analog circuitry operates from a separate 2.5 V nominal supply rail. Control signals which cross the digital-analog boundary must then be translated to the appropriate logic levels. Each translation cell handles a single, differential pair of control signals.

Figure 4.9 shows a single cell of the level-translation circuitry as a bi-stable latch structure. Digital inputs are applied as signals *inA* and *inB* to the 2.5 V-capable input transistors T2 and T3. Cross-coupled transistor pair T1 and T0 provide a positive-feedback action to quickly snap the output nodes *outA* and *outB* to either

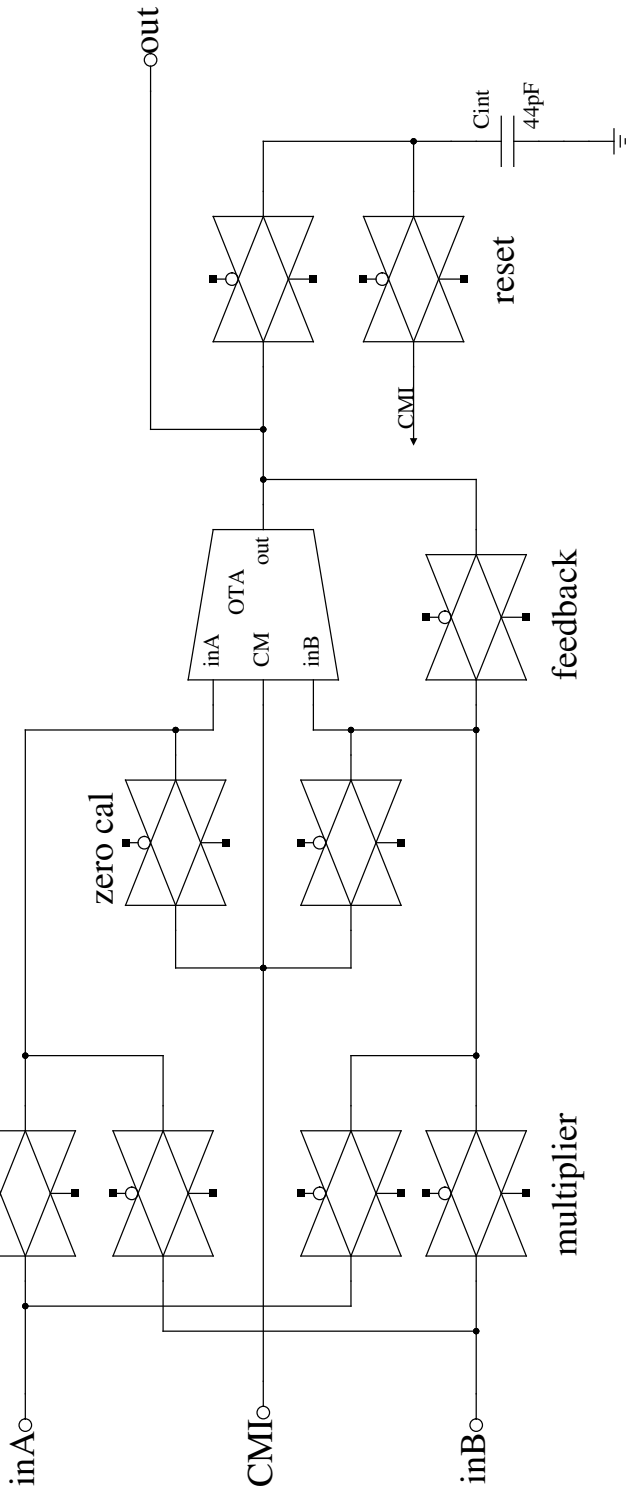

Figure 4.8: Schematic of the analog portion of a single projection channel. Differential signal input is applied at nodes *inA, CMI, inB* and integrator output at node *out*.

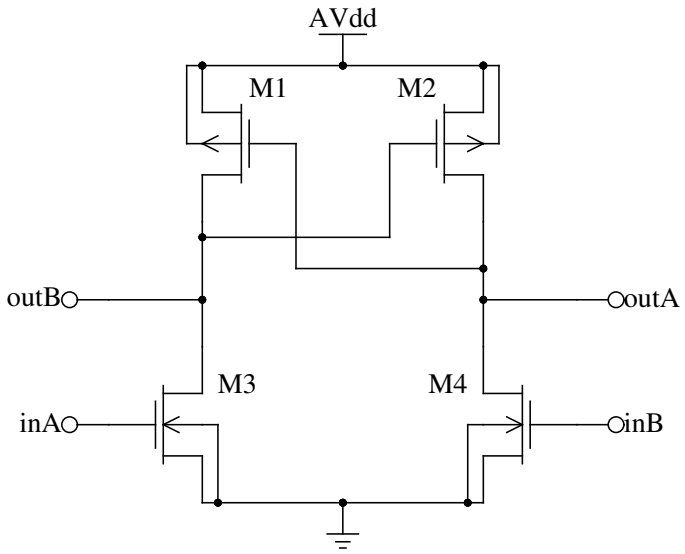

Figure 4.9: Level translator schematic.

the analog supply voltage $AVDD$ or zero. Input transistors are sized to apply a strong enough pull-down to force the latch out of its current state. The PMOS cross-coupled pair are sized to provide a very weak pull-up, with a weak aspect ratio of $(W/L)_p = 0.48/2.40\mu m$.

4.5.2 Analog Integrator

The multiplied waveform is integrated in the analog domain with an OTA-C type integrator. A voltage input signal is converted to an output current with the operational transconductance amplifier (OTA) with a transfer ratio of G_m A/V as in Equation (4.3). This current is applied directly to a linear capacitor C_{int} and the output V_{out} is taken as the capacitor voltage. Equation (4.4) shows the relationship between an input signal integrated for time T and the resulting output voltage value.

$$i_{out}(t) = G_m V_{in}(t) \tag{4.3}$$

$$V_{out} = \frac{1}{C_{int}} \int_0^T i_{out}(t)dt = \frac{G_m}{C_{int}} \int_0^T V_{in}(t)dt \tag{4.4}$$

Figure 4.7 shows a representative schematic of the tunable OTA-C integrator. The integrator time constant required, $\tau = C_{int}/G_m$, depends on the integration time, input voltage amplitude, and output voltage range. At very long time constants, the capacitor should be as large as possible to relax the corresponding OTA's ultra-low G_m requirement.

The IBM-8RF process used for the prototype has a dual-MIM, or metal-oxide-metal-oxide-metal, parallel-plate capacitor option which allows relatively high density, linear capacitors. The lower and upper plates are shorted together to make one plate while the middle metal forms the second plate of the capacitor. Active circuitry is allowed below the capacitors in the process and thus allows area-efficient implementations utilizing large capacitors. For this design, the integration capacitor C_{int} was set to 44 pF. This value corresponds to a capacitor which is only slightly larger than the rest of the OTA layout. Such a capacitor size ensures maximum utilization of available chip area. Due to the complexity of the OTA designed for this system, it is described separately in Section 4.6.

4.5.3 Off-Chip Analog Output

Each of the 48 quadrature harmonic projection channels has two analog outputs. It is not generally feasible to bring all 96 analog voltages off-chip for analog-to-digital conversion at the end of an integration period. A multiplexer and analog pad buffer are used to route each quadrature set signals to a pair of analog output pins on the chip. These two output pins are routed to external ADCs under control of the system processor.

One analog output path multiplexes the in-phase harmonic output while the second routes the quadrature channels. This configuration allows the simultaneous sampling of a quadrature harmonic pair of channels to minimize time-dependent leakage errors. The output to route off-chip and other settings in configured through an SPI-based digital block similar to the OTA configuration block.

Each multiplexer output feeds the input to an amplifier which isolates the sensitive on-chip nets from external influence. To reduce design effort, this buffer was implemented as a copy of the channel OTA with a different digital `SwitchCtl` block to allow unity-gain buffering and local offset calibration. This buffer is sub-optimal due to its high output impedance and slow step response but is sufficient for prototype evaluation.

4.6 Wide-Range Digitally-Tunable OTA

Figure 4.10 shows the OTA implementation, described in detail in the following sections. Bias currents I1 and I2 are digitally-tunable to change the OTA's G_m and to zero the offset current/voltage, described in Section 4.6.1. Differential input transistors M1 and M2, along with linearization elements Ma and Mb perform the main V/I conversion. Output current is generated as the difference between the M1 and M2 drain currents scaled by the mirroring ratios of (M3:M5×M6:M7) and (M4:M5), respectively. For this design, the mirror ratio (M3:M5) was set to unity, while the output node mirrors were constructed with a switchable transfer ratio. The mirror ratio switching is described in Section 4.6.2.