```
1   // Eugene Ngo
2   // 12/2/2022
3   // EE 271
4   // Lab 5
5
6   // doubleFlipFlop module takes in clk, reset, and button as 1-Bit inputs and returns 1-Bit
    out.
7   // This module processes buttons at clock cycles.
8
9   module doubleFlipFlop (clk, reset, button, out);
10
11     input logic clk, reset;
12     input logic button;
13     output logic out;
14
15     logic out_ff1;
16
17     always_ff @(posedge clk) begin
18        out_ff1 <= button;
19     end
20
21     always_ff @(posedge clk) begin
22        out <= out_ff1;
23     end
24  endmodule
25
26  // doubleFlipFlop_testbench tests all expected, unexpected, and edgecase behaviors
27
28  module doubleFlipFlop_testbench();
29
30     logic clk, reset;
31     logic button;
32     logic out;
33
34     doubleFlipFlop dut (.clk, .reset, .button, .out);
35
36     //Set up the clock
37     parameter CLOCK_PERIOD = 100;
38     initial begin
39        clk <= 0;
40        forever #(CLOCK_PERIOD / 2)
41        clk <= ~clk;
42     end
43
44     initial begin
45                         @(posedge clk);
46        reset <= 1;      @(posedge clk);
47                         @(posedge clk);
48        reset <= 0;      @(posedge clk);
49                         @(posedge clk);
50        button <= 1;     @(posedge clk);
51                         @(posedge clk);
52                         @(posedge clk);
53                         @(posedge clk);
54        button <= 0;     @(posedge clk);
55                         @(posedge clk);
56                         @(posedge clk);
57                         @(posedge clk);
58        $stop;
59     end
60  endmodule
```