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          Date: 1/13/2023
 3
          Class: EE 371
 4
          Lab 6
 5
          Taken from Lab 1 and adapted for lab 6 task 1 */
      // seg7 outputs correct decimal value to hex displays based on the output given by the
      counter
 8
      // It also displays "FULL" and "CLEAR" according to the indicator outputs given by the
      counter.
       module seg7 (in, full, clear, hexout0, hexout1, hexout2, hexout3, hexout4, hexout5);
10
11
          input logic full, clear;
12
          input logic [4:0] in;
13
          output logic [6:0] hexout0, hexout1, hexout2, hexout3, hexout4, hexout5;
14
15
          // Assigning hex display variables on necessary numbers.
16
          logic [6:0] hex0, hex1, hex2, hex3, hex4, hex5, hex6, hex7, hex8, hex9;
          assign hex0 = 7'b1000000; //
assign hex1 = 7'b1111001; //
assign hex2 = 7'b0100100; //
assign hex3 = 7'b0110000; //
17
18
19
20
          assign hex4 = 7'b0011001; //
assign hex5 = 7'b0010010; //
21
22
23
          assign hex6 = 7'b0000010; //
          assign hex7 = 7'b1111000; //
24
25
          assign hex8 = 7'b00000000; // 8
26
27
          assign hex9 = 7'b0010000; // 9
28
29
          // Assigning hex display variables on necessary letters.
         // Assigning nex display variables on necessary letters.
logic [6:0] hexf, hexu, hexl, hexc, hexe, hexa, hexr, hexoff;
assign hexf = 7'b0001110; // F
assign hexu = 7'b1000111; // L
assign hexc = 7'b1000110; // C
assign hexe = 7'b0000100; // A
assign hexr = 7'b0001001; // R
30
31
32
33
34
35
          assign hexr = 7'b0101111; // R
assign hexoff = 7'b1111111; // off
36
37
38
39
40
          // Logic for hexout0: 26 different cases for 26 numbers. (0-25)
          always_comb begin
41
              case(in)
42
                   b00000: hexout0 = hex0;
43
                 5'b00001: hexout0 = hex1;
44
45
                  5'b00010: hexout0 = hex2;
                 5'b00011: hexout0 = hex3;
46
                 5'b00100: hexout0 = hex4;
47
48
                 5'b00101: hexout0 = hex5;
                 5'b00110: hexout0 = hex6;
49
                 5'b00111:
                              hexout0 = hex7
50
51
52
53
54
55
56
57
58
                 5'b01000: hexout0 = hex8;
                 5'b01001: hexout0 = hex9;
                 5'b01010: hexout0 = hex0;
                 5'b01011: hexout0 = hex1;
                 5'b01100: hexout0 = hex2;
                 5'b01101: hexout0 = hex3;
                 5'b01110: hexout0 = hex4;
                 5'b01111: hexout0 = hex5;
                 5'b10000: hexout0 = hex6;
59
                   b10001: hexout0 = hex7;
60
                   'b10010: hexout0 = hex8;
61
                   'b10011: hexout0 = hex9;
                 5'b10100:
62
                             hexout0 = hex0;
                 5'b10101:
63
                              hexout0 = hex1;
                 5'b10110:
64
                             hexout0 = hex2;
65
                 5'b10111: hexout0 = hex3;
                   'b11000: hexout0 = hex4;
66
                 5'b11001: hexout0 = hex5;
67
68
                 default: hexout0 = 7'bx;
              endcase
70
          end // always_comb
71
```

```
// Logic for hexout1: 26 different cases for 26 numbers. (0-25)
 73
          always_comb begin
 74
             case(in)
                   b00000: hexout1 = hexr;
 75
                  'b00001: hexout1 = hexoff;
 76
                  'b00010:
                           hexout1 = hexoff
 78
                  'b00011:
                           hexout1 = hexoff:
 79
                           hexout1 = hexoff:
                  'b00100:
 80
                 5'b00101:
                           hexout1 = hexoff
                5'b00110: hexout1 = hexoff
 81
 82
                 5'b00111: hexout1 = hexoff
 83
                 5'b01000: hexout1 = hexoff:
 84
                 5'b01001: hexout1 = hexoff:
 85
                 5'b01010: hexout1 = hex1;
 86
                 5'b01011: hexout1 = hex1;
 87
                 5'b01100: hexout1 = hex1;
 88
                 5'b01101: hexout1 = hex1;
 89
                 5'b01110: hexout1 = hex1;
 90
                  'b01111: hexout1 = hex1;
                 5'b10000: hexout1 = hex1;
 91
 92
                 5'b10001:
                           hexout1 = hex1;
 93
                 5'b10010: hexout1 = hex1;
 94
                 5'b10011:
                           hexout1 = hex1;
 95
                 5'b10100:
                           hexout1 = hex2
 96
                 5'b10101: hexout1 = hex2:
 97
                 5'b10110: hexout1 = hex2;
 98
                 5'b10111: hexout1 = hex2;
 99
                 5'b11000: hexout1 = hex2;
100
                 5'b11001: hexout1 = hex2;
101
                default: hexout1 = 7'bx;
102
             endcase
103
          end // always_comb
104
105
          // Logic for hexout5 - hexout2: display letters when full or clear, turn off otherwise.
          always_comb begin if (full) begin
106
107
108
                 hexout5 = hexf;
109
                 hexout4 = hexu;
110
                hexout3 = hex1
111
                hexout2 = hex1;
112
             end
113
             else if (clear) begin
114
                hexout5 = hexc;
115
                 hexout4 = hex1;
116
                hexout3 = hexe;
                hexout2 = hexa;
117
118
             end
119
             else begin
120
                 hexout5 = hexoff;
                hexout4 = hexoff;
                hexout3 = hexoff:
                 hexout2 = hexoff;
123
124
             end
125
          end // always_comb
126
127
        endmodule // seg7
128
129
        // seg7_testbench tests all expected, unexpected, and edgecase behaviors
130
       module seg7_testbench();
          logic full, clear;
131
          logic [4:0] in;
logic [6:0] hexout0, hexout1, hexout2, hexout3, hexout4, hexout5;
132
133
134
135
          seg7 dut (.in, .full, .clear, .hexout0, .hexout1, .hexout2, .hexout3, .hexout4, .hexout5);
             in = 0; clear = 1; full = 0; #10; // testing clear output
138
             in = 5'b11001; clear = 0; full = 1; #10; // testing full output in = 5'b10011; clear = 0; full = 0; #10; // testing regular output
139
140
141
             $stop;
      end // initial
endmodule // seg7_testbench
142
143
```