```
1   /* Name: Eugene Ngo
2      Date: 3/7/2023
3      Class: EE 371
4      Lab 6: Parking Lot 3D Simulation
5
6   */
7
8   // Clock divider for hardware testing. Takes 1-bit input clock and reset and outputs
9   // 32-bit divided_clocks to get slower clocking for testing on the hardware.
10  // Module was borrowed from EE 271.
11  // divided_clocks[0] = 25MHz, [1] = 12.5Mhz, ... [23] = 3Hz, [24] = 1.5Hz, [25] = 0.75Hz, ..
12  `timescale 1 ps / 1 ps
13  module clock_divider (clock, reset, divided_clocks);
14     input logic reset, clock;
15     output logic [31:0] divided_clocks = 0;
16
17     always_ff @(posedge clock) begin
18        divided_clocks <= divided_clocks + 1;
19     end // always_ff
20
21  endmodule // clock_divider
22
```