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55 56 57

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61 62

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```
// megafunction wizard: %RAM: 2-PORT%
// GENERATION: STANDARD
// VERSION: WM1.0
// MODULE: altsyncram
// Megafunction Name(s):
// altsyncram
   Simulation Library Files(s):
//
              altera mf
   ***************
   THIS IS A WIZARD-GENERATED FILE. DO NOT EDIT THIS FILE!
// 17.0.0 Build 595 04/25/2017 SJ Lite Edition
// ******************
//Copyright (C) 2017 Intel Corporation. All rights reserved. //Your use of Intel Corporation's design tools, logic functions
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//associated documentation or information are expressly subject
//to the terms and conditions of the Intel Program License
//Subscription Agreement, the Intel Quartus Prime License Agreement,
//the Intel MegaCore Function License Agreement, or other
//applicable license agreement, including, without limitation, //that your use is for the sole purpose of programming logic //devices manufactured by Intel and sold by Intel or its
//authorized distributors. Please refer to the applicable
//agreement for further details.
// synopsys translate_off
`timescale 1 ps / 1 ps
// synopsys translate_on
module ram16x8 (
   clock,
   data,
   rdaddress,
   wraddress,
   wren,
   q);
            clock;
   input
   input [7:0]
input [3:0]
input [3:0]
                  data;
                   rdaddress;
                   wraddress;
   input wren;
output [7:0]
`ifndef ALTERA_RESERVED_QIS
// synopsys translate_off
 endif
   tri1
             clock;
             wren;
 ifndef ALTERA_RESERVED_QIS
// synopsys translate_on
 endif
   wire [7:0] sub_wire0;
wire [7:0] q = sub_wire0[7:0];
   altsyncram altsyncram_component (
               .address_a (wraddress),
               .address_b (rdaddress),
               .clock0 (clock),
               .data_a (data),
               .wren_a (wren)
               .q_b (sub_wire0),
               .aclr0 (1'b0),
```

```
.aclr1 (1'b0),
  75
                             .addressstall_a (1'b0),
  76
                             .addresssta]1_b(1'b0),
                             .byteena_a (1'b1),
.byteena_b (1'b1),
.clock1 (1'b1),
.clocken0 (1'b1),
  79
                             .clocken0 (1 b1),
.clocken1 (1'b1),
.clocken2 (1'b1),
.clocken3 (1'b1),
.data_b ({8{1'b1}}),
 83
                             .eccstatus (),
                             .q_a (),
 86
                             .rden_a (1'b1),
.rden_b (1'b1),
 87
 88
                             .wren_b (1'b0));
 89
 90
              defparam
 91
                   altsyncram_component.address_aclr_b = "NONE'
                   altsyncram_component.address_reg_b = "CLOCKO"
 92
                  altsyncram_component.aduress_reg_b = CLOCKO",
altsyncram_component.clock_enable_input_a = "BYPASS",
altsyncram_component.clock_enable_input_b = "BYPASS",
altsyncram_component.clock_enable_output_b = "BYPASS",
altsyncram_component.init_file = "ram16x8.mif",
altsyncram_component.intended_device_family = "Cyclone V",
altsyncram_component.lpm_type = "altsyncram",
altsyncram_component.numwords_a = 16
 93
 94
 95
 96
 97
 98
 99
                   altsyncram_component.numwords_a = 16,
100
                   altsyncram_component.numwords_b = 16,
101
                   altsyncram_component.operation_mode = "DUAL_PORT",
                   altsyncram_component outdata_aclr_b = "NONE", altsyncram_component outdata_reg_b = "CLOCKO"
102
103
                   altsyncram_component.power_up_uninitialized = "FALSE", altsyncram_component.ram_block_type = "M10K",
104
105
106
                   altsyncram_component.read_during_write_mode_mixed_ports = "DONT_CARE",
107
                   altsyncram_component.widthad_a = 4,
108
                   altsyncram_component.widthad_b = 4,
109
                   altsyncram_component.width_a = 8,
110
                   altsyncram_component.width_b = 8,
111
                   altsyncram_component.width_byteena_a = 1;
112
113
114
         endmodule
115
116
              CNX file retrieval info
117
118
         /// Retrieval info: PRIVATE: ADDRESSSTALL_A NUMERIC "0"
// Retrieval info: PRIVATE: ADDRESSSTALL B NUMERIC "0"
119
120
         // Retrieval info: PRIVATE: ADDRESSSTALL_B NUMERIC
121
          // Retrieval info: PRIVATE: BYTEENA_ACLR_A NUMERIC
         // Retrieval info: PRIVATE: BYTEENA_ACLR_B NUMERIC // Retrieval info: PRIVATE: BYTE_ENABLE_A NUMERIC '/ Retrieval info: PRIVATE: BYTE_ENABLE_B NUMERIC '/ Retrieval info: PRIVATE: BYTE_SIZE NUMERIC "8"
122
123
124
125
          // Retrieval info: PRIVATE: BlankMemory NUMERIC "O"
126
         /// Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_A NUMERIC "0"
// Retrieval info: PRIVATE: CLOCK_ENABLE_INPUT_B NUMERIC "0"
127
128
          // Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_A NUMERIC "O"
129
         // Retrieval info: PRIVATE: CLOCK_ENABLE_OUTPUT_B NUMERIC "O"
130
131
         // Retrieval info: PRIVATE: CLRdata NUMERIC "0"
132
          // Retrieval info: PRIVATE: CLRq NUMERIC "0"
133
         // Retrieval info: PRIVATE: CLRrdaddress NUMERIC "O"
134
         // Retrieval info: PRIVATE: CLRrren NUMERIC "0"
          // Retrieval info: PRIVATE: CLRwraddress NUMERIC "O"
135
         // Retrieval info: PRIVATE: CLRWren NUMERIC "0"
// Retrieval info: PRIVATE: Clock NUMERIC "0"
// Retrieval info: PRIVATE: Clock_A NUMERIC "0"
// Retrieval info: PRIVATE: Clock_B NUMERIC "0"
// Retrieval info: PRIVATE: IMPLEMENT_IN_LES NUMERIC "0"
136
137
138
139
140
         /// Retrieval info: PRIVATE: INDATA_ACLR_B NUMERIC "0"
// Retrieval info: PRIVATE: INDATA_REG_B NUMERIC "0"
141
142
         // Retrieval info: PRIVATE: INIT_FILE_LAYOUT STRING "PORT_B"
// Retrieval info: PRIVATE: INIT_TO_SIM_X NUMERIC "0"
143
144
145
              Retrieval info: PRIVATE: INTENDED_DEVICE_FAMILY STRING "Cyclone V"
          // Retrieval info: PRIVATE: JTAG_ENABLED NUMERIC "0"
146
```

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// Retrieval info: PRIVATE: JTAG_ID STRING "NONE"
148
             // Retrieval info: PRIVATE: MAXIMUM_DEPTH NUMERIC "O"
            // Retrieval info: PRIVATE: MEMSIZE NUMERIC "128"
// Retrieval info: PRIVATE: MEM_IN_BITS NUMERIC "0"
// Retrieval info: PRIVATE: MIFfilename STRING "ram16x8.mif"
// Retrieval info: PRIVATE: OPERATION_MODE NUMERIC "2"
// Retrieval info: PRIVATE: OUTDATA_ACLR_B NUMERIC "0"
// Retrieval info: PRIVATE: OUTDATA_REG_B NUMERIC "1"
// Retrieval info: PRIVATE: RAM_BLOCK_TYPE NUMERIC "2"
// Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_MIXED_PORTS NUMERIC "2"
// Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_PORT_A NUMERIC "3"
// Retrieval info: PRIVATE: READ_DURING_WRITE_MODE_PORT_B NUMERIC "3"
// Retrieval info: PRIVATE: REGdata NUMERIC "1"
// Retrieval info: PRIVATE: REGdata NUMERIC "1"
// Retrieval info: PRIVATE: REGGATES NUMERIC "1"
149
             // Retrieval info: PRIVATE: MEMSIZE NUMERIC "128
150
151
152
153
154
155
156
157
158
159
160
             /// Retrieval info: PRIVATE: REGrdaddress NUMERIC "1"
161
             // Retrieval info: PRIVATE: REGrren NUMERIC "1"
162
163
             // Retrieval info: PRIVATE: REGWraddress NUMERIC "1"
             // Retrieval info: PRIVATE: REGwren NUMERIC "1"
164
             // Retrieval info: PRIVATE: REGWREN NUMERIC "I"
// Retrieval info: PRIVATE: SYNTH_WRAPPER_GEN_POSTFIX STRING "O"
// Retrieval info: PRIVATE: USE_DIFF_CLKEN NUMERIC "O"
// Retrieval info: PRIVATE: UseDPRAM NUMERIC "1"
// Retrieval info: PRIVATE: Varwidth NUMERIC "O"
// Retrieval info: PRIVATE: WIDTH_READ_A NUMERIC "8"
// Retrieval info: PRIVATE: WIDTH_READ_B NUMERIC "8"
// Retrieval info: PRIVATE: WIDTH_WRITE_A NUMERIC "8"
// Retrieval info: PRIVATE: WIDTH_WRITE_B NUMERIC "8"
// Retrieval info: PRIVATE: WRADDR_ACLR_B NUMERIC "O"
// Retrieval info: PRIVATE: WRADDR_REG_B NUMERIC "O"
165
166
167
168
169
170
171
172
173
             // Retrieval info: PRIVATE: WRADDR_REG_B NUMERIC "O"
// Retrieval info: PRIVATE: WRCTRL_ACLR_B NUMERIC "O"
// Retrieval info: PRIVATE: enable NUMERIC "O"
174
175
176
             // Retrieval info: PRIVATE: rden NUMERIC "O"
177
178
             // Retrieval info: LIBRARY: altera_mf altera_mf.altera_mf_components.all
             // Retrieval info: CONSTANT: ADDRESS_ACLR_B STRING "NONE"
// Retrieval info: CONSTANT: ADDRESS_REG_B STRING "CLOCKO"
// Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_A STRING "BYPASS"
// Retrieval info: CONSTANT: CLOCK_ENABLE_INPUT_B STRING "BYPASS"
// Retrieval info: CONSTANT: CLOCK_ENABLE_OUTPUT_B STRING "BYPASS"
179
180
181
182
183
             // Retrieval info: CONSTANT: INIT_FILE STRING "ram16x8.mif"
// Retrieval info: CONSTANT: INTENDED_DEVICE_FAMILY STRING "Cyclone V"
// Retrieval info: CONSTANT: LPM_TYPE STRING "altsourcam"
184
185
186
             // Retrieval info: CONSTANT: NUMWORDS_A NUMERIC "16"
187
             // Retrieval info: CONSTANT: NUMWORDS_B NUMERIC "16"
188
             // Retrieval info: CONSTANT: OPERATION_MODE STRING "DUAL_PORT" // Retrieval info: CONSTANT: OUTDATA_ACLR_B STRING "NONE"
189
190
191
             // Retrieval info: CONSTANT: OUTDATA_REG_B STRING "CLOCKO"
             // Retrieval info: CONSTANT: POWER_UP_UNINITIALIZED STRING "FALSE"
// Retrieval info: CONSTANT: RAM_BLOCK_TYPE STRING "M10K"
192
193
             // Retrieval info: CONSTANT: READ_DURING_WRITE_MODE_MIXED_PORTS STRING "DONT_CARE"
// Retrieval info: CONSTANT: WIDTHAD_A NUMERIC "4"
// Retrieval info: CONSTANT: WIDTH_A NUMERIC "4"
// Retrieval info: CONSTANT: WIDTH_A NUMERIC "8"
// Retrieval info: CONSTANT: WIDTH_B NUMERIC "8"
194
195
196
197
198
             // Retrieval info: CONSTANT: WIDTH_B NOMERIC 8
// Retrieval info: CONSTANT: WIDTH_BYTEENA_A NUMERIC "1"
// Retrieval info: USED_PORT: clock 0 0 0 0 INPUT VCC "clock"
// Retrieval info: USED_PORT: data 0 0 8 0 INPUT NODEFVAL "data[7..0]"
// Retrieval info: USED_PORT: q 0 0 8 0 OUTPUT NODEFVAL "q[7..0]"
// Retrieval info: USED_PORT: rdaddress 0 0 4 0 INPUT NODEFVAL "rdaddress[3..0]"
// Retrieval info: USED_PORT: wrand 0 0 0 0 INPUT NODEFVAL "wraddress[3..0]"
199
200
201
202
203
204
             // Retrieval info: USED_PORT: wren 0 0 0 0 INPUT GND "wren"
205
206
             // Retrieval info: CONNECT: @address_a 0 0 4 0 wraddress 0 0 4 0
207
             // Retrieval info: CONNECT: @address_b 0 0 4 0 rdaddress 0 0 4 0
208
             // Retrieval info: CONNECT: @clock0 0 0 0 clock 0 0 0 0
             // Retrieval info: CONNECT: @data_a 0 0 8 0 data 0 0 8 0 // Retrieval info: CONNECT: @wren_a 0 0 0 0 wren 0 0 0 0 // Retrieval info: CONNECT: q 0 0 8 0 @q_b 0 0 8 0 // Retrieval info: GEN_FILE: TYPE_NORMAL ram16x8.v TRUE // Retrieval info: GEN_FILE: TYPE_NORMAL ram16x8.inc FALSE
209
210
211
212
213
             // Retrieval info: GEN_FILE: TYPE_NORMAL ram16x8.cmp FALSE
// Retrieval info: GEN_FILE: TYPE_NORMAL ram16x8.bsf FALSE
214
215
216
             // Retrieval info: GEN_FILE: TYPE_NORMAL ram16x8_inst.v FALSE
217
             // Retrieval info: GEN_FILE: TYPE_NORMAL ram16x8_bb.v TRUE
218
              // Retrieval info: LIB_FILE: altera_mf
219
```

Date: January 25, 2023